PHILIPS

Data handbook

Electronic components and materials

Integrated circuits

Part 9 March 1982

Signetics TTL Logic

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TTL Logic Data Manual 1982

Signetics

Behind any work of this size, there is invariably a group of individuals whose dedication overcomes the seemingly endless stream of problems, questions, and decisions that must be solved, answered, and met. The editors wish to thank Rosalie McClelland and Steve Pankretz for organizing, proofreading, and checking the thousands of specifications contained in this book. Without their dedication it would not have been possible.

PREFACE

Signetics would like to thank you for your interest in our products. We hope you find the product information you need on the TTL data sheets contained in this data manual. The information is presented in a concise and consistent format for easy device and parameter location.

This manual contains product information on most of the Signetics TTL Logic devices. The majority of this book is dedicated to the three 54/74 families of products, i.e., 54/74, 54S/74S and 54LS/74LS. Each data sheet contains the unique dc and ac data for all of the 54/74 families covered by that device type.

This book contains a compilation of most TTL products currently available. Signetics is continually developing new products. As you see new product announcements, you should contact your local Signetics sales office, representative or authorized distributor or write Signetics, c/o Information Services at 811 East Arques Avenue, P.O. Box 409, Sunnyvale, California 94086, for the latest technical information.

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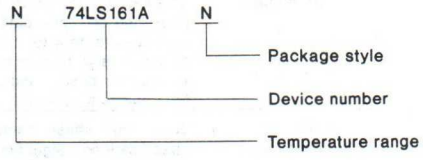
ORDERING INFORMATION

The SigneticsTTL logic products are available in a variety of packages and two temperature ranges. The correct ordering code or part number for the devices is an alpha-numeric sequence as explained below. The commercial range (7400, N8T, etc.) devices are available in plastic and ceramic dual-in-line (DIP) packages, and the military range (5400, S8T, etc.) devices are available in ceramic DIP and ceramic flat packs. All devices are not available in both temperature ranges or all packages. The ordering codes on the individual data sheets indicate the normal or planned availability of the product. However, the availability of specific part numbers can be obtained from your local Signetics sales office or franchised distributor.

Ordering Code



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
N = Commercial range 0°C to 70°C	74LS161A	F = Ceramic DIP N = Plastic DIP
S = Military range −55°C to 125°C	54LS161A	F = Ceramic DIP I = Ceramic DIP Q = Ceramic Flatpack W = Ceramic Flatpack

TTL PRODUCT STATUS AND DEFINITIONS

DEFINITION OF TERMS

Data Sheet Identification	Product Status	Definition
Preview	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Advance Information	Sampling or Pre-Production	This data sheet contains advance information and specifications are subject to change without notice.
Preliminary	First Production	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Selection Guide

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SELECTION GUIDE

ARITHMETIC FUNCTIONS AND OPERATORS

FUNCTION	TYPE	FAMILIES			BITS
		STD	S	LS	
	54/74				
Adders	83	X		X	4 + 4 + Carry
Adders	283			X	4 + 4 + Carry
Arithmetic logic unit	181	X	X	X	4-Bit Binary
Carry lookahead unit	182		X		Lookahead Over 16-Bits
Comparator magnitude	85	X	X	X	4
Encoder, priority	147	X			10-to-4
Encoder, priority	148	X			8-to-3
Parity generator/checker	180	X			8-Bit Odd/Even
Parity generator/checker	280		X		8-Bit Odd/Even
Shifter	350		X		4-Bit, 4-Way Shifter

COUNTERS ASYNCHRONOUS (RIPPLE)

FUNCTION	TYPE	FAMILIES			MODULO
		STD	S	LS	
	54/74				
Decade	90	X		X	2 × 5
Divide-by-12	92	X		X	2 × 6
Binary	93	X		X	2 × 8
Binary	197			X	2 × 8
Decade	290			X	2 × 5
Binary	293			X	2 × 8
Dual decade	390			X	2 × 5 × 2 × 5
8-bit binary	393			X	16 × 16
Dual decade	490			X	10 × 10

COUNTERS, SYNCHRONOUS

FUNCTION	TYPE	FAMILIES			COUNTER TYPES
		STD	S	LS	
	54/74				
Decade	160	X		X	BCD, Master Reset
Binary	161	X		X	4-Bit, Master Reset
Decade	162			X	BCD, Synchronous Reset
Binary	163	X		X	4-Bit, Synchronous Reset
U/D decade	168		X	X	BCD, Synchronous Expansion
U/D binary	169		X	X	4-Bit, Synchronous Expansion
U/D decade	190	X			BCD, U/D Mode Control
U/D binary	191	X		X	4-Bit, U/D Mode Control
U/D decade	192	X		X	BCD, Separate U and D Clocks
U/D binary	193	X		X	4-Bit, Separate U and D Clocks
U/D decade	568			X	BCD, 3-State, Sync and Async Reset
U/D binary	569			X	4-Bit, 3-State, Sync and Async Reset

DECODERS/DEMULTIPLEXERS

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
Dual 1-of-4	139		X	X	Separate Address
Dual 1-of-4	155	X		X	Common Address
Dual 1-of-4	156	X		X	Open Collector Outputs
Dual 1-of-4	256			X	Active HIGH Outputs
1-of-8	138		X	X	3-Enables
1-of-8	259			X	Active HIGH Outputs
1-of-10	42	X		X	BCD, Blank Above "9"
1-of-10	45	X			80mA, 30V Outputs
1-of-10	145	X			80mA, 15V Outputs
1-of-10	445			X	80mA, 7V Outputs
1-of-16	154	X		X	2-Enables

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INTERFACE

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
Quad Buffer	125	X		X	Octal Transceiver, Inverting, Common Enables
Quad Buffer	126	X		X	Octal Transceiver, Inverting, Separate Enables
Octal Buffer	240		X	X	Inverting, 3-State Outputs
Octal Buffer	241		X	X	Non-Inverting, 3-State Outputs
Quad Transceiver	242			X	Inverting, 3-State Outputs
Quad Transceiver	243			X	Non-Inverting, 3-State Outputs
Octal Buffer	244		X	X	Non-Inverting, 3-State Outputs
Octal Transceiver	245			X	Chip Enable and Send/Receive Inputs, 3-State Outputs
Octal D Flip-Flop	273		X	X	Common Clock, Asynchronous Master Reset, Edge-Triggered, MOS Compatible
Octal Transparent Latch	363			X	Common Latch Enable, 3-State Output, MOS Compatible
Octal D Flip-Flop	364			X	Common Clock, Edge-Triggered, 3-State Outputs, MOS Compatible
Hex Buffer/Driver	365A	X		X	Common Enable, 3-State Outputs, Non-Inverting
Hex Inverter Buffer	366A	X		X	Common Enable, 3-State Outputs
Hex Buffer/Driver	367A	X		X	4-Bit and 2-Bit, 3-State Outputs, Non-Inverting
Hex Inverter Buffer	368A	X		X	4-Bit and 2-Bit, 3-State Outputs
Octal Transparent Latch	373		X	X	Independent Latch Enable and Output Enable, MOS Compatible, 3-State
Octal D Flip-Flop	374		X	X	Independent Clock and Output Enable, Edge-Triggered, 3-State
Octal D Flip-Flop	377			X	Common Clock, Clock Enable Input, Edge-Triggered
Octal D Flip-Flop	534		X		Common Output Enable, Positive Edge-Triggered Register, 3-State
Octal Bus Transceiver	640			X	PNP Inputs, Inverting 3-State Outputs, Hysteresis
Octal Bus Transceiver	641			X	Open Collector, Non-Inverting, PNP Inputs, Hysteresis
Octal Bus Transceiver	642			X	Open Collector, Inverting, PNP Inputs, Hysteresis
Octal Bus Transceiver	645			X	PNP Inputs, Non-Inverting 3-State Outputs, Hysteresis
	8T				
Quad Bus Transceiver	26A		X		48mA Low-State Drive, 200μA Bus Loading, MOS/CMOS Interface, High Speed, Inverting
Quad Bus Transceiver	28		X		48mA Low-State Drive, 200μA Bus Loading, MOS/CMOS Interface, High Speed, Non-Inverting
Hex Buffer	95		X		PNP Inputs, High Speed, Common Control Line, MOS/CMOS Compatible
Hex Inverter	96		X		PNP Inputs, High Speed, Common Control Line, MOS/CMOS Compatible
Hex Buffer	97		X		PNP Inputs, High Speed, 2-Bit, 4-Bit Control Line, MOS/CMOS Compatible
Hex Inverter	98		X		PNP Inputs, High Speed, 2-Bit, 4-Bit Control Line, MOS/CMOS Compatible
Octal Transceiver	125			X	PNP Inputs, 3-State Inverting Outputs, Hysteresis
Quad Transceiver	126			X	PNP Inputs, Separate Send/Receive Inputs, 3-State, Inverting, MOS Compatible
Quad Transceiver	127			X	PNP Inputs, Common Chip Enable and a Send/Receive Input, 24mA Drive
Quad Transceiver	128			X	PNP Inputs, Separate Send/Receive Inputs, 3-State, Non-Inverting, MOS Compatible
Quad Transceiver	129			X	PNP Inputs, Common Chip Enable and a Send/Receive Input, 25mA Drive
Octal Transparent Latch	S805		X		Independent Latch Enable and Output Enable, 3-State Output Buffers, MOS Compatible
Octal D Flip-Flop	S806		X		Independent Clock and Output Enable, Positive Edge-Triggered Register, 3-State Output Buffers
Octal Transparent Latch	S807		X		Independent Latch Enable and Output Enable, MOS Compatible, 3-State Output Buffers
Octal D Flip-Flop	S808		X		Independent Clock and Output Enable, Positive Edge-Triggered Register, 3-State, MOS Compatible
Octal Transparent Latch	S809		X		Independent Latch Enable and Output Control, 3-State Inverting Output Buffers

SELECTION GUIDE

LATCHES, TRANSPARENT

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
4-bit D	75	X		X	True and Complement Outputs
4-bit D	197			X	Also 4-Bit Counter
4-bit D	375			X	True and Complement Outputs
4-bit R-S	279	X			Switch Debouncer
Dual 4-bit	256			X	Addressable
Dual 4-bit	116	X			Gated Enable, Master Reset
8-bit D	363			X	3-State, MOS Compatible
8-bit D	373			X	3-State
8-bit	259			X	Addressable
	8T				
8-bit	S805		X		Independent Latch Enable, 3-State, MOS Compatible
8-bit	S807		X		Independent Latch Enable, 3-State, MOS Compatible
8-bit	S809		X		Independent Latch Enable and Output Control, 3-State, Inverting

MULTIPLEXERS

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
Quad 2-input	157	X	X	X	True Outputs
Quad 2-input	158	X	X	X	Complement Outputs
Quad 2-input	257		X	X	3-State "157," Buffer Outputs
Quad 2-input	258		X	X	3-State "158," Buffer Outputs
Quad 2-port	298	X		X	Register Outputs
Dual 4-input	153	X	X	X	Separate Enables
Dual 4-input	253		X	X	3-State "153"
8-input	151	X	X	X	True and Complement Outputs
8-input	251		X	X	3-State "151," Buffer Outputs
16-input	150	X			True and Complement Outputs

REGISTERS, PARALLEL IN-PARALLEL OUT

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
4-bit	173	X		X	3-State Outputs
4-bit	175	X	X	X	True and Complement Outputs, $\overline{MR}$ Input
4-bit	298	X		X	Multiplex Data Inputs
4 x 4	170	X		X	4-Addressable Register
4 x 4	670			X	3-State "LS170"
6-bit	174	X	X	X	Master Reset Input
6-bit	378			X	Clock Enable Input
8-bit	273		X	X	Master Reset Input
8-bit	377			X	Clock Enable Input
8-bit	364			X	3-State MOS Compatible Outputs
8-bit	374		X	X	3-State Outputs
16-bit	172		X		8 x 2, Independent Read and Write Ports
8-bit	534		X		Common Output Enable, Edge-Triggered, 3-State
	8T				
8-bit	S806		X		Independent Clock and Output Enable, 3-State, Edge-Triggered
8-bit	S808		X		Independent Latch Enable and Output Control, 3-State, Inverting

SELECTION GUIDE

REGISTERS, SHIFT-LOAD

FUNCTION	TYPE	FAMILIES			FEATURES
		STD	S	LS	
	54/74				
4-bit	94	X			Parallel In-Serial Out
4-bit	95	X		X	Separate Shift and Load Clocks
4-bit	194	X	X	X	Shift Right/Left Parallel Load
4-bit	195	X	X	X	Shift Right, Parallel Load
4-bit	295			X	Shift-Load, 3-State Outputs
4-bit	395			X	Expandable Shift, 3-State Outputs
5-bit	96	X		X	Shift Right, Parallel Load
8-bit	91	X			Serial In-Serial Out
8-bit	164	X		X	Serial In-Parallel
8-bit	165	X			Parallel In-Serial Out
8-bit	166	X			Parallel In-Serial Out
8-bit	199	X			Universal, Reversible, Shift-Load

Section 2
TTL User's Guide

INTRODUCTION

The TTL Logic devices described in this data manual differ widely in function, complexity and performance, but their electrical input and output characteristics are very similar and are defined and tested to guarantee compatibility. The data sheets that make up this book cover four major categories of TTL circuits and a series of TTL compatible interface products.

The oldest TTL product category is the gold-doped double-diffused type which is made up of the 54/7400 family of devices. This family reflects the same performance ranges and differ only in functions and pin configuration.

The remaining two categories of products are fabricated with a non-saturating Schottky clamped transistor technique. The 54S/74S00 family of TTL products are very high performance, high power devices. The most popular TTL category is the 54LS/74LS Low Power Schottky family. These products feature the performance of the 54/74 family at about 1/4 the power.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings constitute limiting values above which serviceability of the device may be impaired. Provisions should be made in system design and testing to limit voltages and currents as shown below.

OPERATING TEMPERATURE AND VOLTAGE RANGES

The nominal supply voltage (V_{CC}) for all TTL circuits is +5.0 volts. Commercial grade parts are guaranteed to perform with a ±5% supply tolerance (±250mV) over an ambient temperature range of 0°C to 70°C.

The Military grade parts are guaranteed to perform with a ±10% supply tolerance (±500mV) over an ambient temperature range of −55°C to +125°C.

The actual junction temperature can be calculated by multiplying the power dissipation of the device with the thermal resistance of the package and adding it to the measured ambient temperature T_A or package (case) temperature T_C. The thermal resistance for the various packages in which the TTL products are offered is specified with the Package Information in Section 7 of this manual.

GENERAL TTL CIRCUIT CHARACTERISTICS

All TTL products are derived from a common NAND logic structure. The NAND circuit is actually five subcircuits as shown in Figure 1 and each performs a separate function. The input circuit (1) is an AND gate usually fabricated with a multi-emitter transistor which characterizes TTL technology. Many Schottky processed circuits have been designed with PNP or diode inputs in order to optimize the speed/power performance of the circuits.

NAND Gate Example

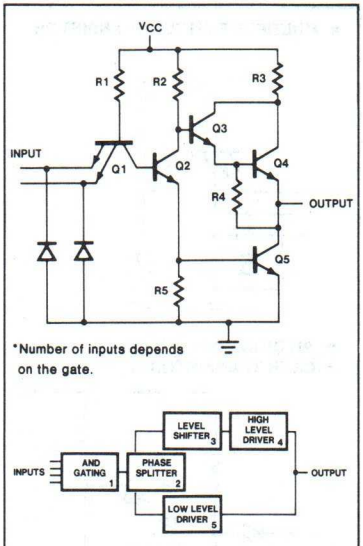


Figure 1

The phase splitter (2) provides the inversion and amplification in the circuit. It determines whether the outputs are active level HIGH or active level LOW. The level shifter (3) provides noise immunity between the HIGH and LOW output levels, and minimizes the possibility of having both HIGH level driver (4) and LOW level driver (5) on simultaneously.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	54/74	54S/74S	54LS/74LS
V_{CC} supply voltage, continuous (Note a)	7.0V	7.0V	7.0V
Input voltage, continuous (Notes a and b)	−0.5V to +5.5V	−0.5V to +5.5V	−0.5V to +7.0V[b]
Input current, continuous	−30mA to +5mA	−30mA to +5mA	−30mA to +1mA
Voltage applied to HIGH outputs (Note a)	−0.5V to V_{CC}	−0.5V to 7.0V	−0.5V to V_{CC}
Voltage applied to "off" Open Collector outputs (Notes a and c)	−0.5V to 7.0V	−0.5V to 7.0V	−0.5V to 7.0V
Current into LOW standard output, continuous	30mA	40mA	15mA
Current into LOW buffer output, continuous	80mA	100mA	50mA
Operating free air temperature range (Mil)	−55°C to +125°C		
Operating free air temperature range (Com'l)	0°C to +70°C		
Storage temperature range	−65°C to +150°C		

NOTES

a. Voltages are referenced to device ground terminal

b. The following LS device inputs are limited to 5.5V input breakdown: All inputs of LS181, Clock inputs of LS90, LS92, LS93, LS196, LS197, LS290, LS293, LS390, LS393 and LS490.

c. Some open collector devices are specially processed to handle higher output voltages of from 15V to 30V. The Absolute Maximum voltage for these devices is 10% over the specified V_{OUT} test condition.

TTL INPUT CONFIGURATIONS

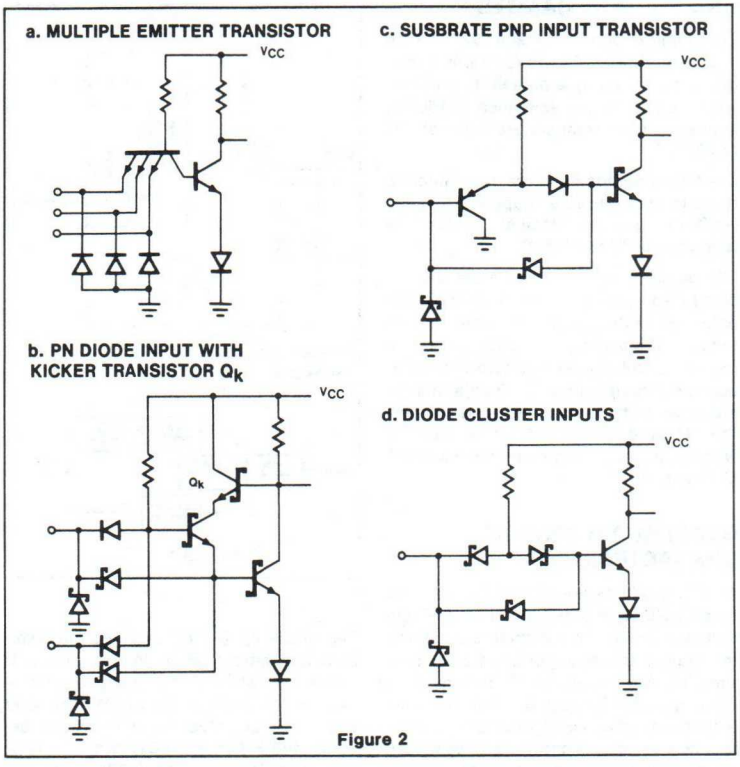


Figure 2

The level shifter (3) and HIGH level driver (4) combine to form an emitter follower circuit that tracks the voltage at the collector of the phase splitter. This circuit is usually designed to drive very heavy capacitive loads so that the initial rise time of the output is determined primarily by the rise time at the phase splitter collector. The LOW level driver (5) is usually a saturating transistor for the gold doped process devices, or a Schottky diode clamped transistor for the Schottky processed devices. These output transistors are designed to sink the rated fan-out current which characterizes the various TTL families.

Input Circuits

The input circuits as described above are basically AND gate configurations designed with multiple-emitter NPN transistors (MET), substrate PNP transistors, or various junction and Schottky diodes as shown in Figure 2. All of the circuit configurations have very high impedance in the HIGH state. When the input votlage is above the circuit threshold voltage, all of the inputs act like reversed biased diodes. The MET transistors are actually operated in the inverse mode, but the gain is so low there is very little current flowing into the devices.

The LOW level input impedance of the MET and diode inputs is determined by the internal pull-up resistor. This resistor is nominally 2KΩ for 54S/74S inputs, and it is 16KΩ to 20KΩ for the 54LS/74LS inputs. Some 54LS/74LS buffer devices have substrate PNP inputs which exhibit very high impedance at both HIGH and LOW input logic levels. This is used to minimize the input load factor and produce better output drive and performance.

The inputs to all Signetics TTL devices have clamp diodes to ground to minimize negative ringing effects. These diodes are designed to operate in the ac mode and cannot handle heavy dc currents for long periods.

Output Circuits

The output circuit configurations used for the TTL products in this manual are shown in Figure 3. The basic advantages and disadvantages of each configuration are given for reference. The different circuits are used to optimize the functional and performance requirements of the various devices, and are not necessarily restricted to individual TTL families. The pull-down circuit (not shown) on the base of the LOW level driver is usually a resistor which provides a means of turning off the output transistor. The majority of the 54S/74S and 54LS/74LS devices use a resistor-transistor network which acts to square-up the V_{IN}-V_{OUT} transfer characteristics of the device.

A resistive pull-up can be added to any TTL output circuit increasing V_{OH} to almost V_{CC}, but only circuits "c," "d," and "e" can be pulled higher than V_{CC}, e.g., to +7.0V for driving MOS circuits. Configurations "a" and "b" have a diode associated with the resistor at the output which clamps the output one diode drop above V_{CC}. This is an important consideration in large systems where sections might be powered down (V_{CC} = 0). In this state, the outputs of circuits "a" and "b" represent a very low impedance at a fairly low voltage (<1.0V), while the outputs of circuits "c," "d," and "e" represent a high impedance and thus a logic HIGH, more appropriate for isolation from the rest of the system.

The output impedance of a typical TTL device in both the LOW and HIGH state is shown in Figure 4. In the LOW state, the output impedance is determined by a saturated transistor (about 8Ω to 10Ω). However, at very high sinking current, especially at low temperature, the output device is not able to stay in saturation and the output impedance rises as shown.

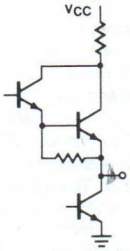
When switching from the LOW to the HIGH state, the totem-pole output structure provides a low output impedance capable of rapidly charging capacitive loads. However, charge and discharge currents must also flow through the V_{CC} and the ground distribution networks. The V_{CC} and ground lines should therefore be short and adequately decoupled.

3-State Outputs

Some of the buffers and registers have 3-state outputs designed for "busing." This type of output electrically performs as a totem-pole output with the additional feature that the output may be disabled, neither sinking nor sourcing current. The 3-state outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from

TTL OUTPUT CONFIGURATIONS

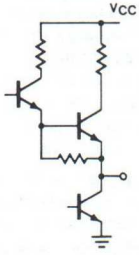
a. DARLINGTON



ADVANTAGE:
- High ac drive capability
- $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$
- Small size (transistors share one common isolation)

DISADVANTAGE:
- Output cannot be pulled higher than one diode drop above V_{CC}

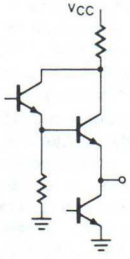
b. 2-STAGE EMITTER FOLLOWER ("DARLINGTON SPLIT")



ADVANTAGE:
- High ac drive capability
- $V_{OH} = V_{CC} - V_{BE}$ at $I_O = 0$

DISADVANTAGE:
- Larger than circuit A
- Output cannot be pulled higher than one diode drop above V_{CC}

c. DARLINGTON WITH RESISTOR TO GROUND



ADVANTAGE:
- High ac drive capability
- Lower $V_{OH} = (V_{CC} - 2\ V_{BE})$ increases speed
- Outputs can be pulled higher than V_{CC}

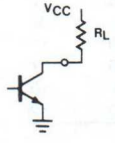
DISADVANTAGE:
- Higher dissipation
- Lower noise immunity in the HIGH state

d. TRANSISTOR—DIODE

ADVANTAGE:
- Lowest power consumption
- Small size
- Outputs can be pulled higher than VCC

DISADVANTAGE:
- Less ac drive capability

e. OPEN COLLECTOR



ADVANTAGE:
- Bussable, allows collector ANDing (Wired-OR)

DISADVANTAGE:
- High output impedance in the HIGH state
- Slow, especially with capacitive loading
- Requires additional resistor

Figure 3

TYPICAL INPUT/OUTPUT CHARACTERISTICS

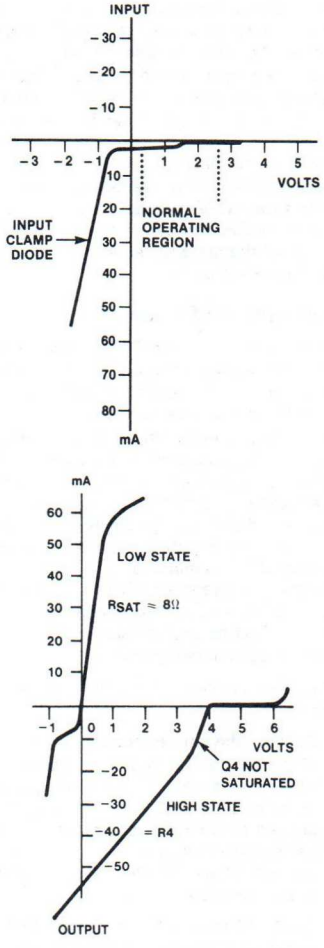


FIGURE 4

excessive power dissipation, only one 3-state output should be active at any time.

DESIGN CONSIDERATIONS

The properties of high speed TTL logic circuits dictate that some care be used in the design and layout of a system. Some general "design considerations" are included in this section. This is not intended to be a thorough guideline for designing TTL systems, but a reference for some of the constraints and techniques to be considered when designing the system.

Clamp Diode Effect on Negative Input Voltages

All Signetics TTL circuits are provided with clamp diodes on the device inputs to minimize negative ringing effects. These diodes should not be used to clamp negative dc voltages or long duration negative pulses especially for 54LS/74LS product. If the input voltage of an LS device is taken more than 0.5 volts negative (referenced to the device ground terminal) for more than 0.5 micro-seconds, it is possible to activate a parasitic circuit component which can cause the HIGH level output of that gate to degrade sufficiently to cause a logic error.

Disposition of Unused Inputs

Electrically open inputs degrade ac noise immunity as well as the switching speed of a circuit. To optimize performance, each input must be connected to a low impedance source. Unused active HIGH NOR or OR inputs must be returned to ground or a LOW level output. Unused active HIGH NAND or AND inputs should be maintained at a voltage greater than 2.7V, but not exceeding the Absolute Maximum Rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times.

Possible ways of handling unused inputs are:

1. Connect the unused active LOW inputs of the TTL devices to ground. The active HIGH inputs should be tied through a resistor of from 1K to 10KΩ to V_{CC}. The unused active HIGH LS inputs can be tied directly to V_{CC}, as long as the leads are very short and the supply is adequately decoupled.
2. Connect the unused HIGH input to the output of an unused gate that is forced HIGH.
3. Tie unused NAND or AND inputs (multi-emitter inputs) of non-LS devices to a used input of the same gate, provided the HIGH level fan out of the driving circuit is not exceeded. Note that the LOW level fan out is not increased by this connection because the inputs share a common base pull-up resistor.

NOTE
For 54LS/74LS devices do *not* connect multiple inputs of a common gate together. This would increase the input coupling capacitance and reduce the ac noise immunity.

Unused Gates

It is recommended that the outputs of unused gates be forced HIGH by tying a NAND gate input or all NOR gate inputs to ground. This lowers the power dissipation and supplies a logic HIGH at the gate output which can be used at unused inputs to other gates.

Increasing Fan Out

To increase fan out, inputs and outputs of gates on the same package may be paralleled. It is advisable to limit the gates being paralleled to those in a single package to avoid large transient supply currents due to different switching times of the gates. This is not detrimental to the devices, but could cause logic problems if the gates are being used as clock drivers.

Isolation Diodes

NEVER REVERSE THE V_{CC} AND GROUND POTENTIALS. Catastrophic failure can occur if more than 100mA is conducted through a forward biased substrate (isolation) diode.

Input Loading and Output Drive Characteristics

The logic levels of all the TTL products are fully compatible with each other. However, the inputs loading and output drive characteristics of each of these families is different and must be taken into consideration when mixing the TTL families in a system. Table I shows the relative drive capabilities of each family for the Commercial temperature and voltage ranges. For Military ranges the 74LS and 74L drive capabilities must be cut in half. You will note that the 74LS Buffers have three times the drive capability of the standard 74LS devices; in fact, they can drive more loads than any other non-buffer TTL device.

Mixing TTL Families

Most TTL families are intended to be used together, but this cannot be done indiscriminately. Each family of TTL devices has unique input and output characteristics optimized to get the desired speed or power features. Fast devices like 54S/74S are designed with relatively low input and output impedances. The speed of these devices is determined primarily by fast rise and fall times internally as well as at the input and output nodes. These fast transitions cause noise of various types in the system. Power and ground line noise is generated by the large currents needed to charge and discharge the circuit and load capacitances during the switching transitions. Signal line noise is generated by the fast output transitions and the relatively low output impedances, which tend to increase reflections.

The noise generated by these 54S/74S devices can only be tolerated in systems designed with very short signal leads, elaborate ground planes, and good, well decoupled power distribution networks. Mixing the slower TTL families like 54/74 and 54LS/74LS with the higher speed families is also possible but must be done with caution. The slower speed families are more susceptible to induced noise than the higher speed families due to their higher input and output impedances. The low power Schottky 54LS/74LS family is especially sensitive to induced noise and must be isolated as much as possible from the 54S/74S devices. Separate or isolated power and ground systems are recommended, and the LS input signal lines should not run adjacent to lines driven by 54S/74S devices.

DRIVING DEVICE	NUMBER OF LOADS DRIVEN						
	74LS	74	74H	74L	74S	8200 AND 9300	82S00
74LS	20	5	4	40	4	5	20
*74LS Buffers	60	15	12	120	12	15	60
74	40	10	8	80	8	10	40
74 Buffers	60	30	24	120	24	30	120
74H	50	12	10	100	10	12	50
74H Buffers	75	37	30	150	30	37	150
74L	9	2	1	20	1	2	9
74S	50	12	10	100	10	12	50
74S Buffers	150	37	30	150	30	37	150
8200 & 9300	40	10	8	80	8	10	40
82S00	50	12	10	100	10	12	50

*The 74LS Buffers include 3-State outputs except LS253 & LS670

Mixing 54/74 and 54LS/74LS is less restrictive, and the overall system design need not be so elaborate. Standard two sided PC boards can be used with good, well decoupled power and ground grid systems. The signal transitions are slower and therefore generate less noise. However, good high speed design techniques are still required, especially when working with counters, registers, or other devices with memory.

Clock Pulse Requirements

Most TTL flip-flop circuits are master-slave devices which makes their clock inputs level sensitive. This is an improvement over ac coupled clock inputs, but it does not make the devices fully insensitive to clock edge rates. The dc level at which the data in the master (input section) is transferred to the slave (output section) is the normal threshold voltage for the devices. For most Signetics TTL devices this level is 1.4V at 25°C, and it changes at a rate of about −4mV/°C.

When the clock input reaches the threshold voltage, the internal gates and the changing outputs start to dump current into the ground lead of the device. If there are enough internal gates or loaded outputs changing at the same time, the chip ground reference level (and therefore the clock input reference level) can rise by as much as 500mV. This ground noise is the algebraic sum of the internal and external ground plane noise. If the clock input of a positive edge triggered device is at or near the threshold of the device during the ground noise transient period, it is quite possible for the internal device to receive multiple clock pulses.

For this reason the rise time on positive edge-triggered devices should be less than the nominal clock to output delay time measured between the 0.8V and 2.0V levels of the clock driver. This edge rate is obtainable from almost any Signetics TTL device of the same family, as long as it is driving no more than rated fan out and no more than 12 to 16 inches of line. When clock pulses are distributed on lines over 16 inches long, all of the clock inputs should be clustered at the receiving end of the line to avoid reflection problems at the driving end.

Special Note

Some of the Signetics Counters and registers have been designed with a special clock buffer that includes a small amount of hysteresis to minimize clock edge rate and noise problems. The LS160A, LS161A, LS162A, LS163A, LS364, and LS374 all have the special clock buffers to increase their tolerance of slow positive clock edges and heavy ground noise.

TTL OUTPUTS TIED TOGETHER

The only TTL outputs that are designed to be tied together are open collector and 3-state outputs. Standard TTL outputs should not be tied together unless their logic levels will always be the same; either all HIGH or all LOW. When connecting open collector or 3-state outputs together some general guidelines must be observed:

Open Collector

These devices must be used whenever two or more OR-tied outputs will be at opposite logic levels at the same time. These devices must have a pull-up resistor (or resistors) added between the OR-tie connector and V_{CC} to establish an active HIGH level. Only special high voltage buffers can be tied to a higher voltage than V_{CC}. The minimum and maximum size of the pull-up resistor is determined as follows:

$$R(Min) = \frac{V_{CC}(Max) - V_{OL}}{I_{OL} - N_2(I_{IL})}$$

$$R(Max) = \frac{V_{CC}(Min) - V_{OH}}{N_1(I_{OH}) + N_2(I_{IH})}$$

where: I_{OL} = Minimum I_{OL} guarantee or OR-tied elements.

$N_2(I_{IL})$ = Cumulative maximum input LOW current for all inputs tied to OR-tie connection.

$N_1(I_{OH})$ = Cumulative maximum output HIGH leakage current for all outputs tied to OR-tie connection.

$N_2(I_{IH})$ = Cumulative maximum input HIGH leakage current for all inputs tied to OR-tie connection.

If a resistor divider network is used to provide the HIGH level, the R(Max) must be decreased enough to provide the required (V_{OH}/R(pull-down)) current.

Minimum propagation delay results when the minimum value of external pull-up resistor is used in Load Circuit 1, Figure 5.

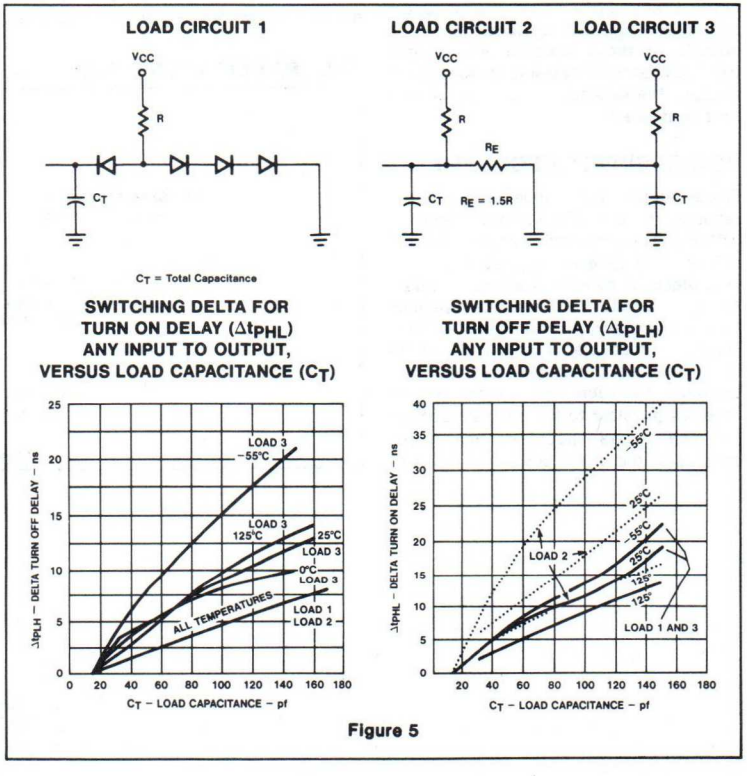


Figure 5

Diodes should be fast recovery 1N4376 or equivalent. External pull-up resistor Load Circuits 2 and 3 give progressively slower propagation delays.

3-STATE OUTPUTS

3-State Outputs are designed to be tied together, but they are not designed to be active simultaneously. In order to minimize noise and protect the outputs from excessive power dissipation, only one 3-state output should be active at any time. This generally requires that the Output Enable signals be non-overlapping. When TTL decoders are used to enable 3-state outputs, the decoder should be disabled while the address is being changed. Since all TTL decoder outputs are subject to decoding spikes, non-overlapping signals cannot normally be guaranteed when the address is changing.

Since most 3-state Output Enable signals are active LOW, shift registers or edge-triggered storage registers provide good Output Enable buffers. Shift registers with one circulating LOW bit, like the "164" or "194" are ideal for sequential enable signals. The "174" or "273" can be used to buffer enable signals from TTL decoders or microcode (ROM) devices. Since the outputs of these registers will change from LOW-to-HIGH faster than from HIGH-to-LOW, the selection of one device at a time is assured.

POWER SUPPLY DECOUPLING

Power supply capacitance decoupling is required for any TTL system. Generally 0.01μF per synchronously driven gate and at least 0.1μF for each 20 gates is required regardless of synchronization. Counters and shift registers are especially susceptible to power and ground line noise. They should be decoupled with a 0.1μF capacitor for each eight internal flip-flops, or one capacitor for each two devices put as close as possible to the devices. Buffers and line drivers should be heavily decoupled at the driver power pins, due to the large current transients needed to charge and discharge the lines.

On-Board Regulation

In most digital systems, there is a large current requirement, and the current supplied usually comes from a main supply. TTL logic tends to generate current spikes during switching due to the overlap in conduction of both upper and lower transistors, thus creating V_{CC} noise. An on-board regulator would not only regulate the power supplied ot the circuits on-board, but also would isolate the noise otherwise propagated to the reset of the system. Systems designed using this technique would not need tight regulation on the main power supply.

LINE DRIVING AND RECEIVING

Open wire connections between TTL circuits should not be bundled, tied, or routed together. Instead, point-to-point wiring should be used, preferably above a ground plane which reduces coupling between conductors.

Single line wire interconnections should not exceed two feet; for wires longer than 15 inches, a ground plane is essential to provide adequate system performance. Over 2-foot twisted pairs or coaxial cable should be used. The characteristic impedance of an open wire over a ground plane is about 150Ω, while for twisted pairs of #26 wire the impedance is about 120Ω. For added protection against crosstalk, coaxial cables can be used but coaxial cables having very low characteristic impedances are difficult to drive. For best performance, coaxial cables with a characteristic impedance R_O of 100Ω should be used. Resistive pull-ups at the receiving end can be used to increase noise margins. If reflection effects are unacceptable, the line must be terminated in its characteristic impedance. One method is shown in Figure 6 where the output of the line is tied to V_{CC} through a resistor equivalent to the characteristic impedance of the line. Therefore, R_O is fairly small, and the driving gate must sink the current through it in addition to the current from the inputs being driven. Terminating the line in a voltage divider with two resistors, each twice the line impedance, reduces the extra sink current by 50%. It is preferable to dedicate gates solely for line driving if the line length is in excess of five feet.

TTL DRIVING TWISTED PAIR

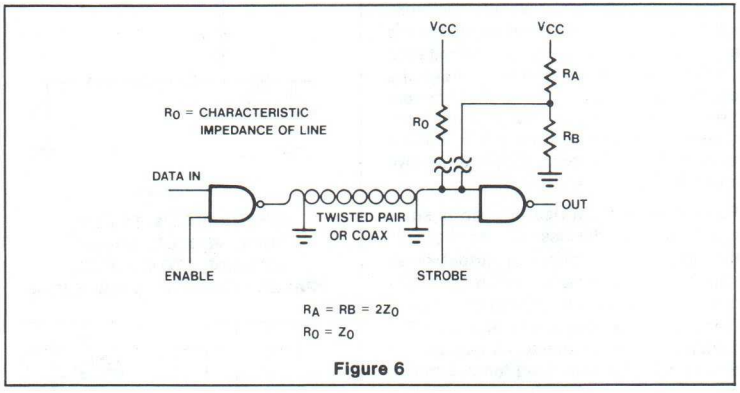


Figure 6

DC SYMBOLS AND DEFINITIONS

Voltages - All voltages are referenced to ground. Negative voltage limits are specified as absolute values (i.e., −10V is greater than −1.0V).

V_{CC}	**Supply voltage:** The range of power supply voltage over which the device is guaranteed to operate within the specified limits.
V_{CD}(Max)	**Input clamp diode voltage:** The most negative voltage at an input when the specified current is forced out of that input terminal. This parameter guarantees the integrity of the input diode intended to clamp negative ringing at the input terminal.
V_{IH}	**Input HIGH voltage:** The range of input voltages recognized by the device as a logic HIGH.
V_{IH}(Min)	**Minimum input HIGH voltage:** This value is the guaranteed input HIGH threshold for the device. The minimum allowed input HIGH in a logic system.
V_{IL}	**Input LOW voltage:** The range of input voltages recognized by the device as a logic LOW.
V_{IL}(Max)	**Maximum input LOW voltage:** This value is the guaranteed input LOW threshold for the device. The maximum allowed input LOW in a logic system.
V_M	**Measurement voltage:** The reference voltage level on ac waveforms for determining ac performance. Usually specified as 1.5V for most TTL families, but 1.3V for the Low Power Schottky 54LS/74LS family.
V_{OH}(Min	**Output HIGH voltage:** The minimum guaranteed HIGH voltage at an output terminal for the specified output current I_{OH} and at the minimum V_{CC} value.
V_{OL}(Max	**Output LOW voltage:** The maximum guaranteed LOW voltage at an output terminal sinking the specified load current I_{OL}.
V_{T+}	**Positive-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition rises from below V_{T-}(Min).
V_{T-}	**Negative-going threshold voltage:** The input voltage of a variable threshold device which causes operation according to specification as the input transition falls from above V_{T+}(Max).

Currents—Positive current is defined as conventional current flow into a device. Negative current is defined as conventional current flow out of a device. All current limits are specified as absolute values.

I_{CC}	**Supply current:** The current flowing into the V_{CC} supply terminal of the circuit with specified input conditions and open outputs. Input conditions are chosen to guarantee worst case operation unless specified.
I_I	**Input leakage current:** The current flowing into an input when the maximum allowed voltage is applied to the input. This parameter guarantees the minimum breakdown voltage for the input.
I_{IH}	**Input HIGH current:** The current flowing into an input when a specified HIGH level voltage is applied to that input.
I_{IL}	**Input LOW current:** The current flowing out of an input when a specified LOW level voltage is applied to that input.
I_{OH}	**Output HIGH current:** The leakage current flowing into a turned off open collector output with a specified HIGH output voltage applied. For devices with a pull-up circuit, the I_{OH} is the current flowing out of an output which is in the HIGH state.
I_{OL}	**Output LOW current:** The current flowing into an output which is in the LOW state.
I_{OS}	**Output short-circuit current:** The current flowing out of an output which is in the HIGH state when that output is short circuit to ground.
I_{OZH}	**Output off current HIGH:** The current flowing into a disabled 3-state output with a specified HIGH output voltage applied.
I_{OZL}	**Output off current LOW:** The current flowing out of a disabled 3-state output with a specified LOW output voltage applied.

AC SWITCHING PARAMETERS AND DEFINITIONS

f_{MAX}	**The maximum clock frequency:** The maximum input frequency at a clock input for predictable performance. Above this frequency the device may cease to function.
t_{PLH}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined LOW level to the defined HIGH level.
t_{PHL}	**Propagation delay time:** The time between the specified reference points on the input and output waveforms with the output changing from the defined HIGH level to the defined LOW level.
t_{PHZ}	**Output disable time from HIGH level of a 3-state output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the HIGH level to a high impedance "off" state.
t_{PLZ}	**Output disable time from LOW level of a 3-state output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from the LOW level to a high impedance "off" state.
t_{PZH}	**Output enable time to a HIGH level of a 3-state output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the HIGH level.
t_{PZL}	**Output enable time to a LOW level of a 3-state output:** The delay time between the specified reference points on the input and output voltage waveforms with the 3-state output changing from a high impedance "off" state to the LOW level.
t_h	**Hold time:** The interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its continued recognition. A negative hold time indicates that the correct logic level may be released prior to the active transition of the timing pulse and still be recognized.
t_s	**Setup time:** The interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure its recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.
t_W	**Pulse width:** The time between the specified reference points on the leading and trailing edges of a pulse.
t_{rec}	**Recovery time:** The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

Section 3
TTL Data Sheets

Quad Two-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7400	9ns	8mA
74LS00	9.5ns	1.6mA
74S00	3ns	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7400N • N74LS00N N74S00N	
Ceramic DIP	N7400F • N74LS00F N74S00F	S5400F • S54LS00F S54S00F
Flatpack		S5400W • S54LS00W S54S00W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

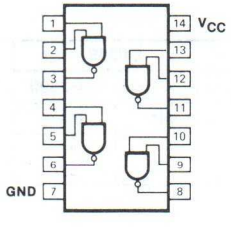
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

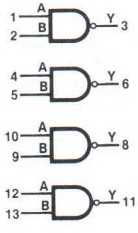
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

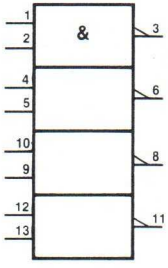
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



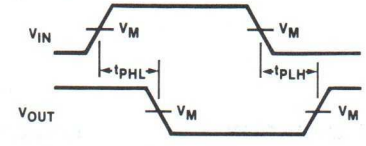
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7400			54/74LS00			54/74S00			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			4	8		0.8	1.6		10	16	mA
		I_{CCL} Outputs LOW			12	22		2.4	4.4		20	36	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

3

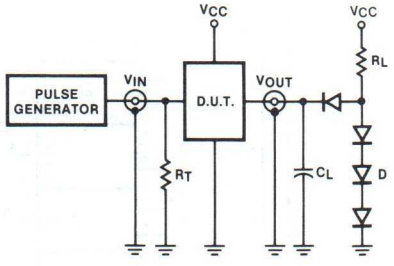
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

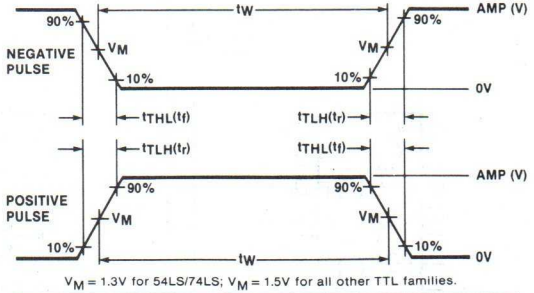
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS01	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS01N	
Ceramic DIP	N74LS01F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

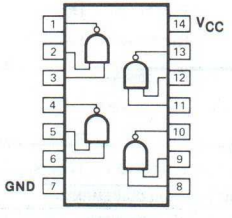
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

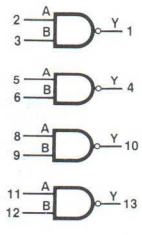
PINS	DESCRIPTION	54/74LS
A, B	Inputs	1LSul
Y	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4 mA I_{IL}.

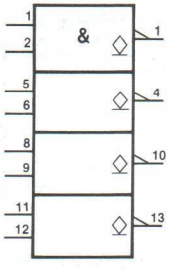
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

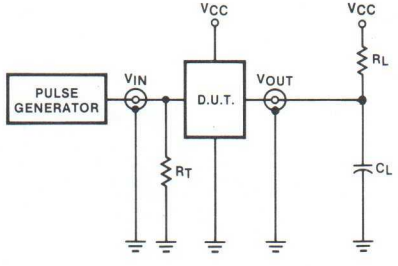
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

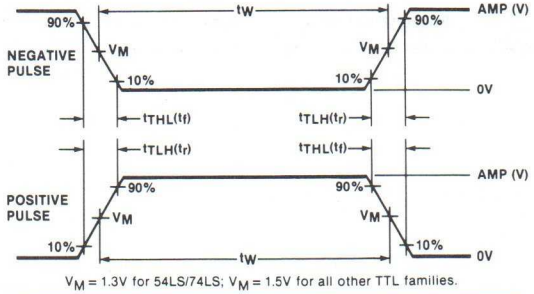
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

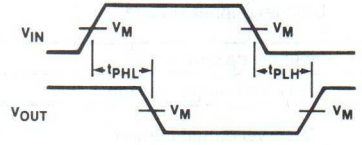
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS01 Min	54/74LS01 Typ[2]	54/74LS01 Max	UNIT
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		0.8	1.6	mA
			I_{CCL}	Outputs LOW		2.4	4.4	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ Min	54LS/74LS C_L = 15pF, R_L = 2kΩ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		32 28	ns

Quad Two-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7402	10ns	11mA
74LS02	10ns	2.2mA
74S02	3.5ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7402N • N74LS02N N74S02N	
Ceramic DIP	N7402F • N74LS02F N74S02F	S54S02F • S54LS02F
Flatpack		S54S02W • S54LS02W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

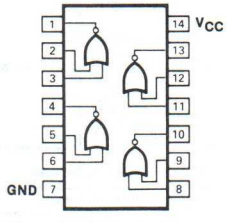
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

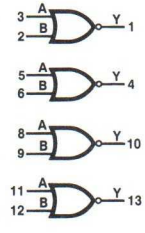
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

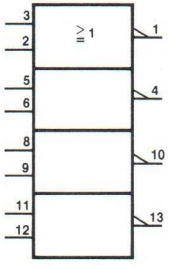
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

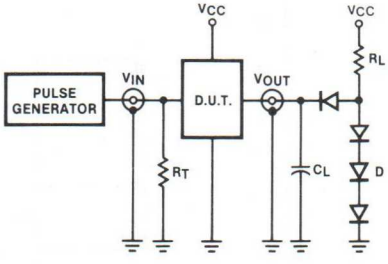
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

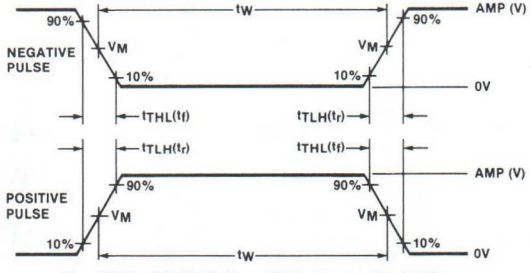
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

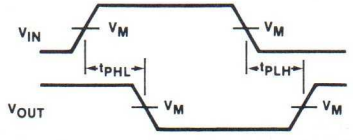
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7402			54/74LS02			54/74S02			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply Current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			8	16		1.6	3.2		17	29	mA
		I_{CCL} Outputs LOW			14	27		2.8	5.4		26	45	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		15 15		5.5 5.5	ns

Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7403	35ns (t_{PLH}) 8ns (t_{PHL})	8mA
74S03	5ns (t_{PLH}) 4.5ns (t_{PHL})	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7403N • N74S03N	
Ceramic DIP	N7403F • N74S03F	S5403F
Flatpack		S5403W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

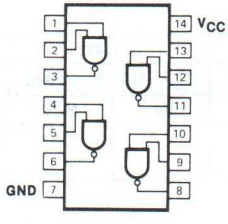
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

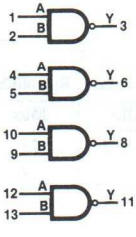
PINS	DESCRIPTION	54/74	54/74S
A, B	Inputs	1ul	1Sul
Y	Output	10ul	10Sul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

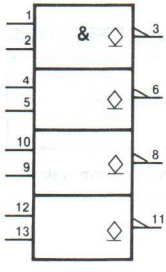
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54S	74	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

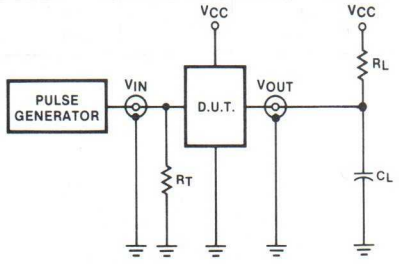
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5	V
I_{OL}	LOW-level output current	Mil			16			20	mA
		Com'l			16			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

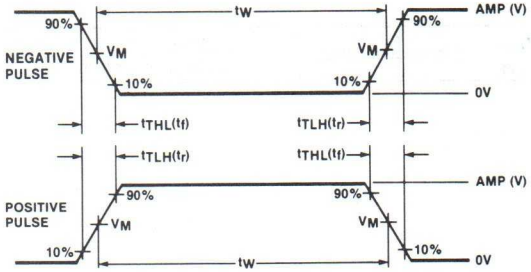
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

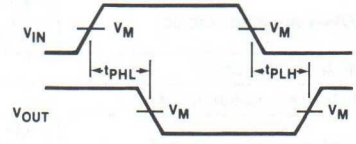
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7403			54/74S03			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					250			250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX		Mil		0.2	0.4			0.5	V
				Com'l		0.2	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0			1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6				mA
			V_I = 0.5V							– 2.0	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		4	8		6	13.2	mA
			I_{CCL}	Outputs LOW		12	22		20	36	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	For 54/7403 only, R_L = 4kΩ for t_{PLH}. Waveform 1		45 15		7.5 7.0	ns

INVERTERS 54/7404, LS04, S04

Hex Inverter

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7404	10ns	12mA
74LS04	9.5ns	2.4mA
74S04	3ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7404N • N74LS04N N74S04N	
Ceramic DIP	N7404F • N74LS04F N74S04F	S5404F • S54LS04F S54S04F
Flatpack		S5404W • S54LS04W S54S04W

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

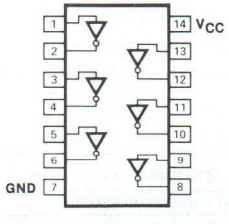
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

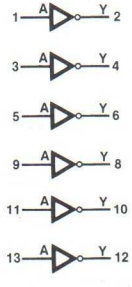
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

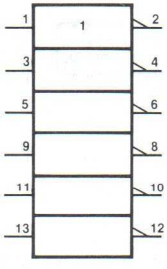
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

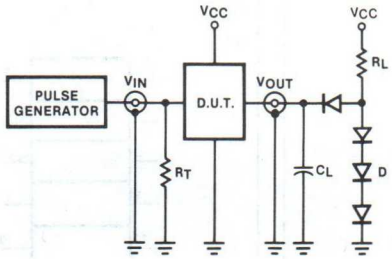
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

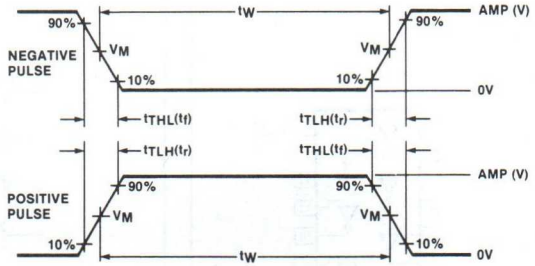
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

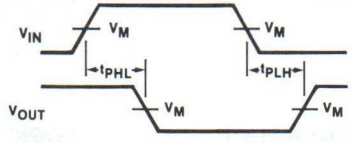
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7404			54/74LS04			54/74S04			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			6	12		1.2	2.4		15	24	mA
		I_{CCL} Outputs LOW			18	33		3.6	6.6		30	54	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		15 15		4.5 5.0	ns

INVERTERS 54/7405, LS05, S05

Hex Inverter (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7405	40ns (t_{PLH}) 8ns (t_{PHL})	12mA
74LS05	17ns (t_{PLH}) 15ns (t_{PHL})	2.4mA
74S05	5ns (t_{PLH}) 4.5ns (t_{PHL})	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7405N • N74LS05N N74S05N	
Ceramic DIP	N7405F • N74LS05F N74S05F	

FUNCTION TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

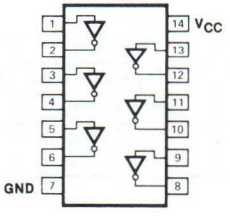
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

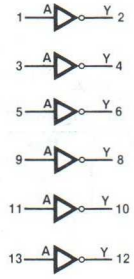
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A	Input	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

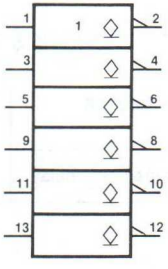
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

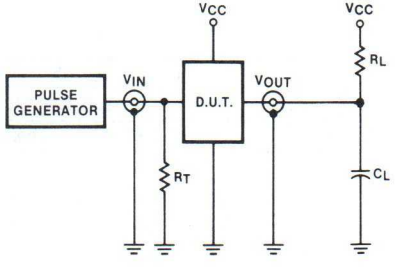
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5			5.5	V
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

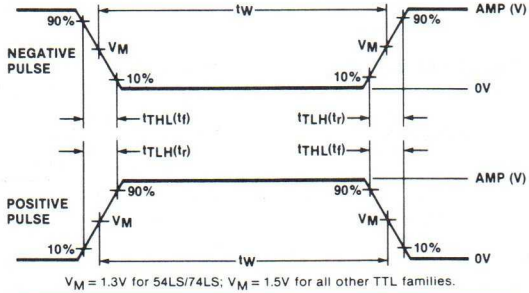
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

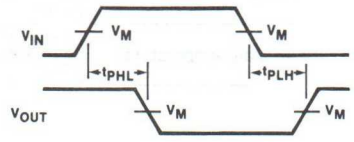
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7405			54/74LS05			54/74S05			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH} HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					250			100			250	μA
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.5			− 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				− 1.6			− 0.4				mA
		V_I = 0.5V										− 2.0	mA
I_{CC} Supply Current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			6	12		1.2	2.4		9	19.8	mA
		I_{CCL} Outputs LOW			18	33		3.6	6.6		30	54	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL} Propagation delay	For 54/7405 only, R_L = 4kΩ for t_{PLH}. Waveform 1		55 15		32 28		7.5 7.0	ns

'06 Hex Inverter Buffer/Driver (Open Collector)
'07 Hex Buffer/Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7406	10ns (t_{PLH}) 15ns (t_{PHL})	31mA
7407	6ns (t_{PLH}) 20ns (t_{PHL})	25mA

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7406N • N7407N	
Ceramic DIP	N7406F • N7407F	

FUNCTION TABLE

'06		'07	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
H	L	H	H
L	H	L	L

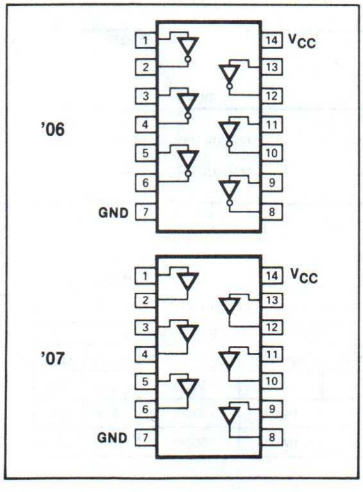
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

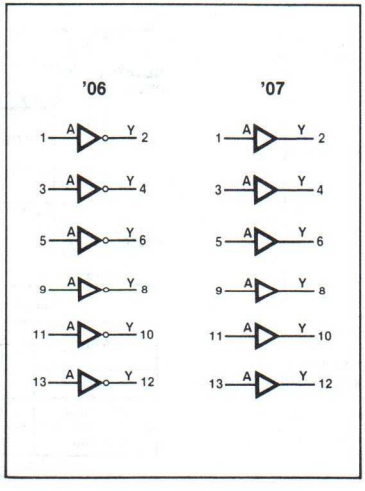
PINS	DESCRIPTION	54/74
A	Input	1ul
Y	Output	10ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

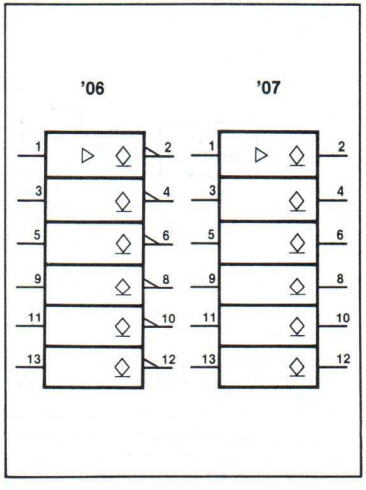
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

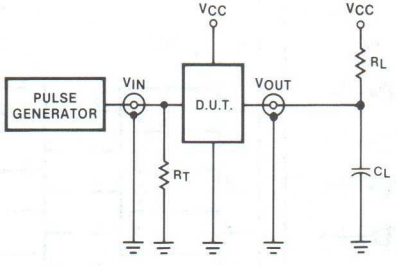
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +30	−0.5 to +30	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
V_{OH}	HIGH-level output voltage				30	V
I_{OL}	LOW-level output current	Mil			30	mA
		Com'l			40	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

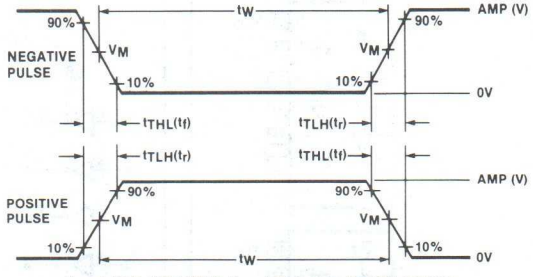
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

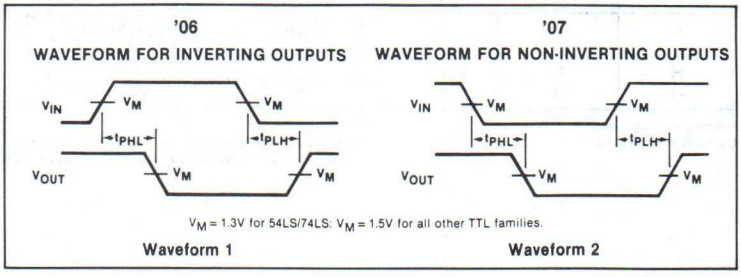
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/7406, 54/7407			UNIT
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 30V						250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 16mA					0.4	V
			I_{OL} = 30mA	Mil				0.7	V
			I_{OL} = 40mA	Com'l				0.7	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}						−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V						1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V						40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V						−1.6	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH	'06		30	48	mA
			I_{CCL}	Outputs LOW			32	51	mA
			I_{CCH}	Outputs HIGH	'07		29	41	mA
			I_{CCL}	Outputs LOW			21	30	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/7406 C_L = 15pF, R_L = 110Ω		54/7407 C_L = 15pF, R_L = 110Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '06 Waveform 2, '07		15 23		10 30	ns

GATES 54/7408, LS08, S08

Quad Two-Input AND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7408	15ns	16mA
74LS08	9ns	3.4mA
74S08	5ns	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7408N • N74LS08N N74S08N	
Ceramic DIP	N7408F • N74LS08F N74S08F	S54S08F • S54LS08F
Flatpack		S54S08W • S54LS08W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

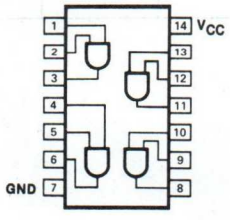
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

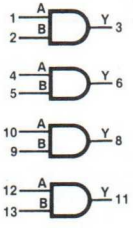
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

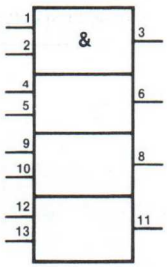
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

3

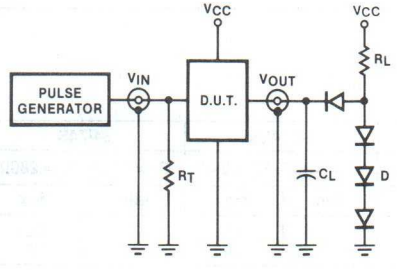
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

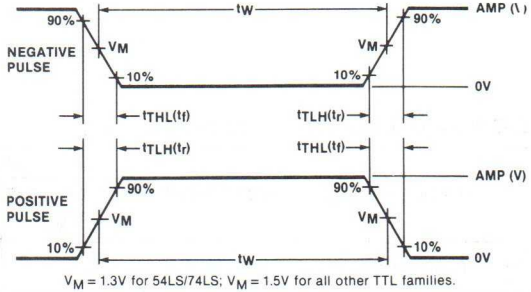
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

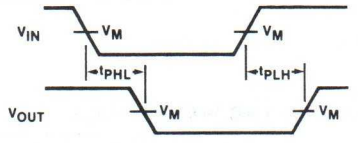
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7408			54/74LS08			54/74S08			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply Current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			11	21		2.4	4.8		18	32	mA
		I_{CCL} Outputs LOW			20	33		4.4	8.8		32	57	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS: V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		27 19		15 20		7.0 7.5	ns

Triple Three-Input NAND ('10), AND ('11) Gates

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7410	9ns	6mA
74LS10	10ns	1.2mA
74S10	3ns	12mA
7411	10ns	11mA
74LS11	9ns	2.6mA
74S11	5ns	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP '10	N7410N • N74LS10N N74S10N	
'11	N7411N • N74LS11N N74S11N	
Ceramic DIP '10	N7410F • N74LS10F N74S10F	S54S10F • S54LS10F
'11	N7411F • N74LS11F N74S11F	S5411F • S54S11F
Flatpack '10		S54S10W • S54LS10W
'11		S5411W • S54S11W

FUNCTION TABLE

INPUTS			OUTPUTS	
A	B	C	Y('10)	Y('11)
L	L	L	H	L
L	L	H	H	L
L	H	L	H	L
L	H	H	H	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

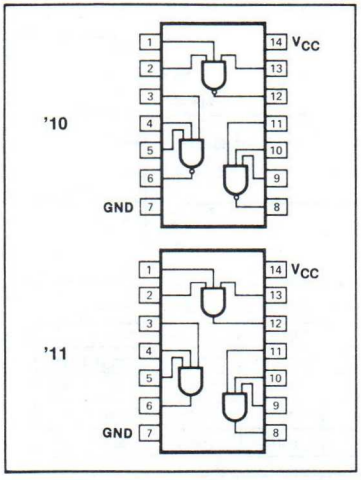
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

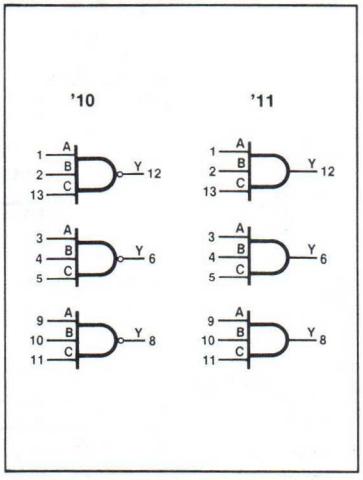
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A–C	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

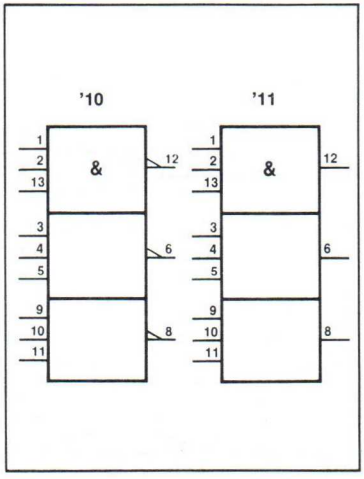
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

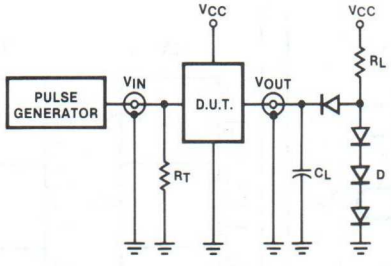
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current	'10			−400			−400			−1000	μA
		'11			−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

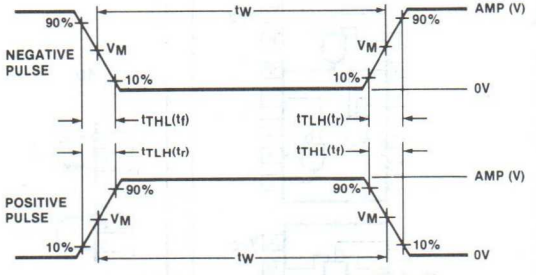
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

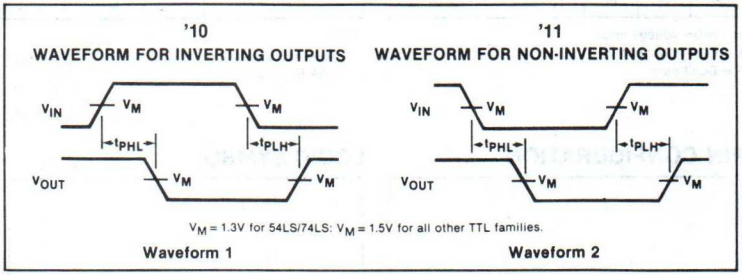
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7410, 11			54/74LS10, 11			54/74S10, 11			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	'10		3	6		0.6	1.2		7.5	12	mA
			I_{CCL} Outputs LOW			9	16.5		1.8	3.3		15	27	mA
			I_{CCH} Outputs HIGH	'11		6	12		1.8	3.6		13.5	24	mA
			I_{CCL} Outputs LOW			15	20		3.3	6.6		24	42	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '10		22 15		15 15		4.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '11		27 19		15 20		7.0 7.5	ns

GATES 54/7413, LS13

Dual 4-Input NAND Schmitt Trigger

DESCRIPTION

The '13 contains two 4-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 4-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transitions, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mV) is determined by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as three inputs remain at a more positive voltage than V_{T+MAX}, the gate will respond in the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7413	17ns	17mA
74LS13	17ns	3.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7413N • N74LS13N	
Ceramic DIP	N7413F • N74LS13F	S54LS13F
Flatpack		S54LS13W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

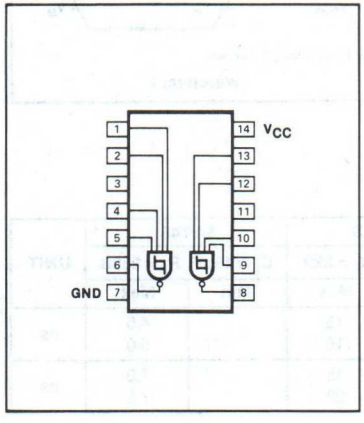
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

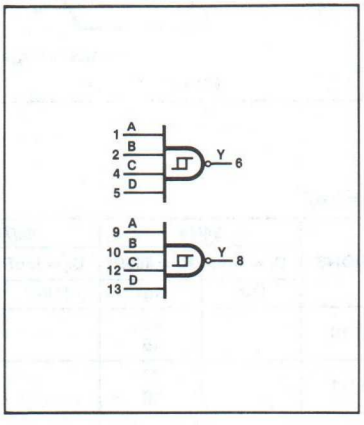
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}

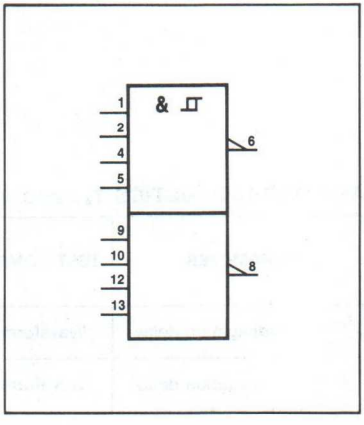
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

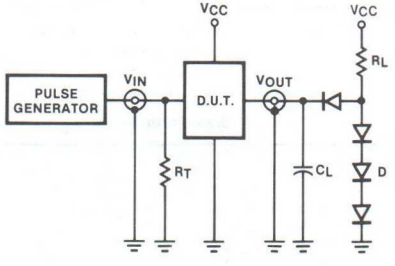
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

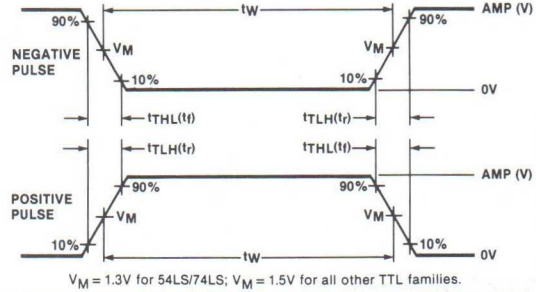
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

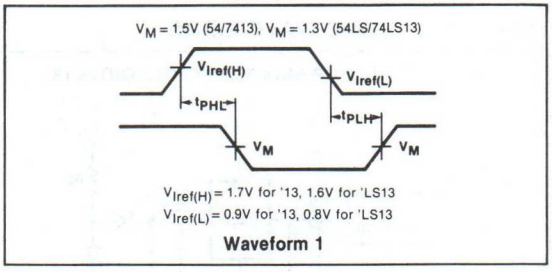
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7413			54/74LS13			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$				-0.65			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$				-0.85			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		14	23		2.9	6	mA
			I_{CCL}	Outputs LOW		20	32		4.1	7	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



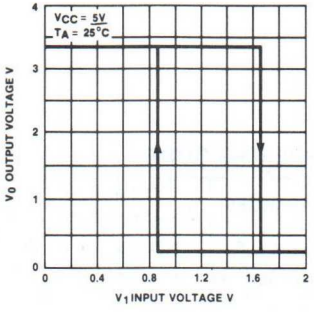
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

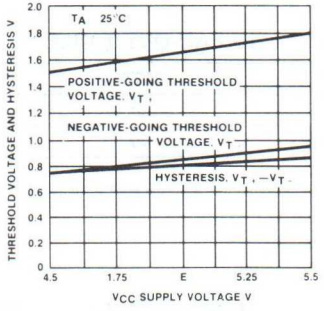
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		27 22		22 27	ns

TYPICAL CHARACTERISTICS

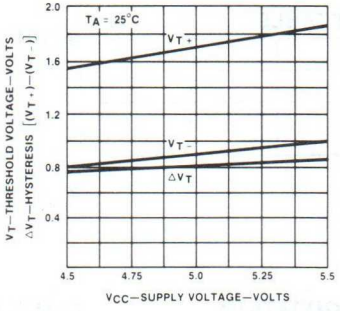
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT} TRANSFER FUNCTION



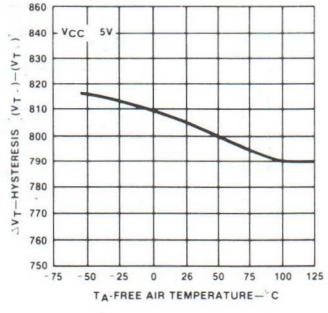
(54/74)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



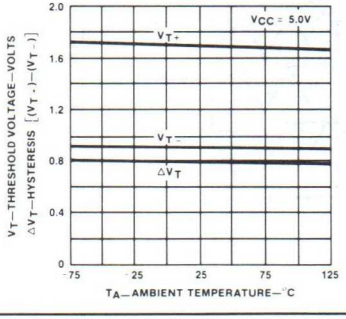
(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs AMBIENT TEMPERATURE



SCHMITT TRIGGERS 54/7414, LS14

Hex Inverter Schmitt Trigger

DESCRIPTION

The '14 contains six logic inverters which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional inverters.

Each circuit contains a Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input thresholds (typically 800mV) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7414	15ns	31mA
74LS14	15ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7414N • N74LS14N	
Ceramic DIP	N7414F • N74LS14F	S5414F • S54LS14F
Flatpack		S5414W • S54LS14W

FUNCTION TABLE

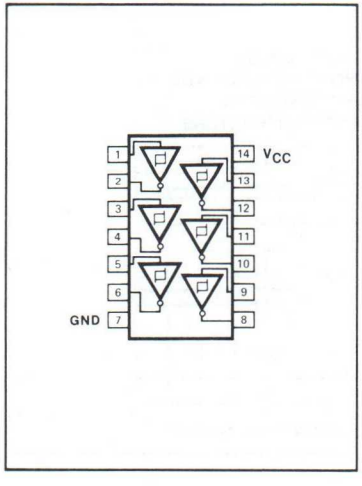
INPUT	OUTPUT
A	Y
0	1
1	0

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

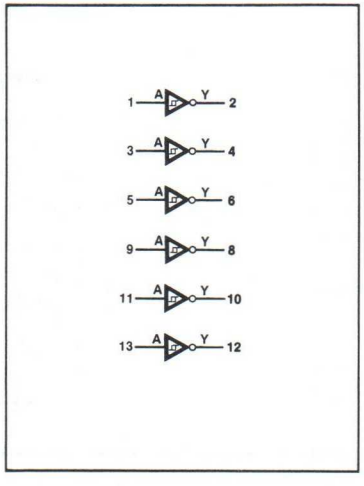
PINS	DESCRIPTION	54/74	54/74LS
A	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

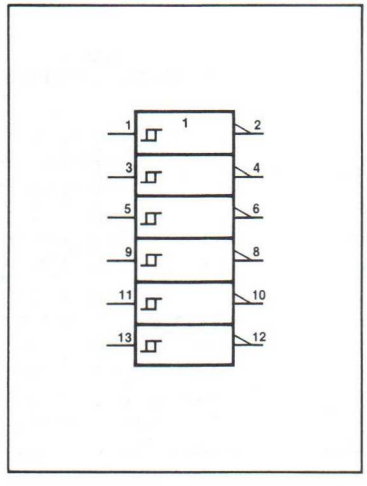
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

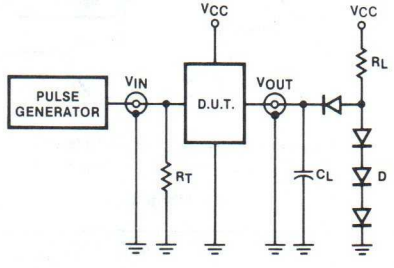
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

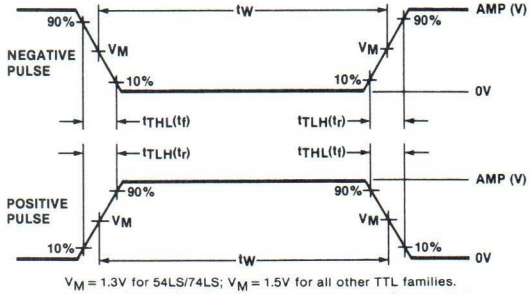
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

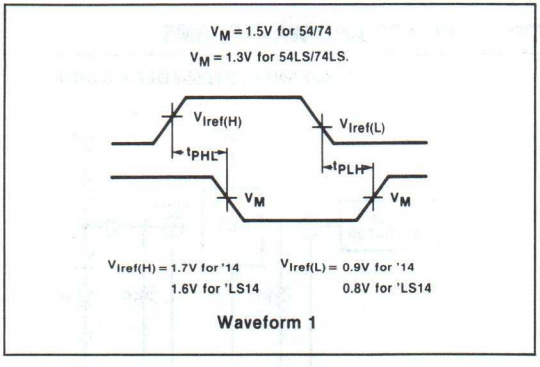
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7414			54/74LS14			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			I_{OL} = MAX	Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$				-0.43			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$				-0.56			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.2			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		22	36		8.6	16	mA
			I_{CCL}	Outputs LOW		39	60		12	21	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



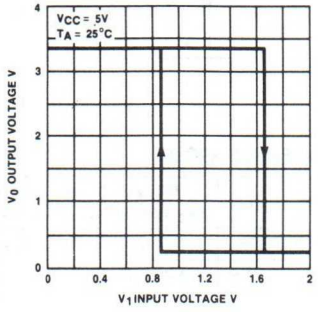
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

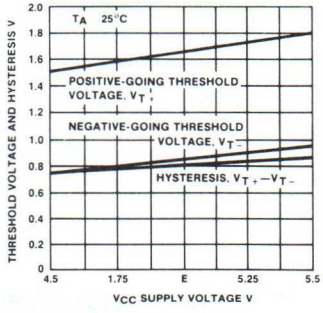
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22		22 22	ns

TYPICAL CHARACTERISTICS

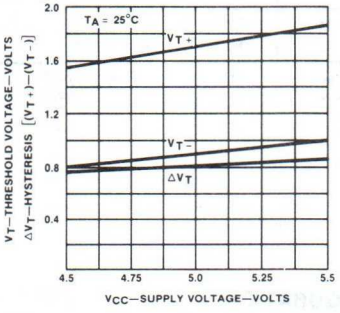
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT}
TRANSFER FUNCTION



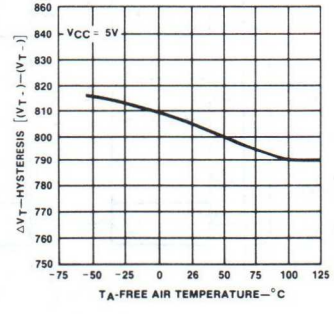
(54/74)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



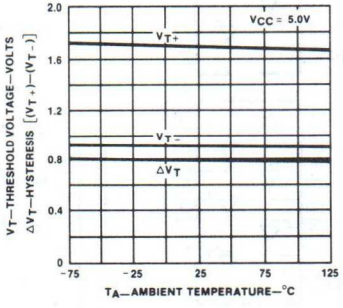
(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs AMBIENT TEMPERATURE



'16 Hex Inverter Buffer/Driver (Open Collector)
'17 Hex Buffer/Driver (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7416	10ns (t_{PLH}) 15ns (t_{PHL})	31mA
7417	6ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7416N • N7417N	
Ceramic DIP	N7416F • N7417F	

FUNCTION TABLE

'16		'17	
INPUT	OUTPUT	INPUT	OUTPUT
A	Y	A	Y
L	H	L	L
H	L	H	H

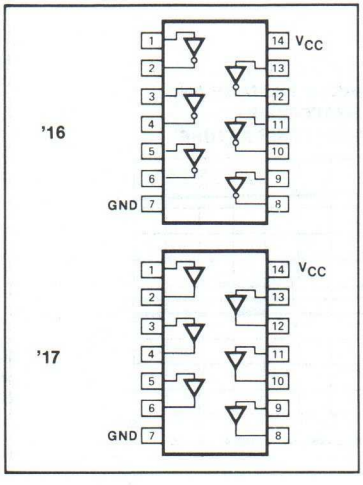
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

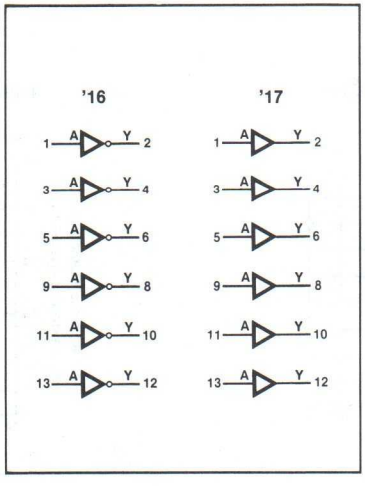
PINS	DESCRIPTION	54/74
A	Input	1ul
Y	Output	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

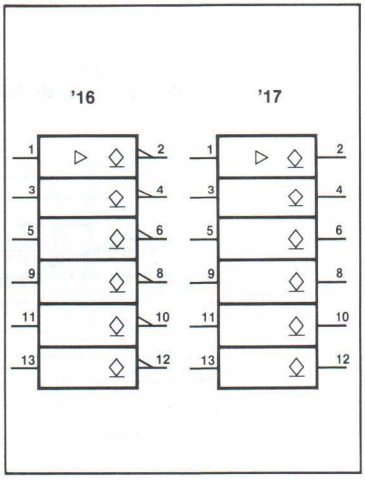
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +15	−0.5 to +15	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

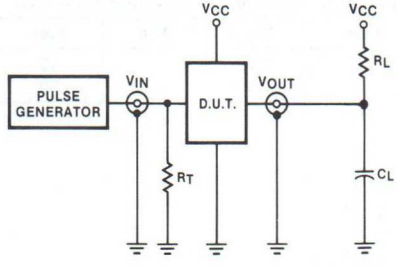
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
V_{OH}	HIGH-level output voltage				15	V
I_{OL}	LOW-level output current	Mil			30	mA
		Com'l			40	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

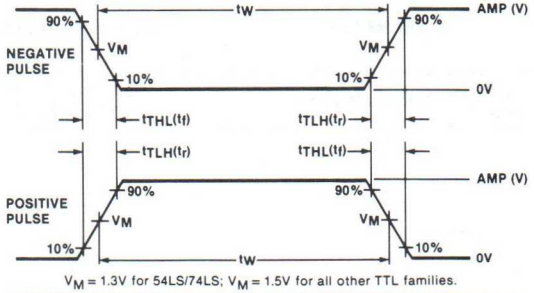
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

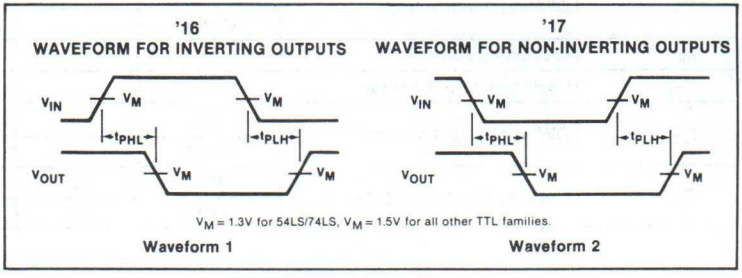
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/7416, 54/7417			UNIT
						Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 15V						250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 16mA					0.4	V
			I_{OL} = 30mA	Mil				0.7	V
			I_{OL} = 40mA	Com'l				0.7	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}						– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V						1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V						40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V						– 1.6	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH	'16		30	48	mA
			I_{CCL}	Outputs LOW			32	51	mA
			I_{CCH}	Outputs HIGH	'17		29	41	mA
			I_{CCL}	Outputs LOW			21	30	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/7416		54/7417		UNIT
			C_L = 15pF, R_L = 110Ω		C_L = 15pF, R_L = 110Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '16 Waveform 2, '17		15 23		10 30	ns

Dual Four-Input NAND ('20), AND ('21) Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7420	10ns	8mA
74LS20	10ns	0.8mA
74S20	3ns	8mA
7421	12ns	8mA
74LS21	9ns	1.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP '20	N7420N • N74LS20N N74S20N	
'21	N7421N • N74LS21N	
Ceramic DIP '20	N7420F • N74LS20F N74S20F	S5420F • S54LS20F S54S20F
'21	N7421F • N74LS21F	
Flatpack '20		S5420W • S54LS20W S54S20W

FUNCTION TABLE

INPUTS				OUTPUTS	
A	B	C	D	Y('20)	Y('21)
L	X	X	X	H	L
X	L	X	X	H	L
X	X	L	X	H	L
X	X	X	L	H	L
H	H	H	H	L	H

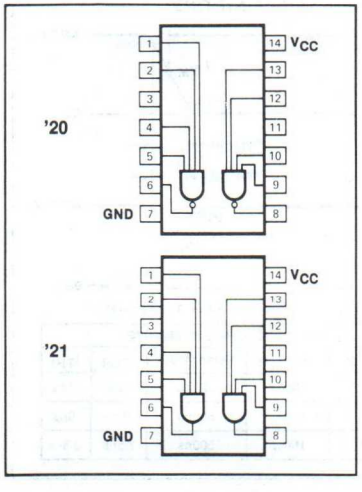
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

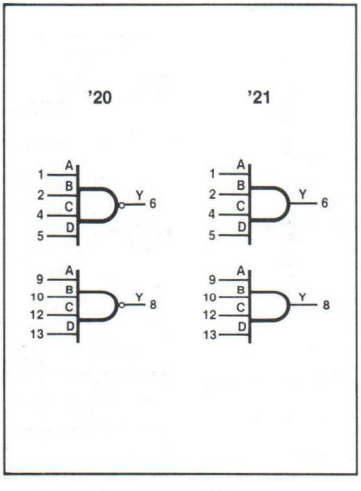
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A–D	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

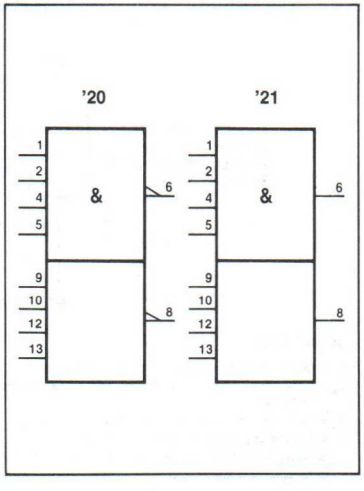
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

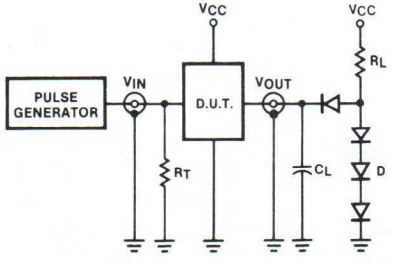
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current	'20			−400			−400			−1000	μA
		'21			−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

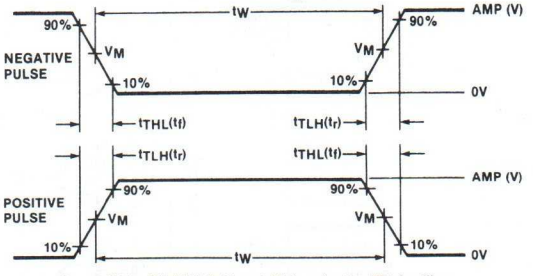
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

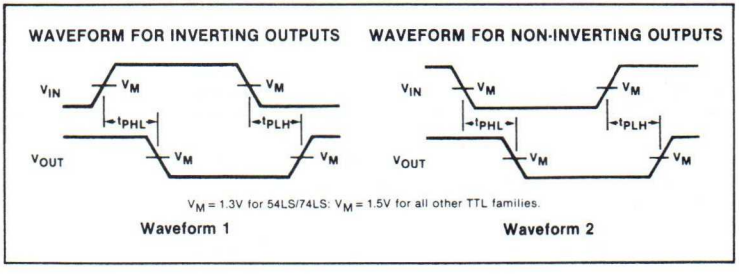
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7420, 21			54/74LS20, 21			54/74S20			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	'20		2	4		0.4	0.8		5	8	mA
			I_{CCL} Outputs LOW	'20		6	11		1.2	2.2		10	18	mA
			I_{CCH} Outputs HIGH	'21		6	8		1.2	2.4				mA
			I_{CCL} Outputs LOW	'21		11	13		2.2	4.4				mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '20		22 15		15 15		4.5 5.0	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '21		27 19		15 20			ns

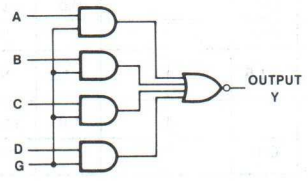
GATE 54/7425

Dual Four-Input NOR Gate With Strobe

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7425	9ns	9mA

LOGIC DIAGRAM

(EACH GATE)



ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7425N	
Ceramic DIP	N7425F	S5425F
Flatpack		S5425W

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
X	X	X	X	L	H
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	H	H

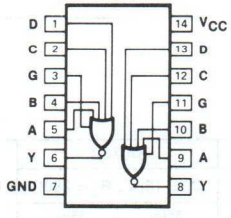
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

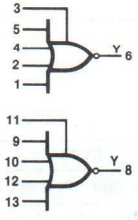
PINS	DESCRIPTION	54/74
A-D	Inputs	1ul
G	Input	4ul
Y	Output	10ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

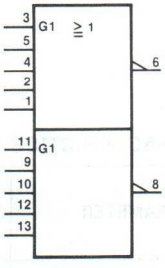
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

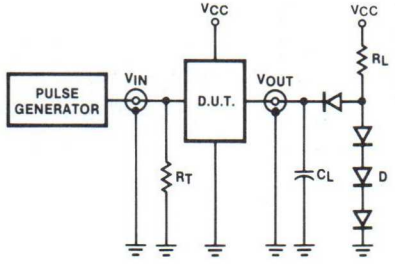
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

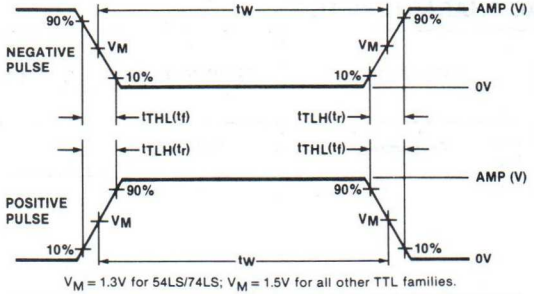
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

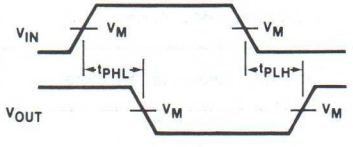
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/7425 Min	54/7425 Typ[2]	54/7425 Max	UNIT
V_{OH}	HIGH-level output votlage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	G input			160	μA
			Other inputs			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	G input			– 6.4	mA
			Other inputs			– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	– 20		– 55	mA
			Com'l	– 18		– 55	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		8	16	mA
			I_{CCL} Outputs LOW		10	19	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 15	ns

Quad Two-Input NAND Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7426	14ns	8mA
74LS26	16ns	1.6mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7426N • N74LS26N	
Ceramic DIP	N7426F • N74LS26F	S5426F

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

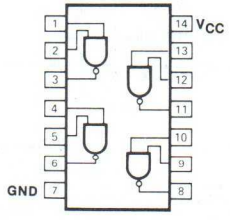
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

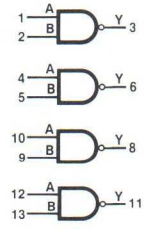
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

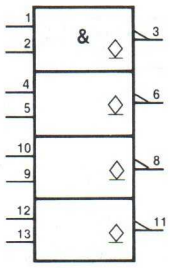
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

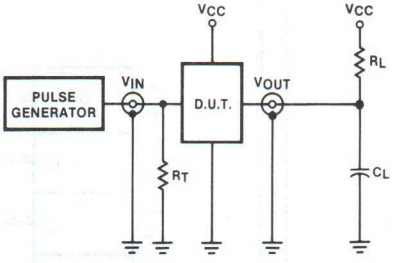
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +15	−0.5 to +15	−0.5 to +15	−0.5 to +15	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
V_{OH}	HIGH-level output voltage				15			15	V
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

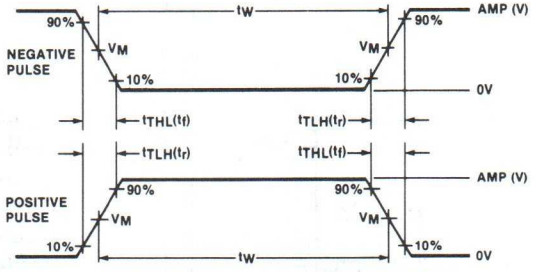
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

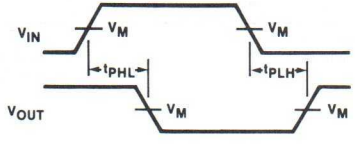
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7426			54/74LS26			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX	V_{OH} = 15V				1000			1000	μA
			V_{OH} = 12V				50			50	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		4	8		0.8	1.6	mA
			I_{CCL}	Outputs LOW		12	22		2.4	4.4	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 1kΩ		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		24 17		32 28	ns

Triple Three-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7427	9ns	13mA
74LS27	10ns	2.7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7427N • N74LS27N	
Ceramic DIP	N7427F • N74LS27F	

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

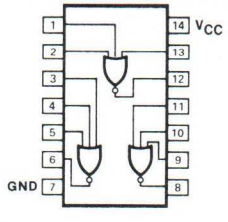
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

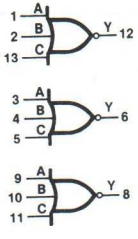
PINS	DESCRIPTION	54/74	54/74LS
A-C	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

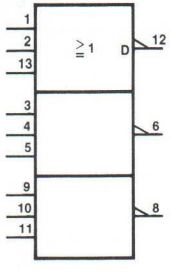
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to −5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

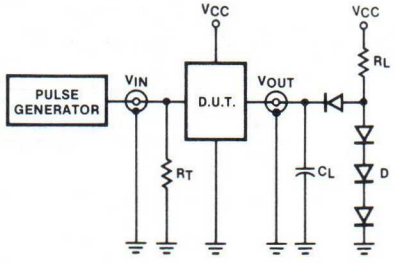
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

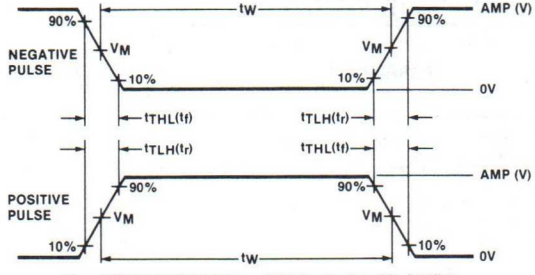
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

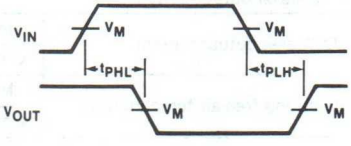
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7427			54/74LS27			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			10	16		2.0	4	mA
			I_{CCL} Outputs LOW			16	26		3.4	6.8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		15 11		15 15	ns

BUFFER 54/7428

Quad Two-Input NOR Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7428	7ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7428N	
Ceramic DIP	N7428F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

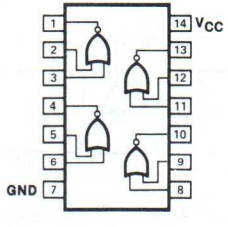
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

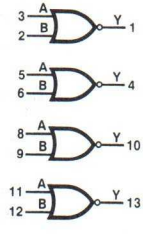
PINS	DESCRIPTION	54/74
A, B	Inputs	1ul
Y	Output	30ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

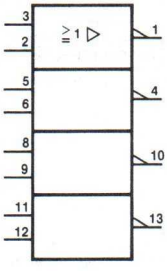
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

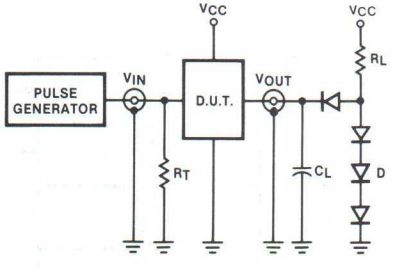
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−2400	μA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

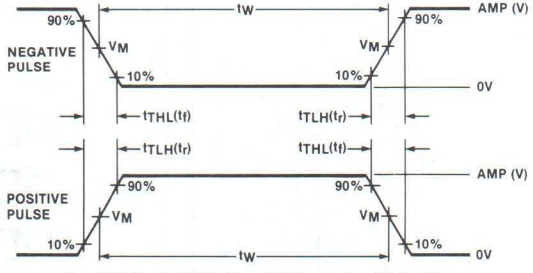
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

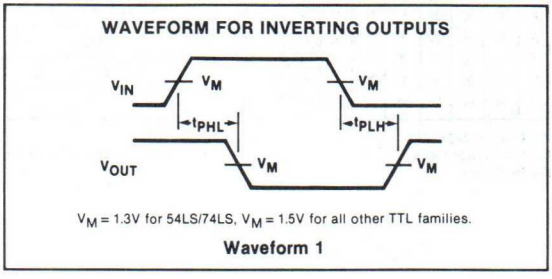
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/7428 Min	54/7428 Typ[2]	54/7428 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	– 70		– 180	mA
			Com'l	– 70		– 180	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		12	21	mA
			I_{CCL} Outputs LOW		33	57	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 R_L = 133Ω Min	54/74 R_L = 133Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 C_L = 50pF		9.0 12	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 C_L = 150pF		15 18	ns

Eight-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7430	11ns	2mA
74LS30	11ns	0.5mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7430N • N74LS30N	
Ceramic DIP	N7430F • N74LS30F	S54LS30F
Flatpack		S54LS30W

FUNCTION TABLE

INPUTS								OUTPUT
A	B	C	D	E	F	G	H	Y
L	X	X	X	X	X	X	X	H
X	L	X	X	X	X	X	X	H
X	X	L	X	X	X	X	X	H
X	X	X	L	X	X	X	X	H
X	X	X	X	L	X	X	X	H
X	X	X	X	X	L	X	X	H
X	X	X	X	X	X	L	X	H
X	X	X	X	X	X	X	L	H
H	H	H	H	H	H	H	H	L

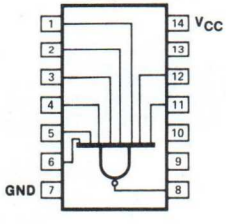
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

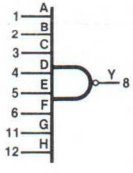
PINS	DESCRIPTION	54/74	54/74LS
A-H	Inputs	1ul	1LSul
Y	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

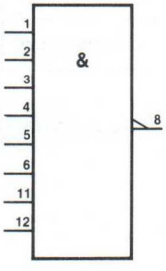
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

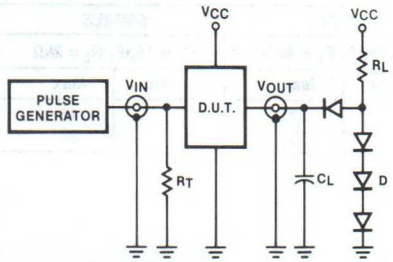
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

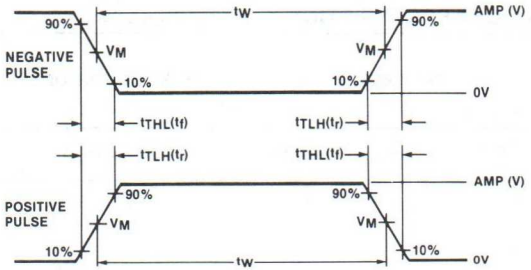
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

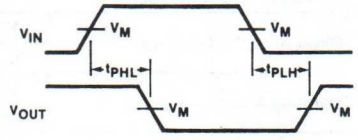
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7430			54/74LS30			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			1	2		0.35	0.5	mA
			I_{CCL} Outputs LOW			3	6		0.6	1.1	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 15		15 20	ns

Quad Two-Input OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7432	12ns	19mA
74LS32	14ns	4.0mA
74S32	4ns	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7432N • N74LS32N N74S32N	
Ceramic DIP	N7432F • N74LS32F N74S32F	S5432F • S54LS32F
Flatpack		S5432W • S54LS32W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

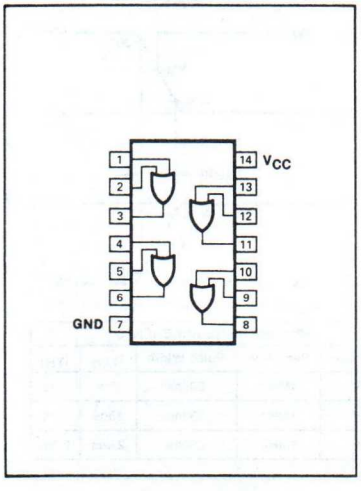
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

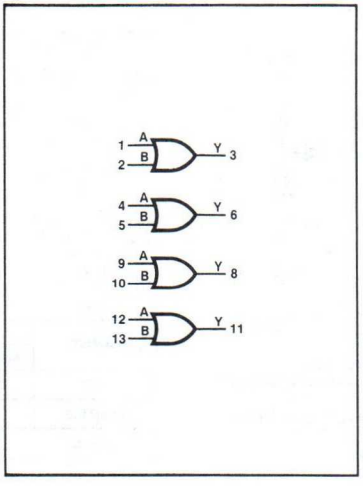
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

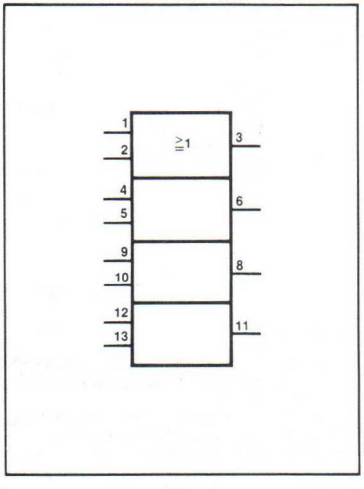
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

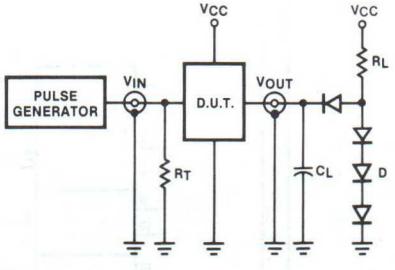
PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

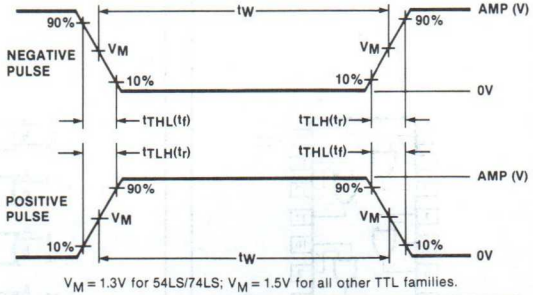
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

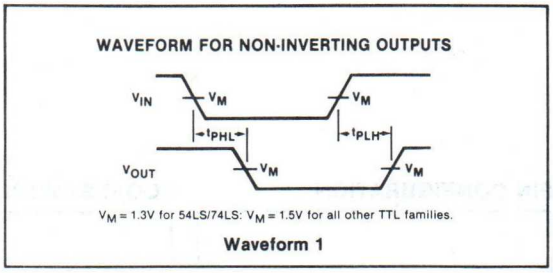
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7432			54/74LS32			54/74S32			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			15	22		3.1	6.2		18	32	mA
		I_{CCL} Outputs LOW			23	38		4.9	9.8		38	68	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM



Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		15 22		22 22		7.0 7.0	ns

Quad Two-Input NOR Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7433	11ns	23mA
74LS33	19ns	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7433N • N74LS33N	
Ceramic DIP	N7433F • N74LS33F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

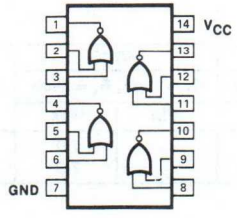
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

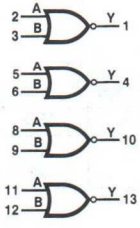
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1ul	1LSul
Y	Output	30ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

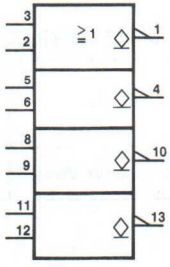
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to −5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

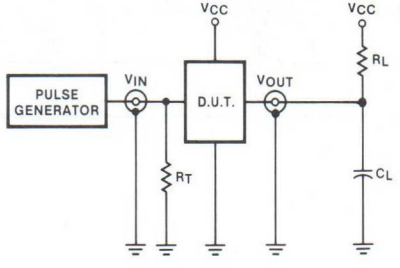
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5	V
I_{OL}	LOW-level output current	Mil			48			12	mA
		Com'l			48			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

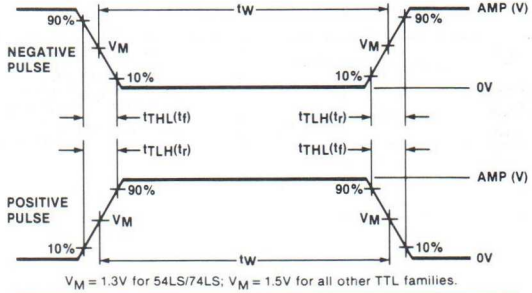
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

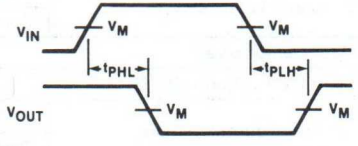
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7433			54/74LS33			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					250			250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		12	21		1.8	3.6	mA
			I_{CCL}	Outputs LOW		33	57		6.9	13.8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			R_L = 133Ω		C_L = 45pF, R_L = 667Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	C_L = 50pF for 54/7433 Waveform 1		15 18		32 28	ns
t_{PLH} t_{PHL}	Propagation delay	C_L = 150pF for 54/7433 Waveform 1		22 24			ns

Quad Two-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7437	11ns	22mA
74LS37	12ns	3.5mA
74S37	4ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7437N • N74LS37N N74S37N	
Ceramic DIP	N7437F • N74LS37F N74S37F	S54S37F • S54LS37F
Flatpack		S54S37W • S54LS37W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

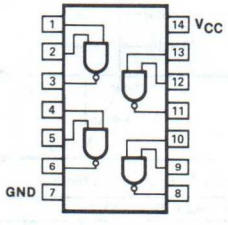
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

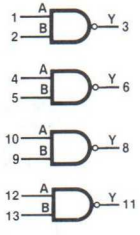
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

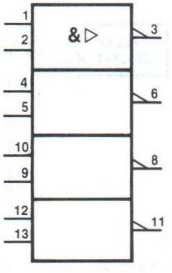
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

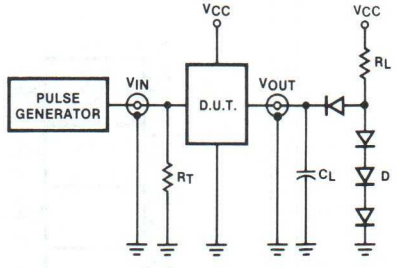
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−1200			−1200			−3000	μA
I_{OL}	LOW-level output current	Mil			48			12			60	mA
		Com'l			48			24			60	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

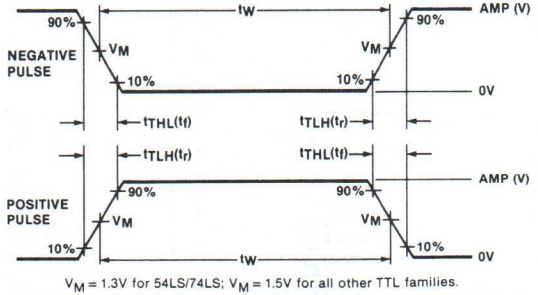
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

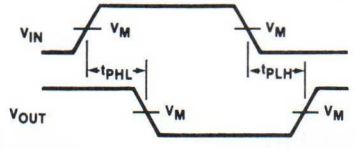
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7437			54/74LS37			54/74S37			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 12mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			100	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 4.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 70	– 30		– 100	– 50		– 225	mA
			Com'l	– 18		– 70	– 30		– 100	– 50		– 225	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			9	15.5		0.9	2		20	36	mA
		I_{CCL} Outputs LOW			34	54		6	12		46	80	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second for the 54/7437 and 54/74LS37, and 100 milliseconds for the 54/74S37.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 45pF, R_L = 133Ω		C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 93Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay	Waveform 1		22		24		6.5	ns
t_{PHL}			15		24		6.5	

Quad Two-Input NAND Buffers (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7438	13ns	28mA
74LS38	19ns	3.5mA
74S38	6.5ns	33mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7438N • N74LS38N N74S38N	
Ceramic DIP	N7438F • N74LS38F N74S38F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

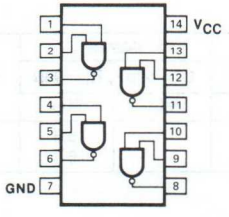
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

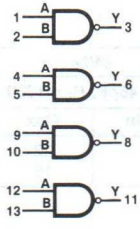
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

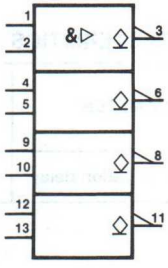
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

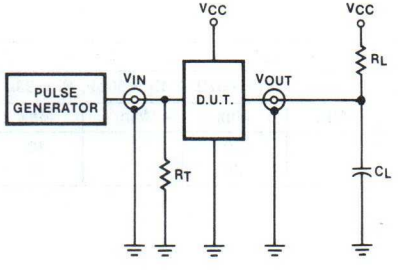
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5			5.5	V
I_{OL}	LOW-level output current	Mil			48			12			60	mA
		Com'l			48			24			60	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

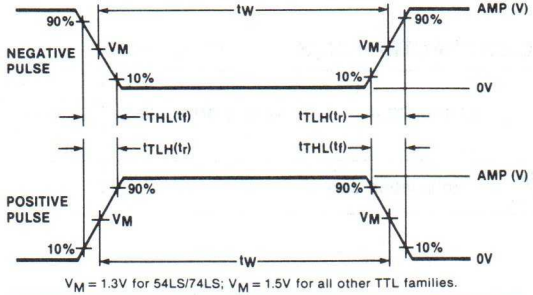
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

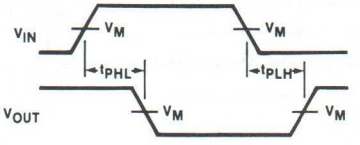
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7438			54/74LS38			54/74S38			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					250			250			250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 4.0	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		5	8.5		0.9	2		20	36	mA
			I_{CCL}	Outputs LOW		34	54		6	12		46	80	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
			C_L = 45pF, R_L = 133Ω		C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 93Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 18		32 28		10 10	ns

Quad Two-Input NAND Buffer (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7439	11ns	4.5mA (I_{CCH}) 30mA (I_{CCL})

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7439N	
Ceramic DIP	N7439F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

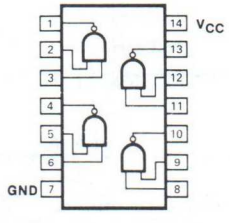
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

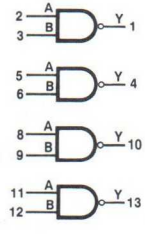
PINS	DESCRIPTION	54/74
A, B	Inputs	1ul
Y	Output	30ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

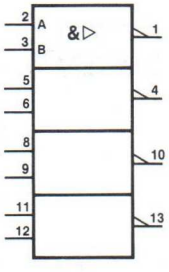
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

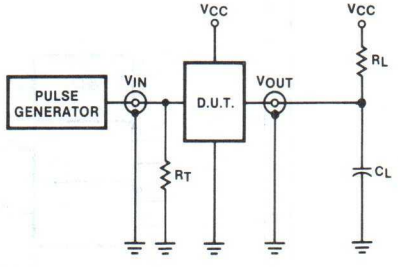
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

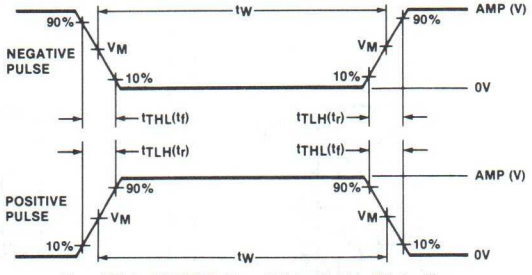
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

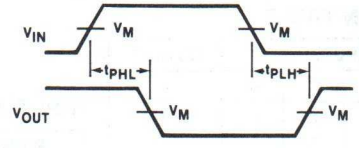
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/7439 Min	54/7439 Typ[2]	54/7439 Max	UNIT
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IL} = MAX, V_{OH} = 5.5V				250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				− 1.6	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		4.5	8.5	mA
			I_{CCL} Outputs LOW		30	54	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 45pF, R_L = 133Ω Min	54/74 C_L = 45pF, R_L = 133Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 18	ns

Dual Four-Input NAND Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7440	11ns	11mA
74LS40	12ns	1.8mA
74S40	6ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7440N • N74LS40N N74S40N	
Ceramic DIP	N7440F • N74LS40F N74S40F	S54S40F
Flatpack		S54S40W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

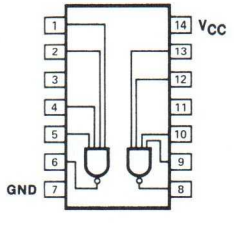
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

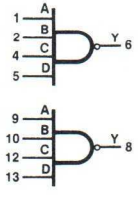
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A–D	Inputs	1ul	2Sul	1LSul
Y	Output	30ul	30Sul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

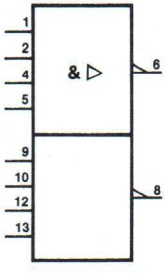
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

3

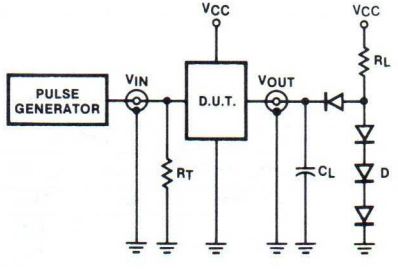
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−1200			−1200			−3000	μA
I_{OL}	LOW-level output current	Mil			48			12			60	mA
		Com'l			48			24			60	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

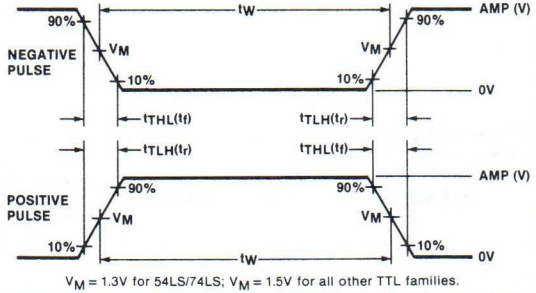
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

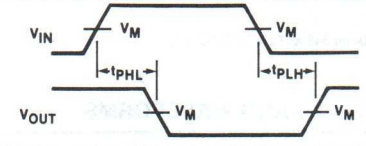
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7440			54/74LS40			54/74S40			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 12mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			100	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 4	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 70	– 15		– 100	– 50		– 225	mA
			Com'l	– 18		– 70	– 15		– 100	– 50		– 225	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			4	8		0.45	1		10	18	mA
		I_{CCL} Outputs LOW			17	27		3	6		25	44	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second. The 54/74S40 test time for I_{OS} should not exceed 100ms.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 133Ω		C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 93Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		24 24		6.5 6.5	ns

DECODERS 54/7442, LS42

BCD-To-Decimal Decoder (1-of-10)

- **Mutually exclusive outputs**
- **1-of-8 demultiplexing capability**
- **Outputs disabled for input codes above nine**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7442	15ns	28mA
74LS42	18ns	7mA

DESCRIPTION

The '42 decoder accepts four active HIGH BCD inputs and provides 10 mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with active LOW input enables.

The logic design of the '42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input, A_3, produces a useful inhibit function when the '42 is used as a 1-of-8 decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

ORDERING CODE

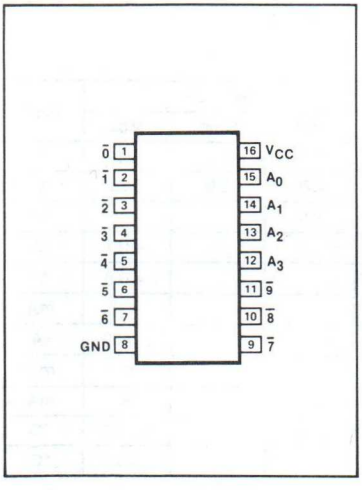
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7442N • N74LS42N	
Ceramic DIP	N7442F • N74LS42F	S5442F • S54LS42F
Flatpack		S5442W • S54LS42W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

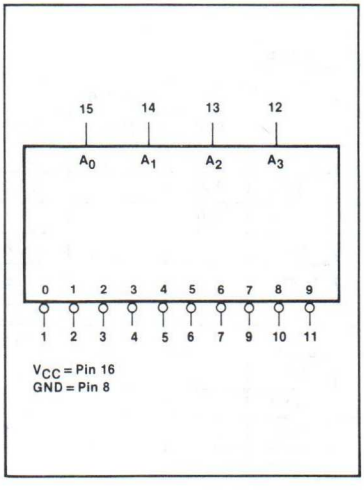
PINS	DESCRIPTION	54/74	54/74LS
A_0-A_3	Inputs	1ul	1LSul
$\bar{0}$-$\bar{9}$	Ouputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

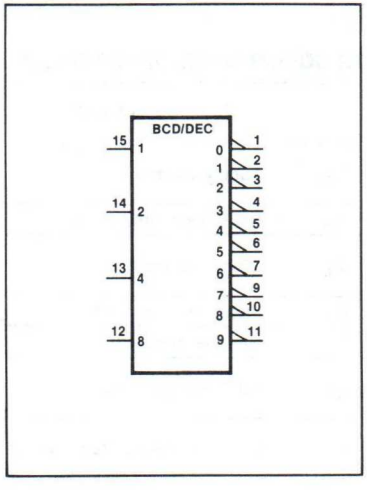
PIN CONFIGURATION



LOGIC SYMBOL

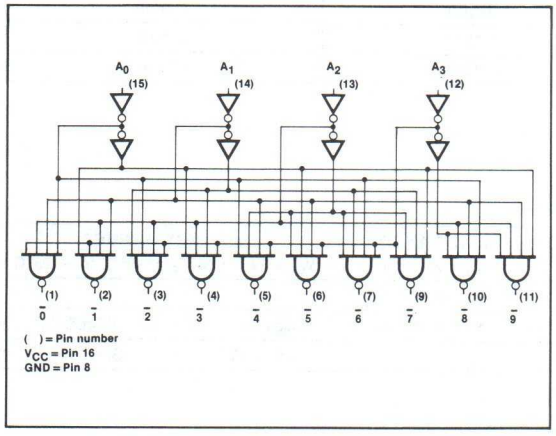


LOGIC SYMBOL (IEEE/IEC)



DECODERS 54/7442, LS42

LOGIC DIAGRAM



FUNCTION TABLE

A_3	A_2	A_1	A_0	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$	$\bar{8}$	$\bar{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to −5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

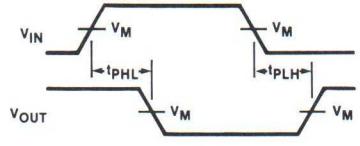
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7442			54/74LS42			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		28	41		7	13	mA
				Com'l		28	56		7	13	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open and all inputs grounded.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

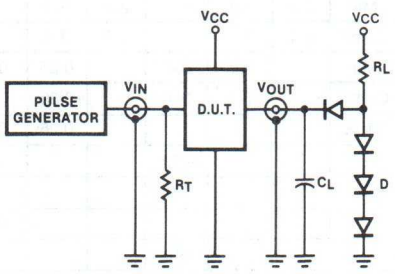
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		30		30	ns
t_{PHL}	Address to output	3 logic levels		30		30	
t_{PLH}	Propagation delay	Waveform 1		25		25	ns
t_{PHL}	Address to output	2 logic levels		25		25	

TEST CIRCUITS AND WAVEFORMS

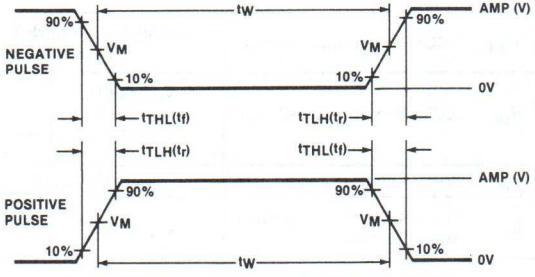
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DRIVER 54/7445

BCD-To-Decimal Decoder/Driver (Open Collector)

- **80mA output sink capability**
- **30V output breakdown voltage**
- **Ideally suited as lamp or solenoid driver**
- **See '42 for standard TTL output version**
- **See '145 for "LS" version**

TYPE	MAX I_{OL}	TYPICAL SUPPLY CURRENT (Total)
7445	80mA	43mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7445N	
Ceramic DIP	N7445F	

DESCRIPTION

The '45 decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are off. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '45 can sink 20mA while maintaining the standardized guaranteed output LOW voltage (V_{OL}) of 0.4V, but it can sink up to 80mA with a guaranteed V_{OL} of less than 0.9V.

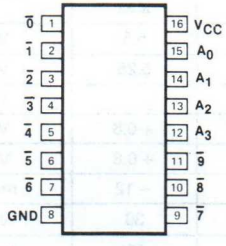
The '45 features an output breakdown voltage of 30V and is ideally suited as a lamp or solenoid driver.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

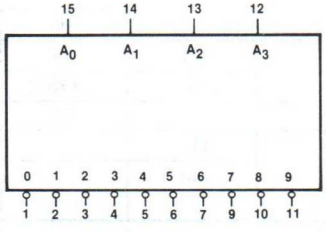
PINS	DESCRIPTION	54/74
A_0–A_3	Inputs	1ul
$\overline{0}$–$\overline{9}$	Outputs	12.5ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

PIN CONFIGURATION

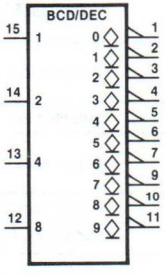


LOGIC SYMBOL



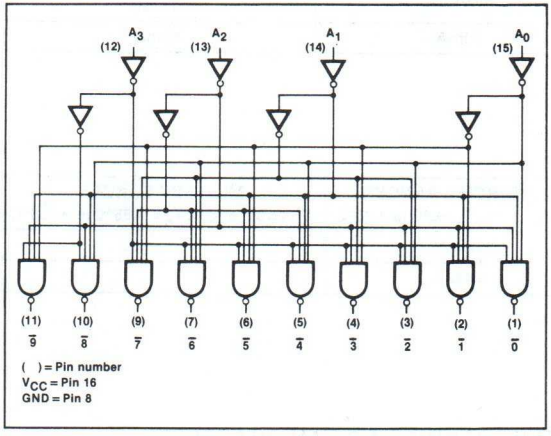
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER 54/7445

LOGIC DIAGRAM



FUNCTION TABLE

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +30	−0.5 to +30	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
V_{OH}	HIGH-level output voltage				30	V
I_{OL}	LOW-level output current	Mil			80	mA
		Com'l			80	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

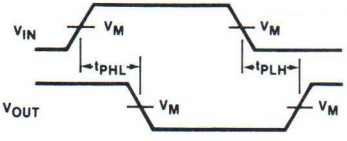
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/7445			UNIT
				Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 30V				250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 20mA			0.4	V
			I_{OL} = 80mA		0.5	0.9	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				– 1.6	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	Mil		43	62	mA
			Com'l		43	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with all inputs grounded and outputs open.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

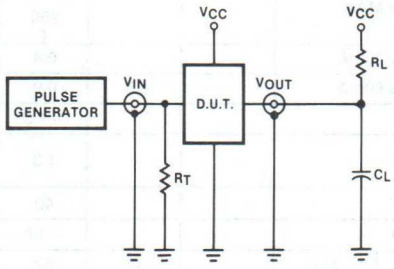
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 100Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		50 50	ns

TEST CIRCUITS AND WAVEFORMS

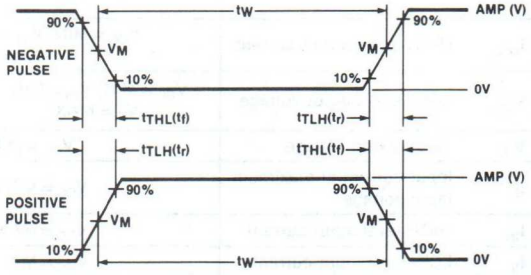
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

'51, 'S51 Dual 2-Wide 2-Input AND-OR-Invert Gate
'LS51 Dual 2-Wide 3-Input, 2-Wide 2-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7451	11ns	5.7mA
74LS51	12ns	1.1mA
74S51	3.5ns	11mA

FUNCTION TABLE
'51, 'S51, ½ 'LS51

INPUTS				OUTPUT
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

'LS51

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	X	X	X	L
X	X	X	H	H	H	L
All other combinations						H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ORDERING CODE

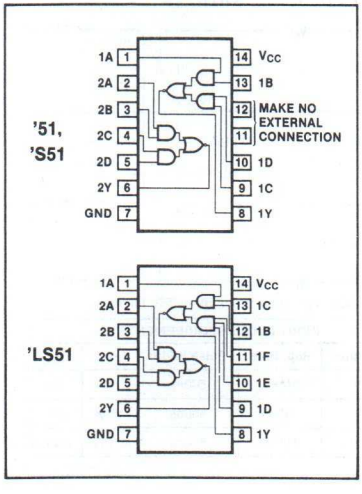
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7451N • N74LS51N N74S51N	
Ceramic DIP	N7451F • N74LS51F N74S51F	S54S51F • S54LS51F
Flatpack		S54S51W • S54LS51W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

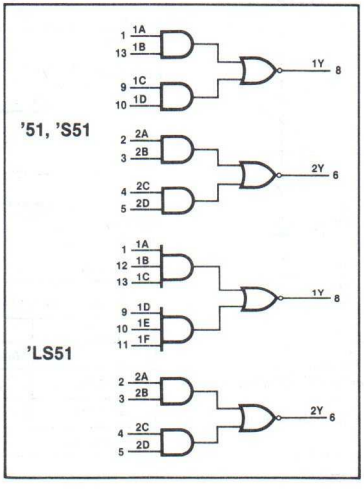
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

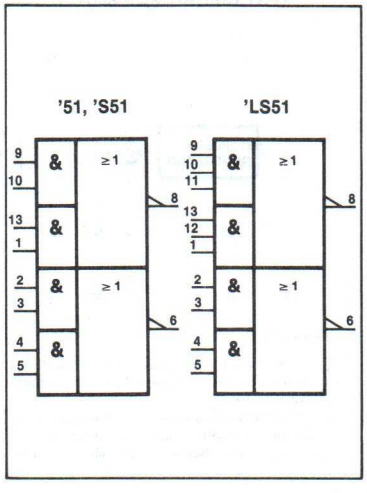
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

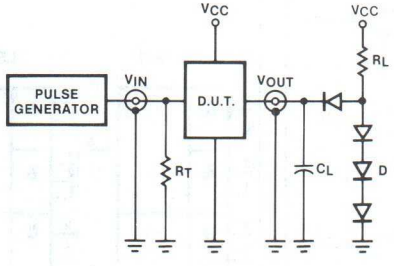
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

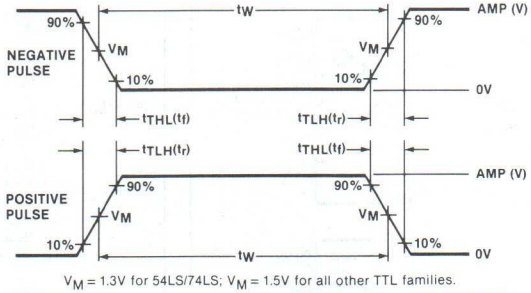
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

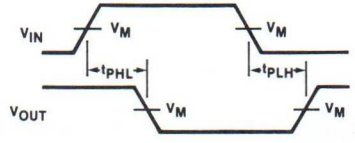
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/7451			54/74LS51			54/74S51			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[4]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH			4	8		0.8	1.6		8.2	17.8	mA
		I_{CCL} Outputs LOW			7.4	14		1.4	2.8		13.6	22	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
t_{PLH} / t_{PHL} Propagation delay	Waveform 1		22 15		20 20		5.5 5.5	ns

GATE 54/74LS54

Four-Wide Two- & Three-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS54	12ns	0.9mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS54N	
Ceramic DIP	N74LS54F	

FUNCTION TABLE

INPUTS										OUTPUT
A	B	C	D	E	F	G	H	J	K	Y
H	H	X	X	X	X	X	X	X	X	L
X	X	H	H	H	X	X	X	X	X	L
X	X	X	X	X	H	H	X	X	X	L
X	X	X	X	X	X	X	H	H	H	L
All other combinations										H

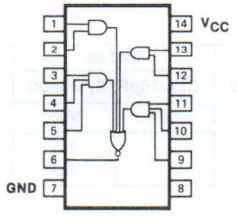
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

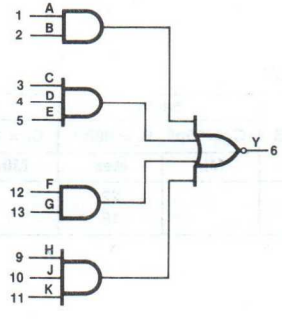
PINS	DESCRIPTION	54/74LS
A-K	Inputs	1LSul
Y	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

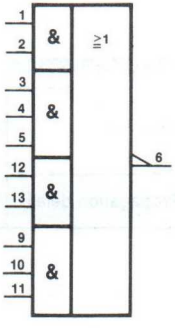
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

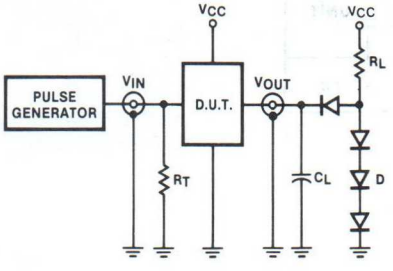
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

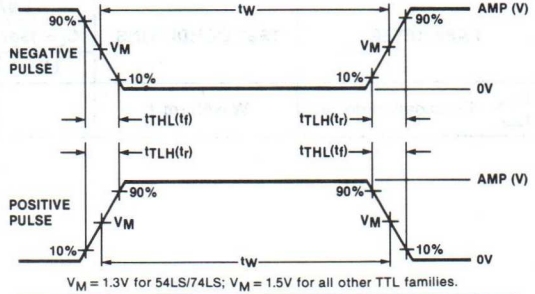
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

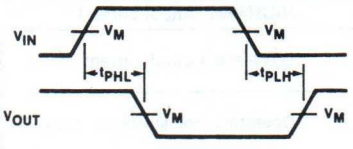
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS54			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		0.8	1.6	mA
			I_{CCL}	Outputs LOW		1.0	2.0	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		20 20	ns

Four-Two-Three-Two-Input AND-OR-Invert Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S64	3.5ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S64N	
Ceramic DIP	N74S64F	

FUNCTION TABLE

INPUTS											OUTPUT
A	B	C	D	E	F	G	H	J	K	L	Y
H	H	X	X	X	X	X	X	X	X	X	L
X	X	H	H	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

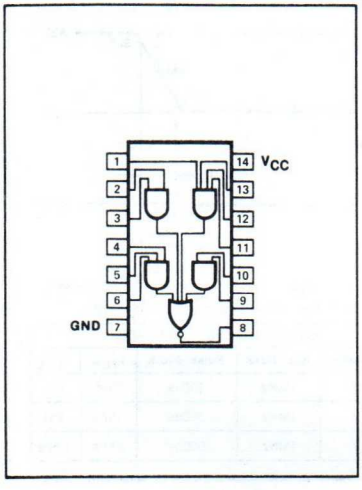
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

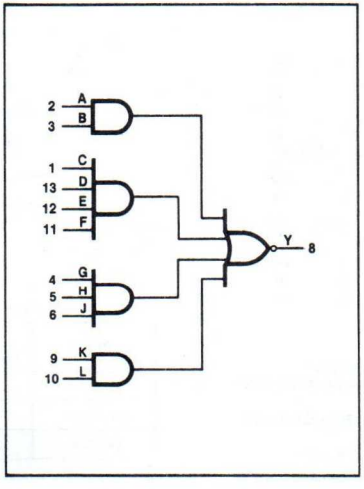
PINS	DESCRIPTION	54/74S
A-L	Inputs	1Sul
Y	Output	10Sul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

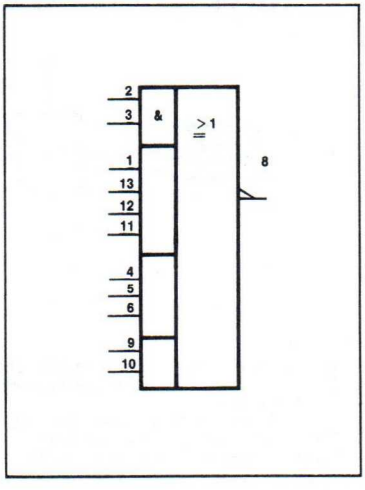
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

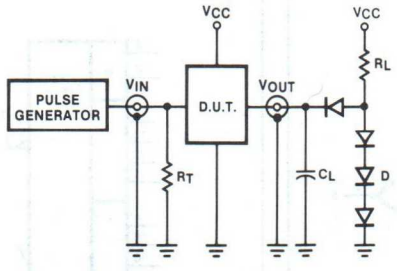
PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

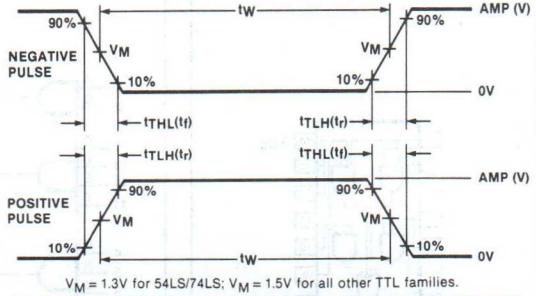
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

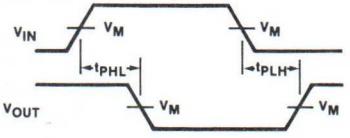
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S64 Min	54/74S64 Typ[2]	54/74S64 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil			0.5	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		7	12.5	mA
			I_{CCL} Outputs LOW		8.5	16	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74S C_L = 15pF, R_L = 280Ω Min	54/74S C_L = 15pF, R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		5.5 5.5	ns

FLIP-FLOPS

54/7473, LS73

Dual J-K Flip-Flop

DESCRIPTION

The '73 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 7473 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW transition. For the 7473, the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS73 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7473	20MHz	10mA
74LS73	45MHz	4mA

ORDERING CODE

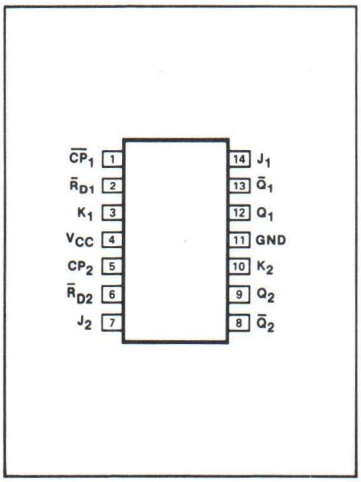
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7473N • N74LS73N	
Ceramic DIP	N7473F • N74LS73F	S5473F • S54LS73F
Flatpack		S5473W • S54LS73W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

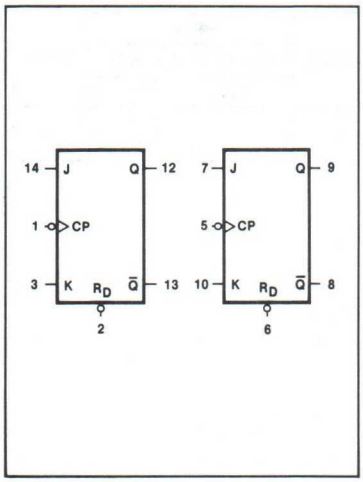
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}$	Clock input	2ul	4LSul
$\overline{R}_D$	Reset input	2ul	3LSul
J, K	Data inputs	1ul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

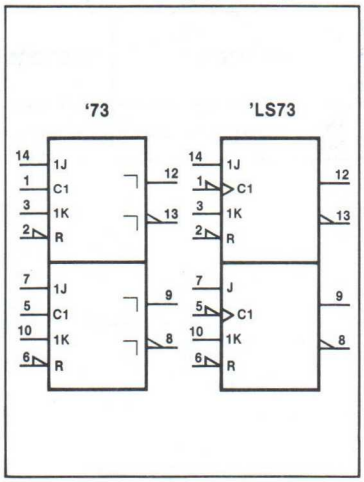
PIN CONFIGURATION



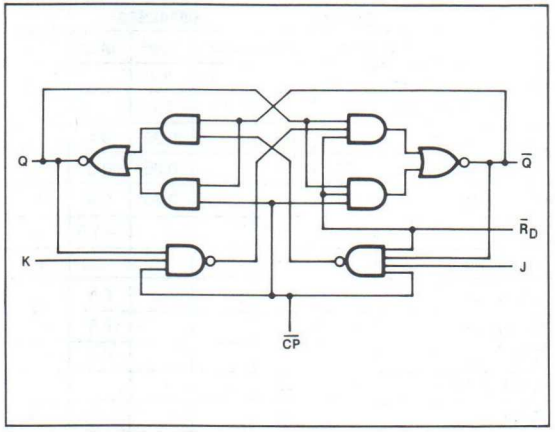
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{R}_D$	$\overline{CP}$[b]	J	K	Q	$\overline{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "0" (Reset)	H	⎍	l	h	L	H
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.[a]
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.[a]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⎍ = Positive Clock pulse.

NOTES
a. The J and K inputs of the 7473 must be stable while the Clock is HIGH for conventional operation.
b. The 74LS73 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/7473			54/74LS73			UNIT
						Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX			Mil	2.4	3.4		2.5	3.4		V
					Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX		Mil		0.2	0.4		0.25	0.4	V
					Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA		74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}						– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All Inputs				1.0				mA
			V_I = 7.0V	J, K Inputs							0.1	mA
				$\overline{R}_D$ Inputs							0.3	mA
				$\overline{CP}$ Inputs							0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	J, K Inputs				40				μA
				$\overline{R}_D$ Inputs				80				μA
				$\overline{CP}$ Inputs				80				μA
			V_I = 2.7V	J, K Inputs							20	μA
				$\overline{R}_D$ Inputs							60	μA
				$\overline{CP}$ Inputs							80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		J, K Inputs				– 1.6			– 0.4	mA
				$\overline{R}_D$ Inputs				– 3.2			– 0.8	mA
				$\overline{CP}$ Inputs				– 3.2			– 0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			Mil	– 20		– 57	– 20		– 100	mA
					Com'l	– 18		– 57	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX					10	40		4	8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 3	15		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1, 'LS73 Waveform 3, '73		25 40		20 30	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ to output	Waveform 2		25 40		20 30	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

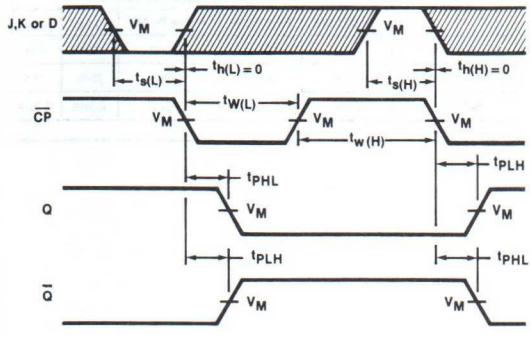
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	47				ns
$t_W(L)$	Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s	Setup time J or K to Clock[a]	Waveform 1	0		20		ns
t_h	Hold time J or K to Clock	Waveform 1	0		0		ns

3

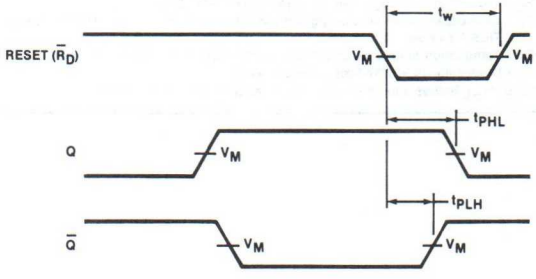
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



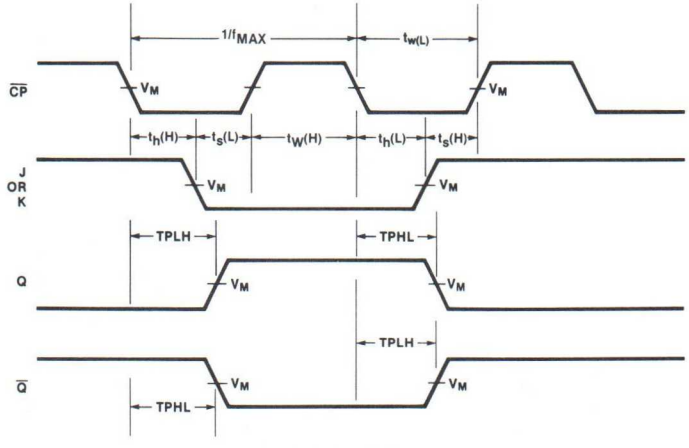
Waveform 1

RESET TO OUTPUT DELAYS, RESET PULSE WIDTHS



Waveform 2

PROPAGATION DELAY AND f_{MAX}

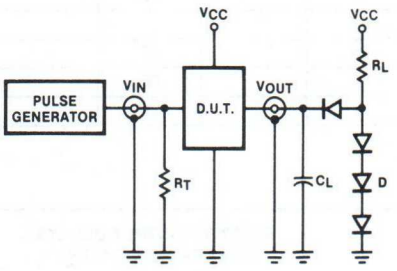


Waveform 3

V_M = 1.3V for 54LS/74S: V_M = 1.5V for all other TTL famillies.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

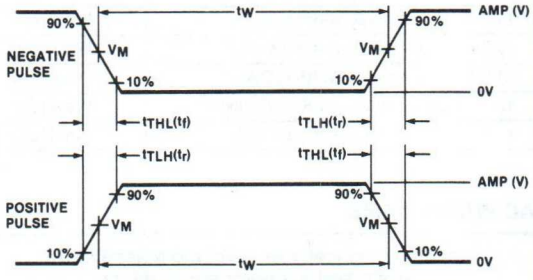
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual D-Type Flip-Flop

DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7474	25MHz	17mA
74LS74A	33MHz	4mA
74S74	100MHz	30mA

3

ORDERING CODE

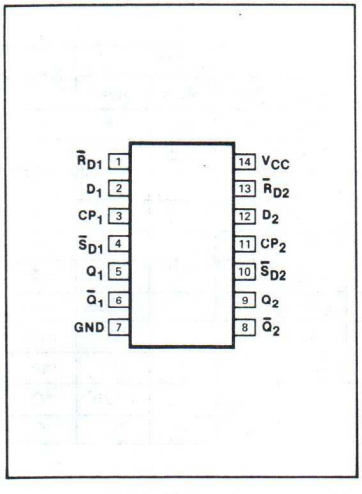
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7474N • N74LS74AN N74S74N	
Ceramic DIP	N7474F • N74LS74AF N74S74F	S5474F • S54LS74AF S54S74F
Flatpack		S5474W • S54LS74AW S54S74W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

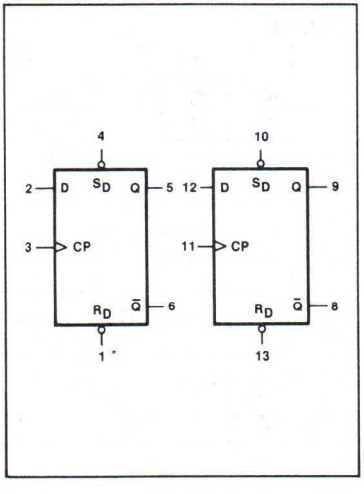
PINS	DESCRIPTION	54/74	54/74S	54/74LS
D	Input	1ul	1Sul	1LSul
$\overline{R}_D$	Input	2ul	3Sul	2LSul
$\overline{S}_D$	Input	1ul	2Sul	2LSul
CP	Input	2ul	2Sul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

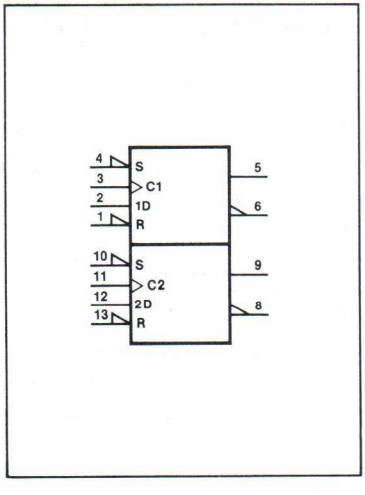
PIN CONFIGURATION



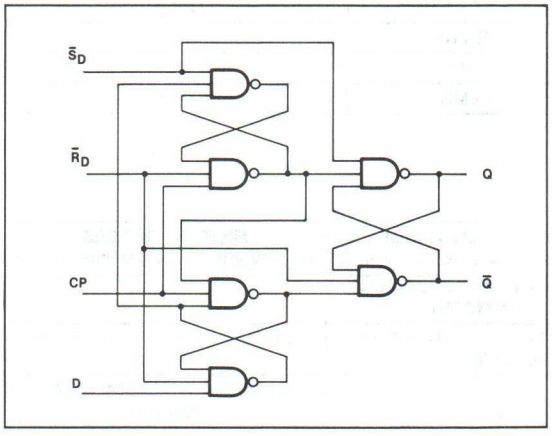
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined[a]	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

NOTE
(a) Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7474			54/74LS74A			54/74S74			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[6]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	D input						0.1				mA
				$\overline{R}_D$ input						0.2				mA
				$\overline{S}_D$ input						0.2				mA
				CP input						0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	D input			40							μA
				$\overline{R}_D$ input			120							μA
				$\overline{S}_D$ input			80							μA
				CP input			80							μA
			V_I = 2.7V	D input						20			50	μA
				$\overline{R}_D$ input						40			150	μA
				$\overline{S}_D$ input						40			100	μA
				CP input						20			100	μA
I_{IL}	LOW-level input current[5]	V_{CC} = MAX	V_I = 0.4V	D input			-1.6			-0.4				mA
				$\overline{R}_D$ input			-3.2			-0.8				mA
				$\overline{S}_D$ input			-1.6			-0.8				mA
				CP input			-3.2			-0.4				mA
			V_I = 0.5V	D input									-2	mA
				$\overline{R}_D$ input									-6	mA
				$\overline{S}_D$ input									-4	mA
				CP input									-4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-57	-20		-100	-40		-100	mA
				Com'l	-18		-57	-20		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				17	30		4	8		30	50	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the shorted circuit should not exceed one second.
4. Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and $\overline{Q}$ outputs HIGH in turn.
5. Set is tested with reset HIGH and reset is tested with set HIGH.
6. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		54LS/74LS C_L = 15pF, R_L = 2kΩ		54S/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	15		25		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		25 40		25 40		9 9	ns
t_{PLH} t_{PHL}	Propagation delay Set or Reset to output	Waveform 2		25 40		25 40		6 13.5	ns
		Waveform 2 CP = HIGH							
t_{PHL}	Set or Reset to output	Waveform 2 CP = LOW		40		40		8	ns

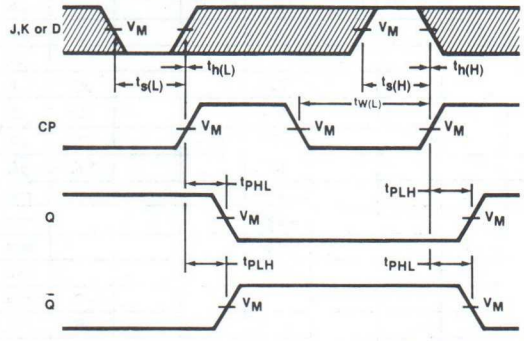
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_W(H)$ Clock pulse width (HIGH)	Waveform 1	30		25		6		ns
$t_W(L)$ Clock pulse width (LOW)	Waveform 1	37				7.3		ns
$t_W(L)$ Set or reset pulse width (LOW)	Waveform 2	30		25		7		ns
$t_s(H)$ Setup time (HIGH) data to clock	Waveform 1	20		20		3		ns
$t_s(L)$ Setup time (LOW) data to clock	Waveform 1	20		20		3		ns
t_h Hold time data to clock	Waveform 1	5		5		2		ns

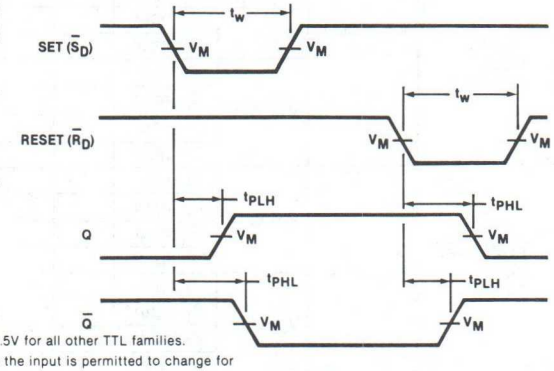
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

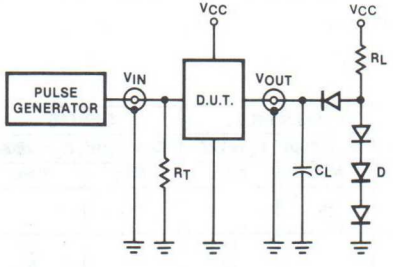


Waveform 2

$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

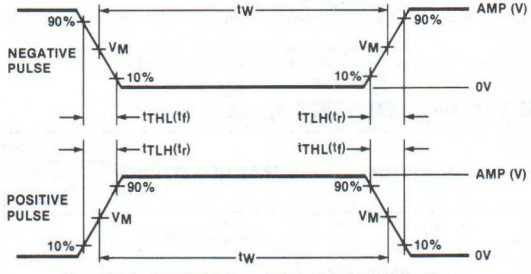
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCHES

54/7475, LS75

Quad Bistable Latch

- **4-bit bistable latch**
- **Refer to 54LS/74LS375 for V_{CC} and GND on corner pins**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7475	18ns (t_{PLH}) 9ns (t_{PHL})	32mA
74LS75	15ns (t_{PLH}) 9ns (t_{PHL})	6.3mA

DESCRIPTION

The '75 has four bistable latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched outputs remain stable as long as the enable is LOW.

ORDERING CODE

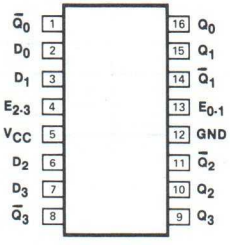
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N7475N • N74LS75N	
Ceramic DIP	N7475F • N74LS75F	S5475F • S54LS75F
Flatpack		S5475W • S54LS75W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

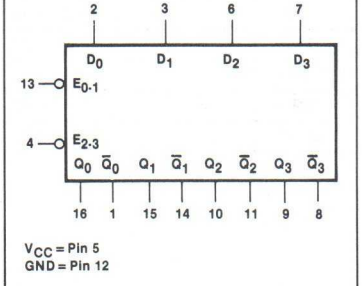
PINS	DESCRIPTION	54/74	54/74LS
D	Input	2ul	1LSUl
E	Input	4ul	4LSUl
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA.

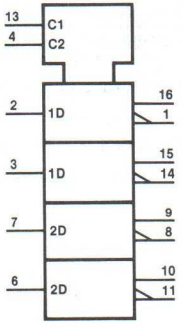
PIN CONFIGURATION



LOGIC SYMBOL

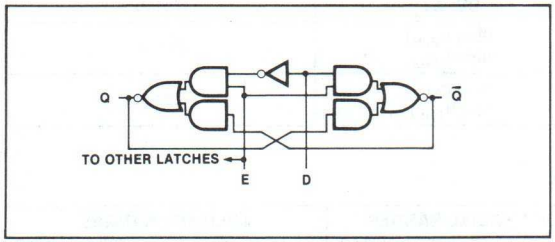


LOGIC SYMBOL (IEEE/IEC)



LATCHES 54/7475, LS75

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	$\overline{Q}$
Data Enabled	H H	L H	L H	H L
Data Latched	L	X	q	$\overline{q}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7475			54/74LS75			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	D inputs						0.1	mA
				E inputs						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	D inputs			80				μA
				E inputs			160				μA
			V_I = 2.7V	D inputs						20	μA
				E inputs						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	D inputs			-3.2			-0.4	mA
				E inputs			-6.4			-1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-57	-20		-100	mA
				Com'l	-18		-57	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		32	46		6.3	12	mA
				Com'l		32	53		6.3	12	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

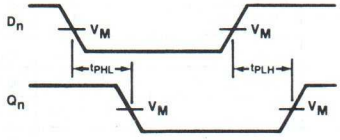
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		30 25		27 17	ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		40 15		20 15	ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		30 15		27 25	ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		30 15		30 15	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	Enable pulse width	Waveform 3	20		20		ns
t_s	Setup time, Data to Enable	Waveform 4	20		20		ns
t_h	Hold time, Data to Enable	Waveform 4	5.0		5.0		ns

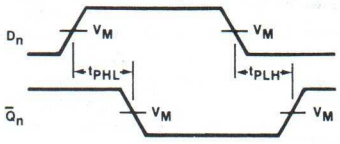
AC WAVEFORMS

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 1

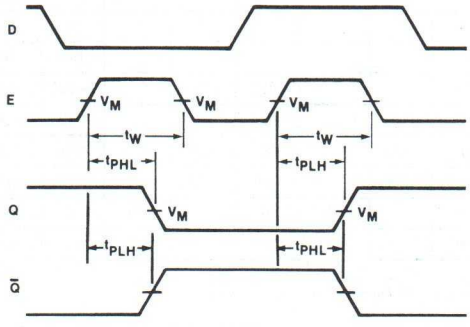
PROPAGATION DELAY DATA TO $\overline{Q}$ OUTPUTS



Waveform 2

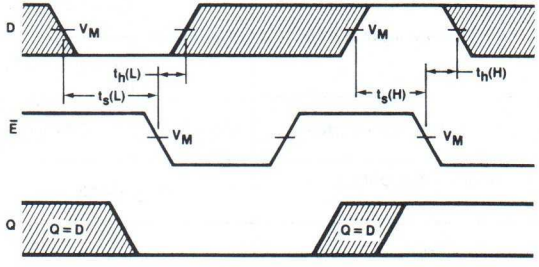
V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



Waveform 3

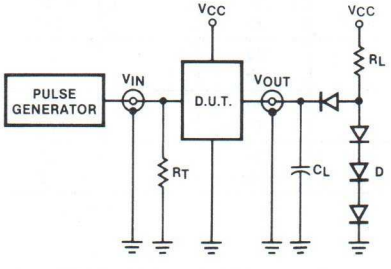
DATA SETUP AND HOLD TIMES



Waveform 4

TEST CIRCUITS AND WAVEFORMS

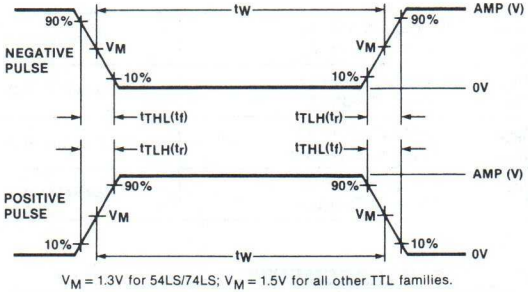
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS

54/7476, LS76

Dual J-K Flip-Flop

DESCRIPTION

The '76 is a dual J-K flip-flop with individual J, K, Clock, Set and Reset inputs. The 7476 is positive pulse-triggered. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. The J and K inputs must be stable while the Clock is HIGH for conventional operation.

The 74LS76 is a negative edge-triggered flip-flop. The J and K inputs must be stable only one setup time prior to the HIGH-to-LOW Clock transition.

The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs. When LOW, they override the Clock and Data inputs, forcing the outputs to the steady state levels as shown in the Function Table.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7476	20MHz	10mA
74LS76	45MHz	4mA

ORDERING CODE

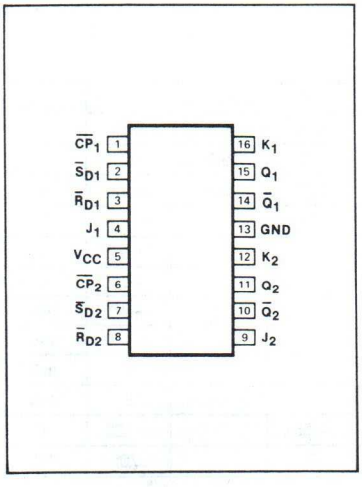
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7476N • N74LS76N	
Ceramic DIP	N7476F • N74LS76F	S5476F • S54LS76F
Flatpack		S5476W • S54LS76W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

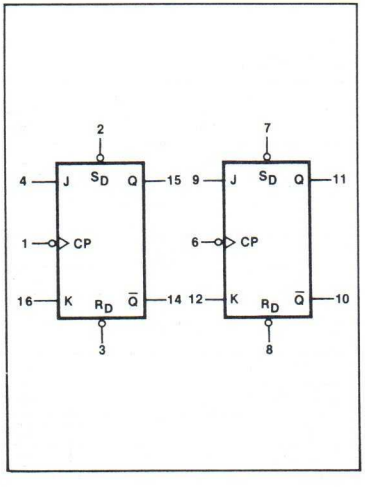
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}$	Clock input	2ul	2LSul
$\overline{R}_D$, $\overline{S}_D$	Reset and Set inputs	2ul	2LSul
J, K	Data inputs	1ul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

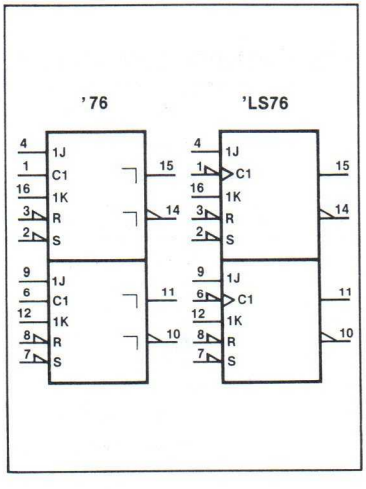
PIN CONFIGURATION



LOGIC SYMBOL

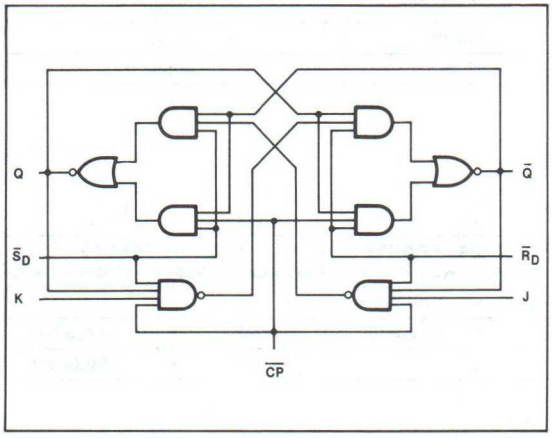


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS 54/7476, LS76

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\bar{S}_D$	$\bar{R}_D$	$\overline{CP}$[b]	J	K	Q	$\bar{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined[a]	L	L	X	X	X	H	H
Toggle	H	H	⎍	h	h	$\bar{q}$	q
Load "0" (Reset)	H	H	⎍	l	h	L	H
Load "1" (Set)	H	H	⎍	h	l	H	L
Hold "no change"	H	H	⎍	l	l	q	$\bar{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.[c]
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.[c]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⎍ = Positive Clock pulse.

NOTES
a. Both outputs will be HIGH while both $\bar{S}_D$ and $\bar{R}_D$ are LOW, but the output states are unpredictable if $\bar{S}_D$ and $\bar{R}_D$ go HIGH simultaneously.
b. The 74LS76 is edge triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.
c. The J and K inputs of the 7476 must be stable while the Clock is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7476			54/74LS76			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	J, K Inputs						0.1	mA
				$\overline{S}_D$, $\overline{R}_D$ Inputs						0.3	mA
				$\overline{CP}$ Inputs						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	J, K Inputs			40				μA
				$\overline{S}_D$, $\overline{R}_D$ Inputs			80				μA
				$\overline{CP}$ Inputs			80				μA
			V_I = 2.7V	J, K Inputs						20	μA
				$\overline{S}_D$, $\overline{R}_D$ Inputs						60	μA
				$\overline{CP}$ Inputs						80	μA
I_{IL}	LOW-level input current[5]	V_{CC} = MAX, V_I = 0.4V		J, K Inputs			– 1.6			– 0.4	mA
				$\overline{S}_D$, $\overline{R}_D$ Inputs			– 3.2			– 0.8	mA
				$\overline{CP}$ Inputs			– 3.2			– 0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				10	40		4	8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.
5. $\overline{S}_D$ is tested with $\overline{R}_D$ HIGH, and $\overline{R}_D$ is tested with $\overline{S}_D$ HIGH.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 3	15		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1, 'LS76 Waveform 3, '76		25 40		20 30	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		25 40		20 30	ns

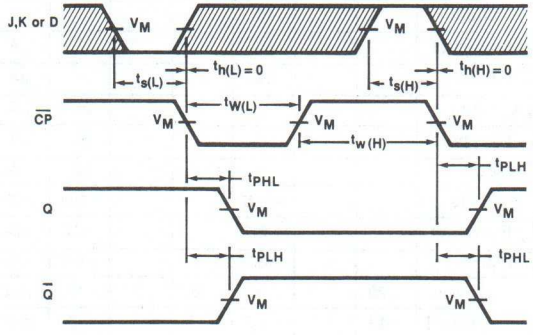
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	47				ns
$t_W(L)$	Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s	Setup time J or K to Clock[(c)]	Waveform 1	0		20		ns
t_h	Hold time J or K to Clock	Waveform 1	0		0		ns

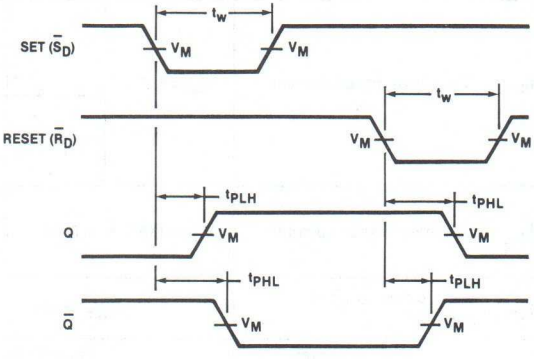
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



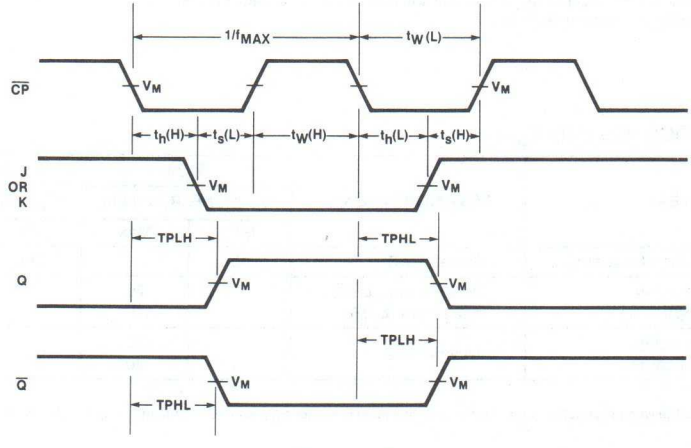
Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS



Waveform 2

PROPAGATION DELAY AND f_{MAX}

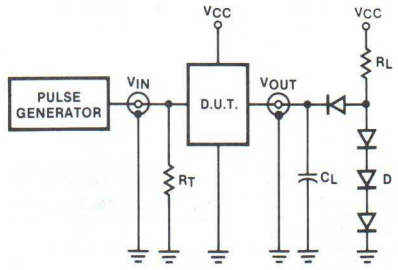


Waveform 3

$V_M = 1.3V$ for 54LS/74S: $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

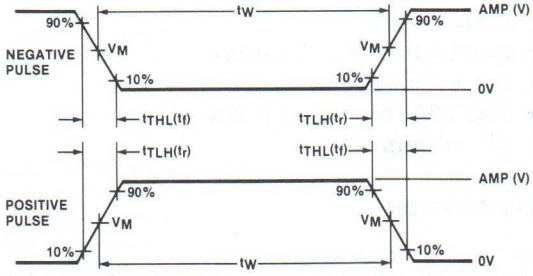
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

ADDERS

54/7483, LS83A

4-Bit Full Adder

- **High speed 4-bit binary addition**
- **Cascadeable in 4-bit increments**
- **LS83A has fast internal carry lookahead**
- **See'283 for corner power pin version**

TYPE	TYPICAL ADD TIMES (Two 8-bit Words)	TYPICAL SUPPLY CURRENT (Total)
7483	23ns	66mA
74LS83A	25ns	19mA

DESCRIPTION

The '83 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs (Σ_1-Σ_4) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '83 can be used with either all active-HIGH operands (positive logic) or with all active-LOW operands (negative logic). See Function Table. With active-HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1, can arbitrarily be assigned to pins 10, 11, 13, etc.

ORDERING CODE

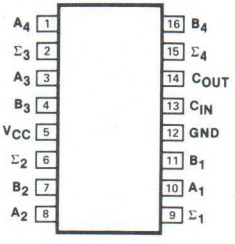
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7483N • N74LS83AN	
Ceramic DIP	N7483F • N74LS83AF	S5483F • S54LS83AF
Flatpack		S5483W • S54LS83AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

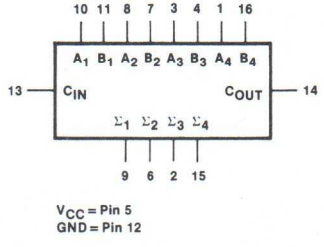
PINS	DESCRIPTION	54/74	54/74LS
A_1, B_1, A_3, B_3, C_{IN}	Inputs	2ul	
A_2, B_2, A_4, B_4	Inputs	1ul	
A, B	Inputs		2LSul
C_{IN}	Input		1LSul
Sum	Outputs	10ul	10LSul
Carry	Output	5ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

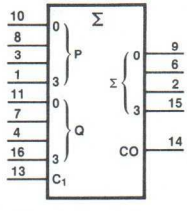
PIN CONFIGURATION



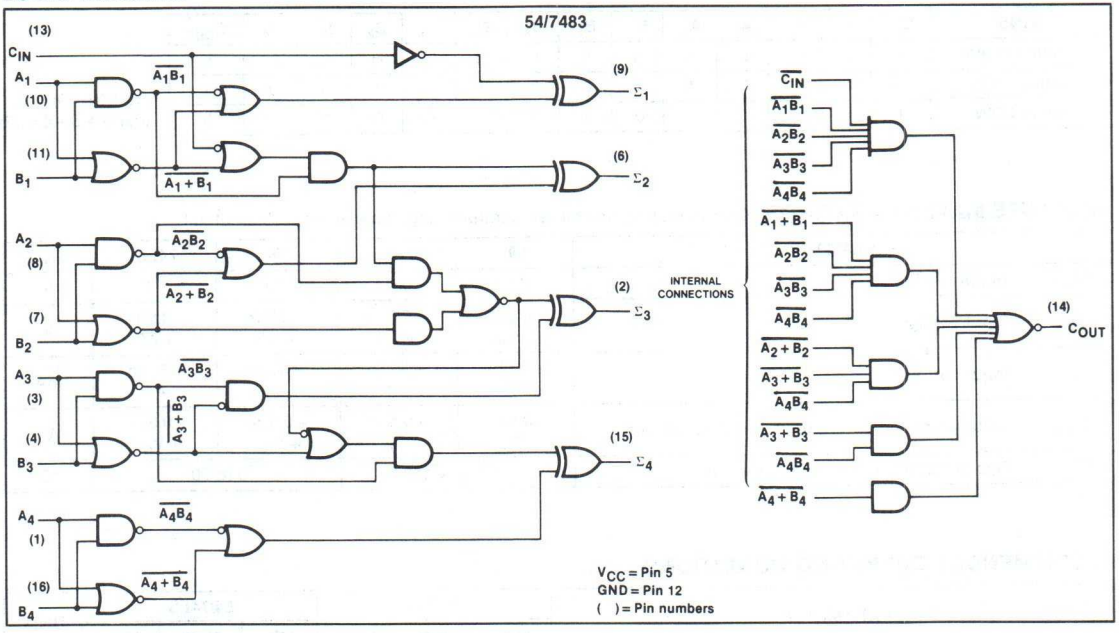
LOGIC SYMBOL



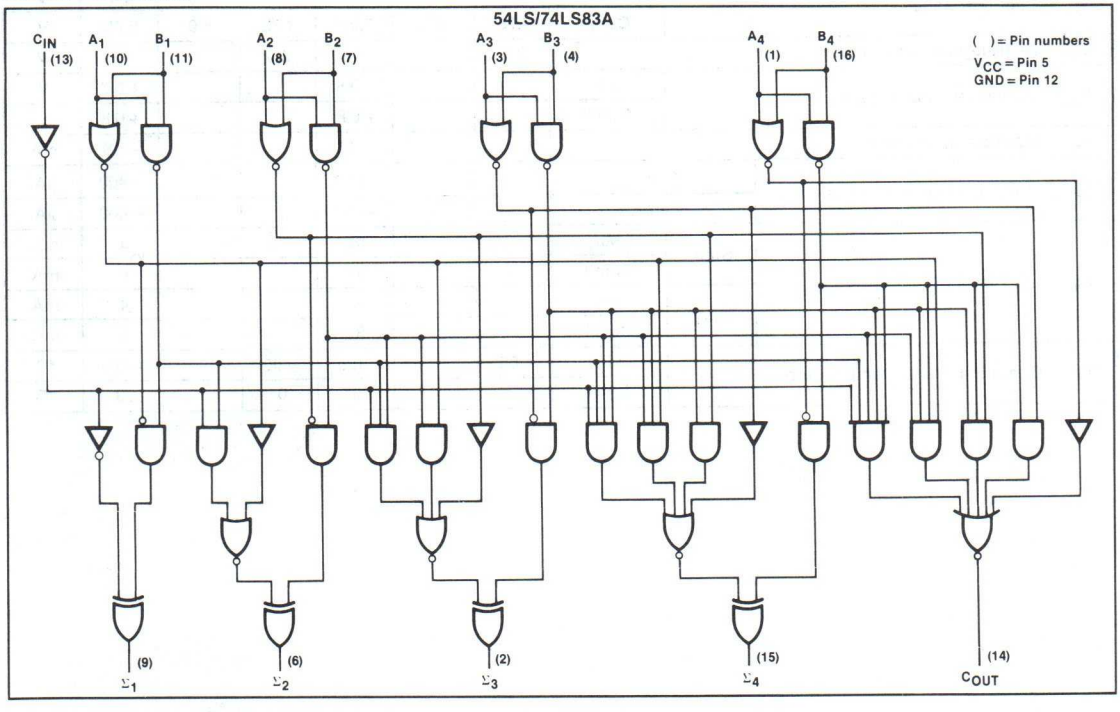
LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

(10 + 9 = 19)
(carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

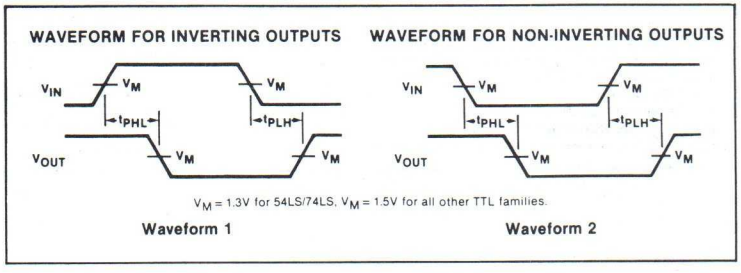
PARAMETER				54/74			54/74LS			UNIT
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			2.0			V
V_{IL}	LOW-level input voltage		Mil			+0.8			+0.7	V
			Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current					−12			−18	mA
I_{OH}	HIGH-level output current	Sum				−800			−400	μA
		Carry				−400			−400	μA
I_{OL}	LOW-level output current	Sum	Mil			16			4	mA
			Com'l			16			8	mA
		Carry	Mil			8			4	mA
			Com'l			8			8	mA
T_A	Operating free-air temperature		Mil	−55		+125	−55		+125	°C
			Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7483			54/74LS83A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	A,B inputs						0.2	mA
				C_{IN} input						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	A_1,B_1,A_3,B_3,C_{IN}			80				μA
				A_2,B_2,A_4,B_4			40				μA
			V_I = 2.7V	A,B inputs						40	μA
				C_{IN} input						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	A_1,B_1,A_3,B_3,C_{IN}				– 3.2				mA
			A_2,B_2,A_4,B_4				– 1.6				mA
			A,B inputs							– 0.8	mA
			C_{IN} input							– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Sum outputs	Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
			C_{OUT} output	Mil	– 20		– 70	– 20		– 100	mA
				Com'l	– 18		– 70	– 20		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, outputs open	All inputs at 4.5V	Mil		66	99		19	34	mA
				Com'l		66	110		19	34	mA
			All inputs grounded						22	39	mA
			All B inputs low, other inputs at 4.5V						19	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS

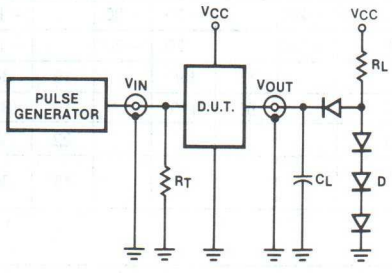


AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 50pF$, $R_L = 400\Omega$		54/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		34 34		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		35 35		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		50 40		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		50 50		24 24	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		40 35		24 24	ns
t_{PLH} t_{PHL}	Propagation delay C_{IN} to C_{OUT}	Waveform 2 $R_L = 780\Omega$ for 54/7483		20 20		17 22	ns
t_{PLH} t_{PHL}	Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2 $R_L = 780\Omega$ for 54/7483		22 22		17 17	ns

TEST CIRCUITS AND WAVEFORMS

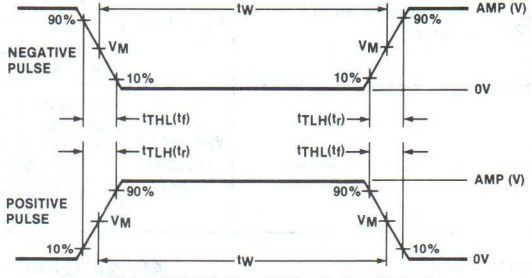
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COMPARATORS 54/7485, LS85, S85

4-Bit Magnitude Comparator

- **Magnitude comparison of any binary words**
- **Serial or parallel expansion without extra gating**
- **Use 54S/74S85 for very high speed comparisons**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7485	23ns	55mA
74LS85	23ns	10mA
74S85	12ns	73mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7485N • N74LS85N N74S85N	
Ceramic DIP	N7485F • N74LS85F N74S85F	S5485F • S54LS85F S54S85F
Flatpack		S5485W • S54LS85W S54S85W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
A_0–A_3, B_0–B_3, $I_{A=B}$	Inputs	3ul	3Sul	3LSul
$I_{A<B}$, $I_{A>B}$	Inputs	1ul	1Sul	1LSul
A = B, A < B, A > B	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −4.0mA I_{IL}.

DESCRIPTION

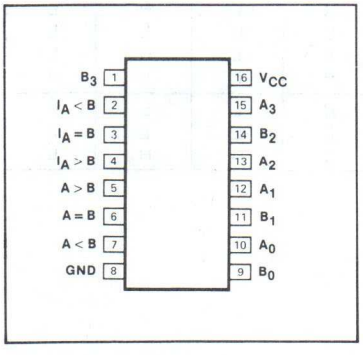
The '85 is a 4-bit magnitude comparator that can be expanded to almost any length. It compares two 4-bit binary, BCD, or other monotonic codes and presents the three possible magnitude results at the outputs. The 4-bit inputs are weighted ($A_0 \rightarrow A_3$) and ($B_0 \rightarrow B_3$), where A_3 and B_3 are the most significant bits.

The operation of the '85 is described in the Function Table, showing all possible logic conditions. The upper part of the table describes the normal operation under all conditions that will occur in a single device or in a series expansion scheme. In the upper part of the table the three outputs are mutually exclusive. In the lower part of the table, the outputs reflect the feed-forward conditions that exist in the parallel expansion scheme.

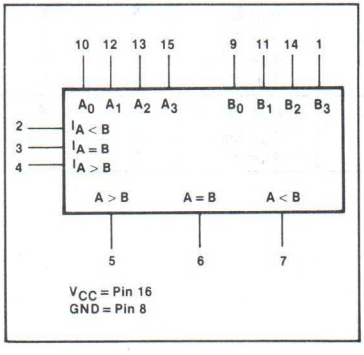
The expansion inputs $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ are the least significant bit positions. When used for series expansion, the A > B, A = B and A < B outputs of the least significant word are connected to the corresponding $I_{A>B}$, $I_{A=B}$, and $I_{A<B}$ inputs of the next higher stage. Stages can be added in this manner to any length, but a propagation delay penalty of about 15ns is added with each additional stage. For proper operation the expansion inputs of the least significant word should be tied as follows: $I_{A>B}$ = LOW, $I_{A=B}$ = HIGH, and $I_{A<B}$ = LOW.

The parallel expansion scheme shown in Figure A demonstrates the most efficient general use of these comparators. In the parallel expansion scheme, the expansion inputs can be used as a fifth input bit position except on the least significant device which must be connected as in the serial scheme. The expansion inputs are used by labeling $I_{A>B}$ as an "A" input, $I_{A<B}$ as a "B" input and setting $I_{A=B}$ LOW. The '85 can be used as a 5-bit comparator only when the outputs are used to drive the (A_0–A_3) and (B_0–B_3) inputs of another '85 device. The parallel technique can be expanded to any number of bits as shown in Table 1.

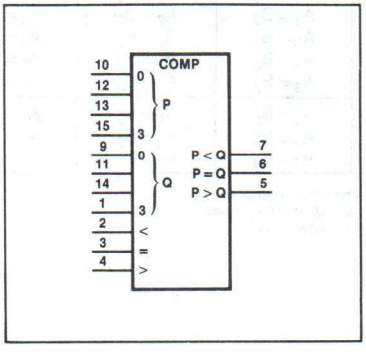
PIN CONFIGURATION



LOGIC SYMBOL

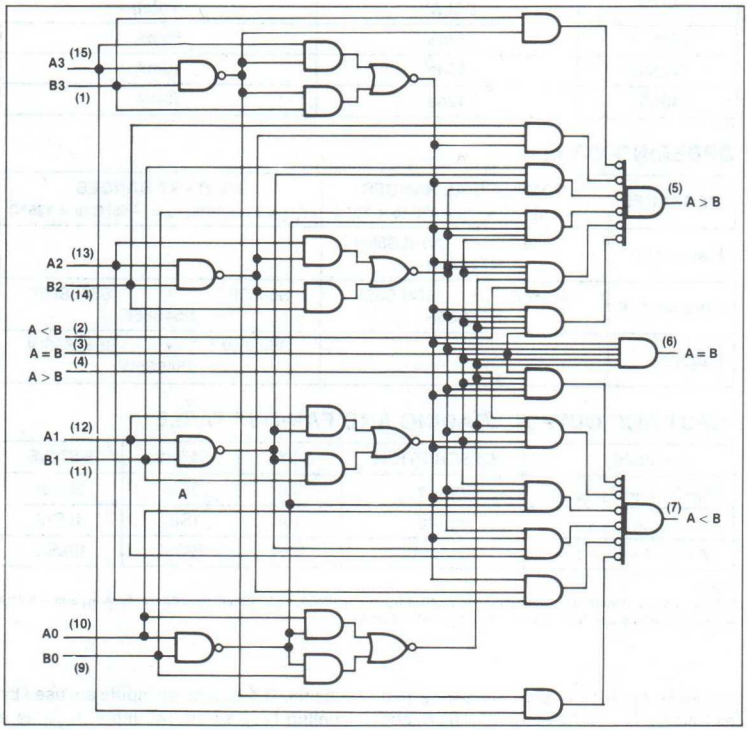


LOGIC SYMBOL (IEEE/IEC)



COMPARATORS 54/7485, LS85, S85

LOGIC DIAGRAM



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3, B_3	A_2, B_2	A_1, B_1	A_0, B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	A>B	A<B	A=B
$A_3 > B_3$	X	X	X	X	X	X	H	L	L
$A_3 < B_3$	X	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 > B_2$	X	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 < B_2$	X	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 > B_1$	X	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 < B_1$	X	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 > B_0$	X	X	X	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 < B_0$	X	X	X	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	L	L	H	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	H	L	L	H	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	X	X	H	L	L	H
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	H	H	L	L	L	L
$A_3 = B_3$	$A_2 = B_2$	$A_1 = B_1$	$A_0 = B_0$	L	L	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

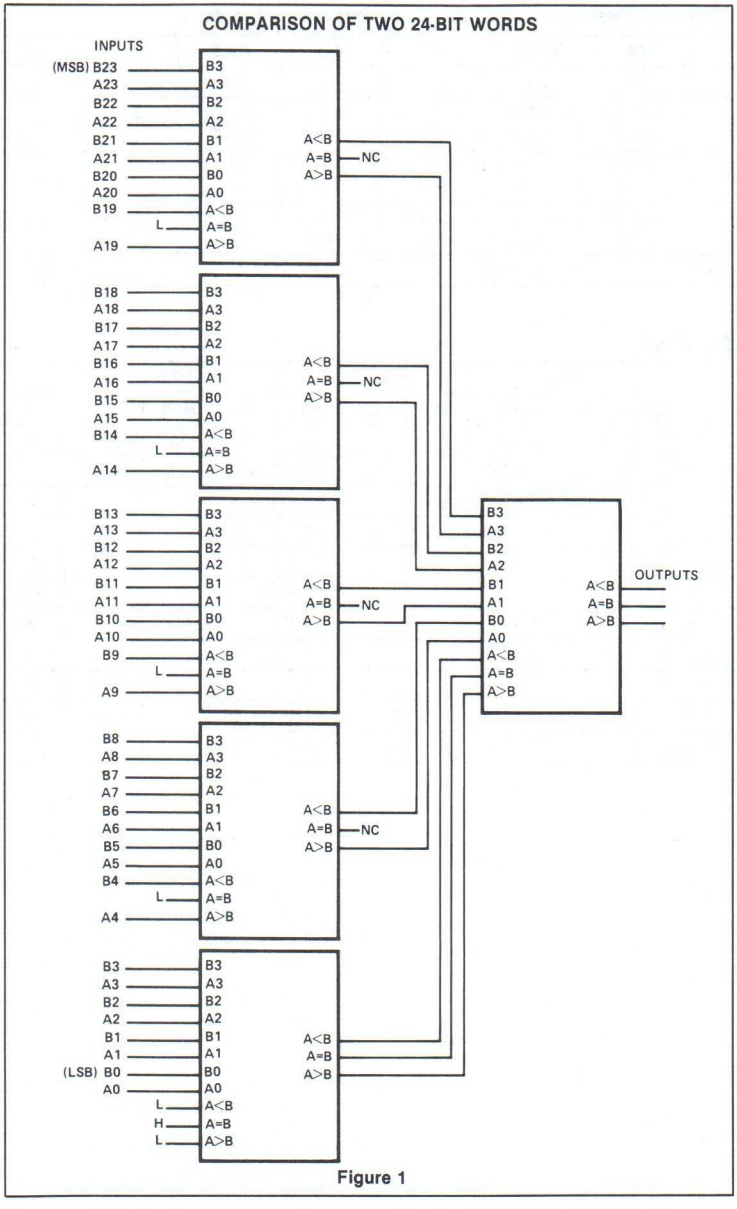


Figure 1

TABLE 1.

WORD LENGTH	NUMBER OF PACKAGES	TYPICAL SPEEDS		
		54/74	54S/74S	54LS/74LS
1-4 Bits	1	23ns	12ns	23ns
5-25 Bits	2-6	40ns	22ns	46ns
25-120 Bits	8-31	63ns	34ns	69ns

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−400			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7485			54/74LS85			54/74S85			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	$I_{A<B}$, $I_{A>B}$						0.1				mA
				Other inputs						0.3				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	$I_{A<B}$, $I_{A>B}$			40							μA
				Other Inputs			120							μA
			V_I = 2.7V	$I_{A<B}$, $I_{A>B}$						20			50	μA
				Other inputs						60			150	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	$I_{A<B}$, $I_{A>B}$			– 1.6			– 0.4				mA
				Other inputs			– 4.8			– 1.2				mA
			V_I = 0.5V	$I_{A<B}$, $I_{A>B}$									– 2.0	mA
				Other inputs									– 6.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				55	88		10.4	20		73	115	mA
		S54S85W only, T_A = 125°C											110	mA

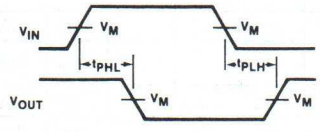
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the shorted circuit should not exceed one second.
4. I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5V.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

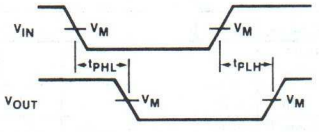
PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		54S/74S $C_L = 15pF$, $R_L = 280\Omega$		UNIT
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B input to A<B, A>B output	Waveform 1 3 logic levels		26 30		36 30		16 16.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B input to A = B output	Waveform 2 4 logic levels		35 30		45 45		18 16.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A<B}$ and $I_{A=B}$ input to A>B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A=B}$ input to A = B output	Waveform 2 2 logic levels		20 17		20 26		10.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay $I_{A>B}$ and $I_{A=B}$ input to A<B output	Waveform 1 1 logic level		11 17		22 17		7.5 8.5	ns

AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



WAVEFORM FOR NON-INVERTING OUTPUTS

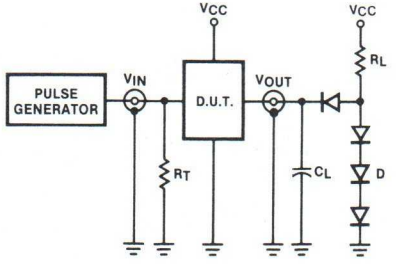


V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1 **Waveform 2**

TEST CIRCUITS AND WAVEFORMS

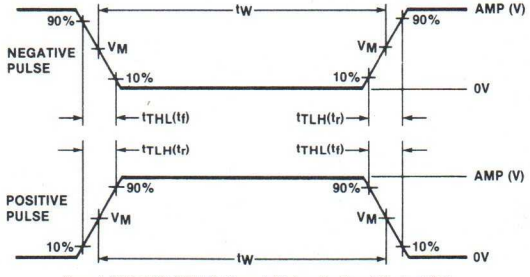
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad Two-Input Exclusive-OR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7486	14ns	30mA
74LS86	10ns	6.1mA
74S86	7ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7486N • N74LS86N N74S86N	
Ceramic DIP	N7486F • N74LS86F N74S86F	S5486F • S54LS86F S54S86F
Flatpack		S5486W • S54LS86W S54S86W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

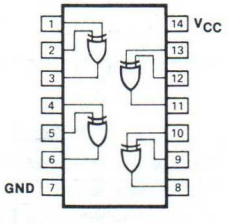
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

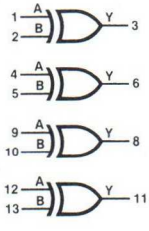
PINS	DESCRIPTION	54/74	54/74S	54/74LS
A, B	Inputs	1ul	1Sul	1LSul
Y	Output	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

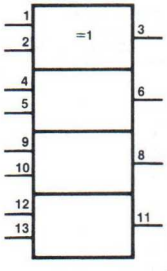
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

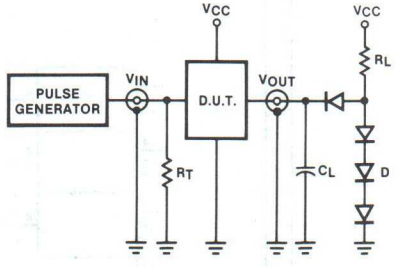
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

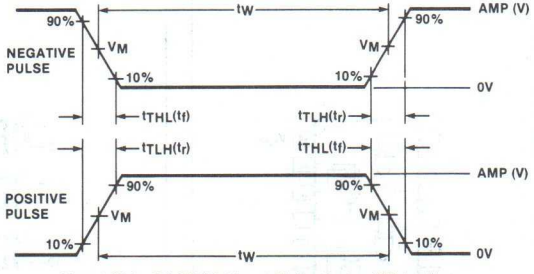
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

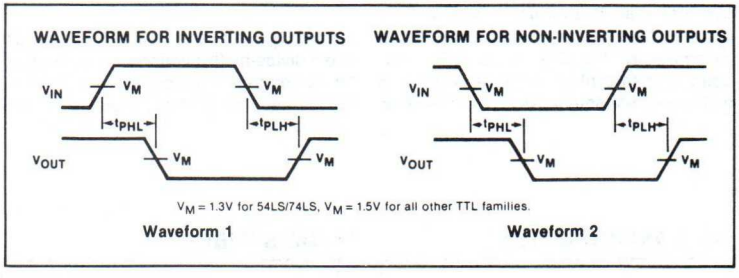
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7486			54/74LS86			54/74S86			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.2				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							40			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.8				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 15		– 100	– 40		– 100	mA
				Com'l	– 18		– 55	– 15		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		30	43		6.1	10		50	75	mA
				Com'l		30	50		6.1	10		50	75	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with inputs grounded and outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input LOW Waveform 2		23 17		23 17		10.5 10	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input HIGH Waveform 1		30 22		30 22		10.5 10	ns

COUNTERS

54/7490, LS90

Decade Counter

DESCRIPTION

The '90 is a 4-bit, ripple-type Decade Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the clocks and the MR inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count producing a BCD count sequence. In a symmetrical Bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the CP_1 input and a divide-by-ten square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain a divide-by-five operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7490	30MHz	30mA
74LS90	42MHz	9mA

ORDERING CODE

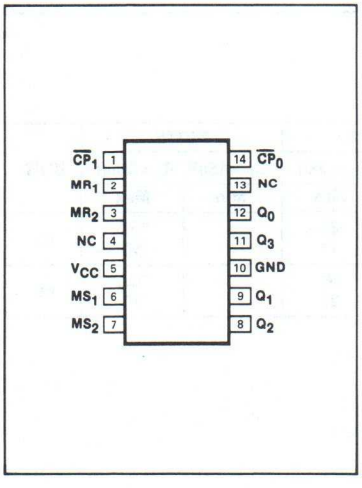
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7490N • N74LS90N	
Ceramic DIP	N7490F • N74LS90F	S54LS90F
Flatpack		S54LS90W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

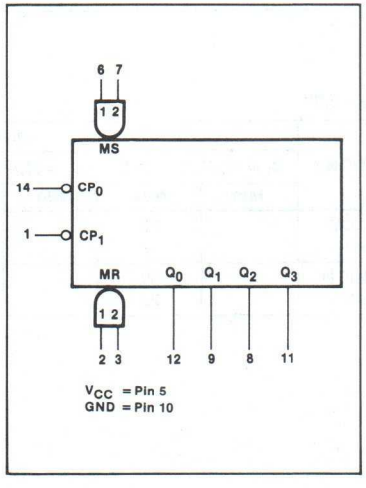
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}_0$	Input	2ul	6LSul
$\overline{CP}_1$	Input	4ul	8LSul
MR, MS	Inputs	1ul	1LSul
Q_0-Q_3	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

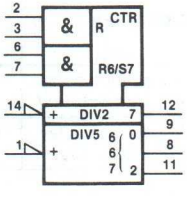
PIN CONFIGURATION



LOGIC SYMBOL

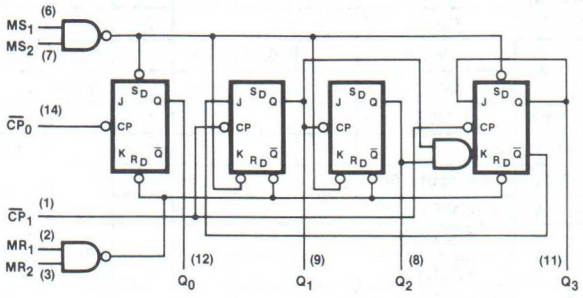


LOGIC SYMBOL (IEEE/IEC)



COUNTERS 54/7490, LS90

LOGIC DIAGRAM



MODE SELECTION— FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
H	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE— FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS

(Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

NOTE
V_{IN} is limited to +5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs on the 54/74LS90 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7490			54/74LS90			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All inputs '90			1.0				mA
			V_I = 7.0V	MR, MS inputs						0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ input						0.2	mA
				$\overline{CP}_1$ input						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	MR, MS inputs			40				μA
				$\overline{CP}_0$ input			80				μA
				$\overline{CP}_1$ input			160				μA
			V_I = 2.7V	MR, MS inputs						20	μA
				$\overline{CP}_0$ input[5]						40	μA
				$\overline{CP}_1$ input[5]						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	MR, MS inputs			– 1.6			– 0.4	mA
				$\overline{CP}_0$ input			– 3.2			– 2.4	mA
				$\overline{CP}_1$ input			– 6.4			– 3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		30	46		9	15	mA
				Com'l		30	53		9	15	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS90 only is 80μA for $\overline{CP}_0$ and 160μA for $\overline{CP}_1$ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		54/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	Min	Max	
f_{MAX} f_{MAX}	Input count frequency, $\overline{CP}_0$ to Q_0 Input count frequency, $\overline{CP}_1$ to Q_1	Waveform 1	10 10		32 16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		100 100		48 50	ns
t_{PHL}	MR input to any output	Waveform 2				40	ns
t_{PLH}	MS input to Q_0 and Q_3 outputs	Waveform 3				30	ns
t_{PHL}	MS input to Q_1 and Q_2 outputs	Waveform 2				40	ns

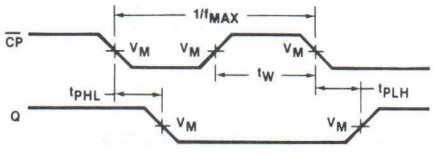
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

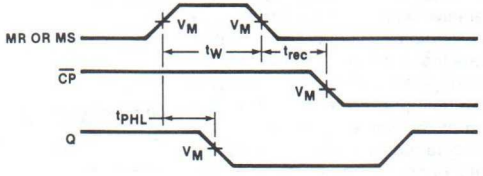
PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		30		ns
t_W	MS, MR pulse width	Waveform 2	50		15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2			25		ns
t_{rec}	Recover time, MS to $\overline{CP}$	Waveforms 2 & 3			25		ns

3

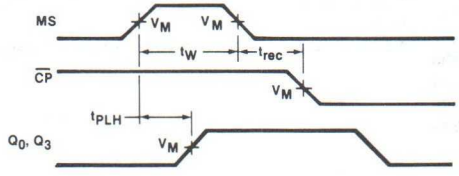
AC WAVEFORMS



Waveform 1



Waveform 2

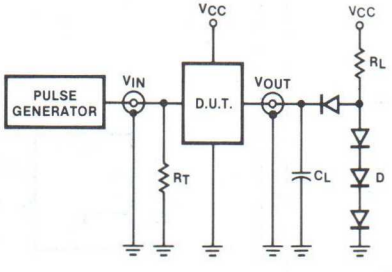


Waveform 3

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Function Table.

TEST CIRCUITS AND WAVEFORMS

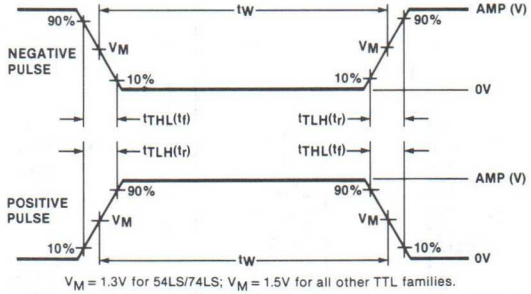
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

REGISTER 54/7491A

8-Bit Shift Register

- **8-bit serial-in-serial-out shift register**
- **Common buffered clock**
- **2-input gate for serial data entry**
- **True and Complement outputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7491A	18MHz	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7491AN	
Ceramic DIP	N7491AF	S5491AF
Flatpack		S5491AW

DESCRIPTION

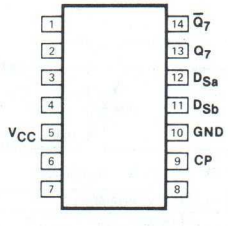
The '91A is an 8-bit serial-in-serial-out shift register. The serial data is entered through a 2-input AND gate (D_{Sa} and D_{Sb}). HIGH data is entered when both D_{Sa} and D_{Sb} are HIGH. LOW data is entered when either Serial Data input is LOW. The Data inputs are edge-triggered and must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock input (CP) for predictable operation. The data is shifted one bit to the right ($Q_0 \rightarrow Q_2 \cdots \rightarrow Q_7$) synchronous with each LOW-to-HIGH clock transition. The '91A has no reset capacity, so initialization requires the shifting in of at least 8 bits of known data. Once the register is fully loaded, the Q output follows the Serial inputs delayed by eight clock pulses. The Complement ($\overline{Q}$) output from the last stage is also available for simpler decoding applications.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

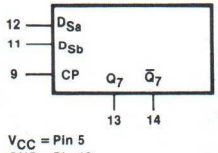
PINS	DESCRIPTION	54/74
All	Inputs	1ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

PIN CONFIGURATION

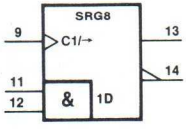


LOGIC SYMBOL



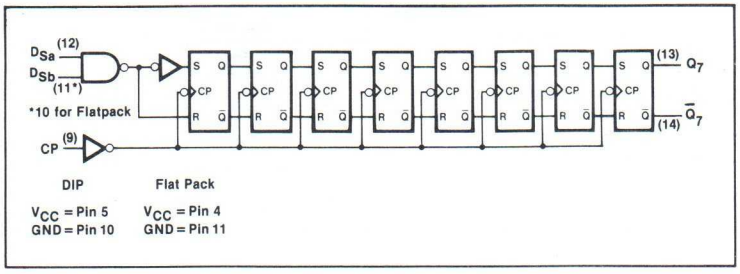
VCC = Pin 5
GND = Pin 10
Pin numbers for DIP package

LOGIC SYMBOL (IEEE/IEC)



REGISTER 54/7491A

LOGIC DIAGRAM



3

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			FIRST STAGE		OUTPUTS	
	CP	D_{Sa}	D_{Sb}	Q_0	$\bar{Q}_0$	Q_7	$\bar{Q}_7$
Shift, reset first stage	↑	l	X	L	H	q_6	$\bar{q}_6$
	↑	X	l	L	H	q_6	$\bar{q}_6$
Shift, set first stage	↑	h	h	H	L	q_6	$\bar{q}_6$

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced register output one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

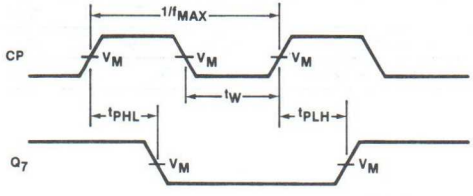
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/7491A			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	– 20		– 57	mA
			Com'l	– 18		– 57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Mil		35	50	mA
			Com'l		35	58	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All typical values are at V_{CC} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after the eighth clock pulse with the output open and D_{Sa} and D_{Sb} inputs grounded.

AC WAVEFORMS

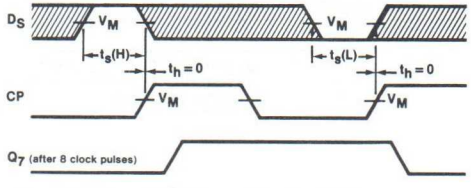
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 1

DATA SETUP AND HOLD TIMES



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	10		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		40 40	ns

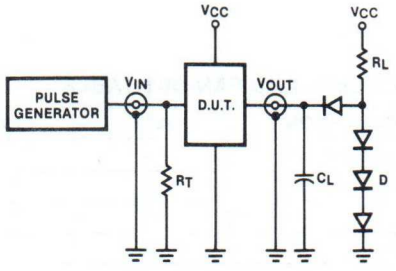
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	25		ns
t_s	Setup time, Data to clock	Waveform 2	25		ns
t_h	Hold time, Data to clock	Waveform 2	0		ns

TEST CIRCUITS AND WAVEFORMS

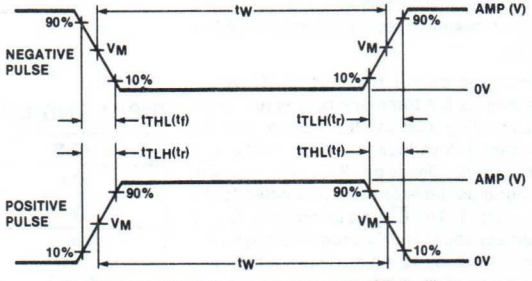
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS 54/7492, LS92

Divide-By-Twelve Counter

DESCRIPTION

The '92 is a 4-bit, ripple-type Divide-by-12 Counter. The device consists of four master-slave flip-flops internally connected to provide a divde-by-two section and a divide-by-six section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a Modulo-12, Divide-by-12 Counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-12 square wave output. In a divide-by-six counter no external connections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
7492	28MHz	28mA
74LS92	42MHz	9mA

ORDERING CODE

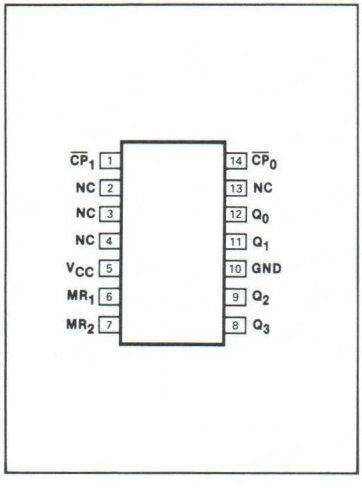
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7492N • N74LS92N	
Ceramic DIP	N7492F • N74LS92F	S54LS92F
Flatpack		S54LS92W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

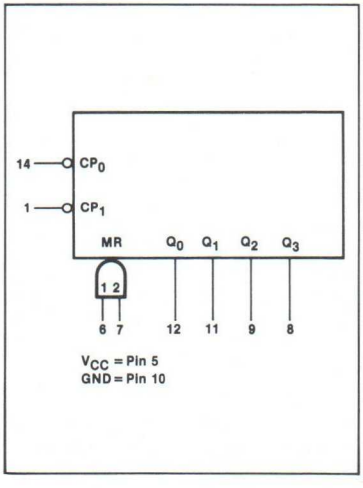
PINS	DESCRIPTION	54/74	54/74LS
MR	Master Reset inputs	1ul	1LSul
CP_0	Input	2ul	6LSul
CP_1	Input	4ul	8LSul
Q_0-Q_3	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

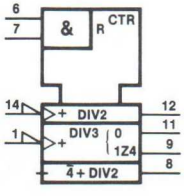
PIN CONFIGURATION



LOGIC SYMBOL

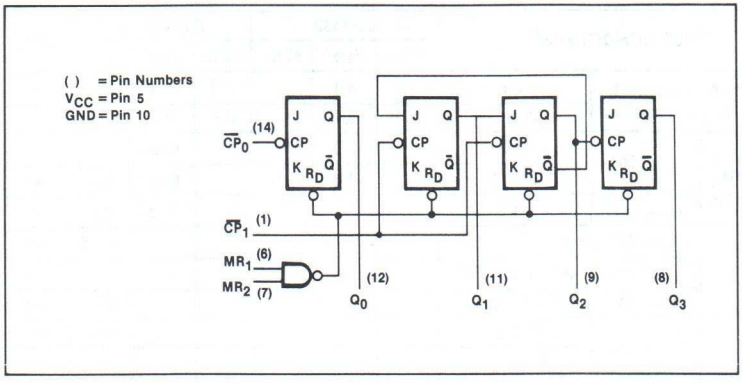


LOGIC SYMBOL (IEEE/IEC)



COUNTERS 54/7492, LS92

LOGIC DIAGRAM



FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

NOTE
V_{IN} is limited to +5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs on the 54/74LS92 only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7492			54/74LS92			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All inputs '92			1.0				mA
			V_I = 7.0V	MR inputs						0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ input						0.2	mA
				$\overline{CP}_1$ input						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	MR inputs			40				μA
				$\overline{CP}_0$ input			80				μA
				$\overline{CP}_1$ input			160				μA
			V_I = 2.7V	MR inputs						20	μA
				$\overline{CP}_0$ input[5]						40	μA
				$\overline{CP}_1$ input[5]						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	MR inputs			– 1.6			– 0.4	mA
				$\overline{CP}_0$ input			– 3.2			– 2.4	mA
				$\overline{CP}_1$ input			– 6.4			– 3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil			44		9	15	mA
				Com'l			51		9	15	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS92 only is 80μA for $\overline{CP}_0$ and 160μA for $\overline{CP}_1$ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		54/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	Min	Max	
f_{MAX}	$\overline{CP}_0$ input count frequency	Waveform 1	10		32		MHz
f_{MAX}	$\overline{CP}_1$ input count frequency	Waveform 1	10		16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		100 100		48 50	ns
t_{PHL}	$\overline{MR}$ input to any output	Waveform 2				40	ns

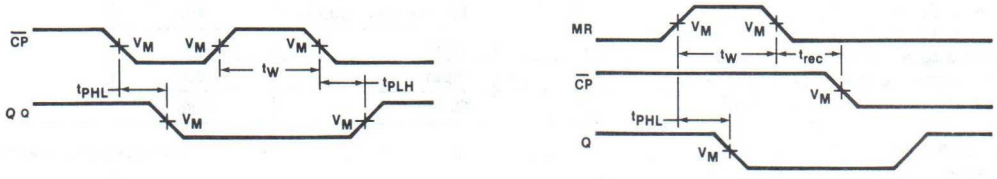
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		30		ns
t_W	MR pulse width	Waveform 2	50		15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2			25		ns

3

AC WAVEFORMS

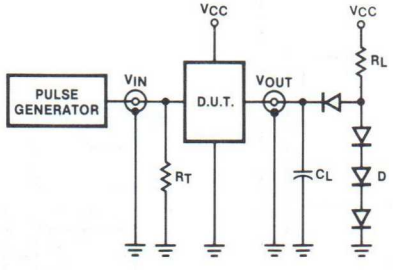


The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Function Table.

Waveform 1 **Waveform 2**

TEST CIRCUITS AND WAVEFORMS

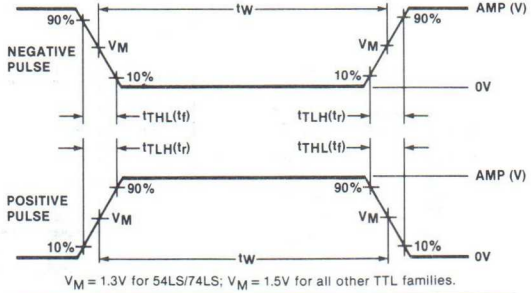
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS 54/7493, LS93

4-Bit Binary Ripple Counter

DESCRIPTION

The '93 is a 4-bit, ripple-type Binary Counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the Function Table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7493	40MHz	28mA
74LS93	42MHz	9mA

ORDERING CODE

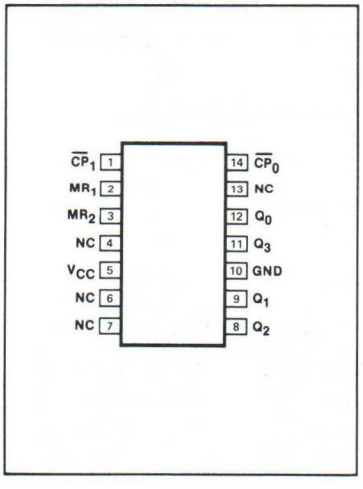
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7493N • N74LS93N	
Ceramic DIP	N7493F • N74LS93F	S5493F • S54LS93F
Flatpack		S5493W • S54LS93W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

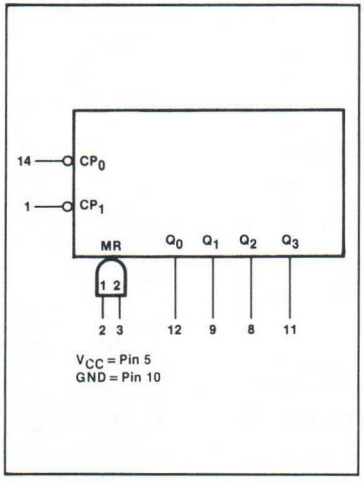
PINS	DESCRIPTION	54/74	54/74LS
MR	Master Reset inputs	1ul	1LSul
$\overline{CP}_0$	Input	2ul	6LSul
$\overline{CP}_1$	Input	2ul	4LSul
Q_0-Q_3	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

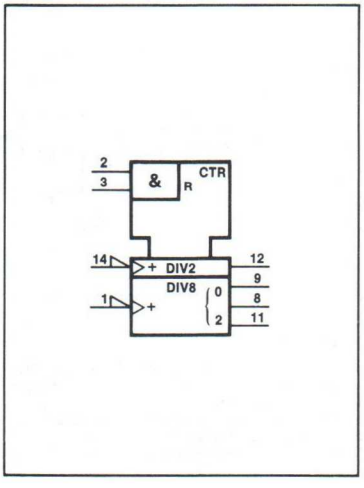
PIN CONFIGURATION



LOGIC SYMBOL

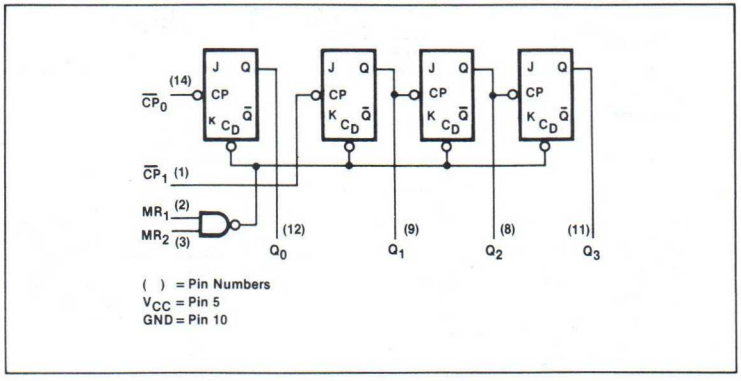


LOGIC SYMBOL (IEEE/IEC)



COUNTERS 54/7493, LS93

LOGIC DIAGRAM



( ) = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

NOTE
V_{IN} is limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs only on the 54/74LS93.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7493			54/74LS93			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	All inputs '93			1.0				mA
			V_I = 7.0V	MR inputs						0.1	mA
			V_I = 5.5V	$\overline{CP}_0$, $\overline{CP}_1$ inputs						0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	MR inputs			40				μA
				$\overline{CP}_0$, $\overline{CP}_1$ inputs			80				μA
			V_I = 2.7V	MR inputs						20	μA
				$\overline{CP}_0$, $\overline{CP}_1$ inputs[5]						40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	MR inputs			– 1.6			– 0.4	mA
				$\overline{CP}_0$ input			– 3.2			– 2.4	mA
				$\overline{CP}_1$ input			– 3.2			– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		28	46		9	15	mA
				Com'l		28	53		9	15	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS93 only is 80μA for $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX} f_{MAX}	$\overline{CP}_0$ input count frequency $\overline{CP}_1$ input count frequency	Waveform 1	10 10		32 16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1				16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1				16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1				32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1				51 51	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		135 135		70 70	ns
t_{PHL}	MR input to any output	Waveform 2				40	ns

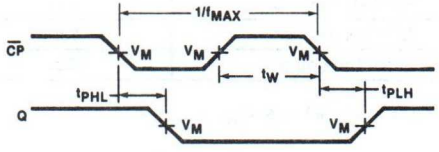
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	50		15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	50		30		ns
t_W	MR pulse width	Waveform 2	50		15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2			25		ns

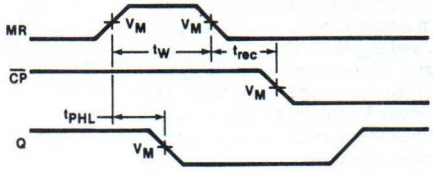
3

AC WAVEFORMS



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 1

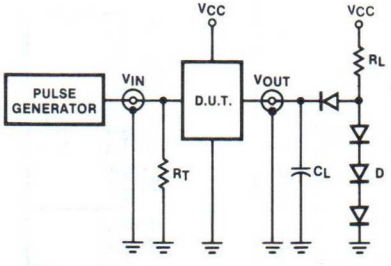


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 2

TEST CIRCUITS AND WAVEFORMS

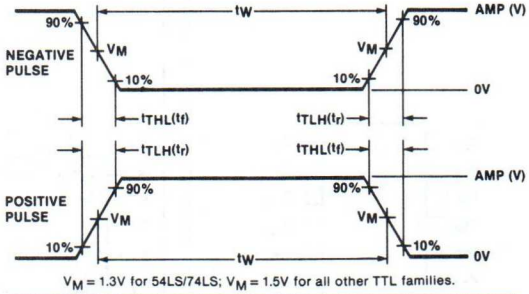
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER 54/7494

4-Bit Shift Register

- **4-bit parallel-to-serial converter**
- **Two asynchronous ones transfer parallel data ports**
- **Buffered active HIGH Master Reset**
- **Buffered positive edge-triggered clock**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
7494	25ns	35mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7494N	
Ceramic DIP	N7494F	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
PL_0, PL_1	Parallel Load inputs	4ul
D_S, D_n, CP, MR	All other inputs	1ul
Q_d	Serial Data output	10ul

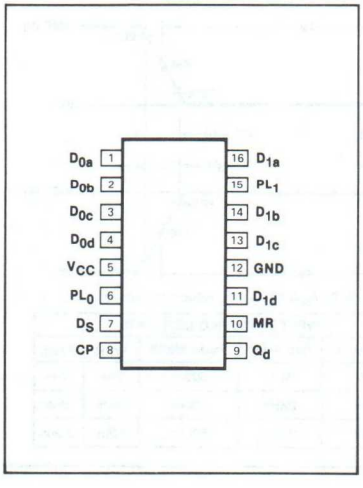
NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

DESCRIPTION

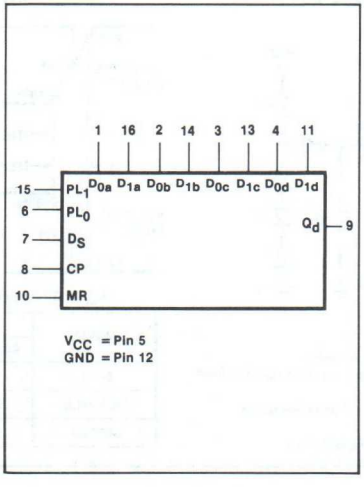
The '94 is a 4-bit shift register with serial and parallel (ones transfer) data entry. To facilitate parallel ones transfer from two sources, two Parallel Load inputs (PL_0 and PL_1) with associated Parallel Data inputs (D_{0a}-D_{0d} and D_{1a}-D_{1d}) are provided. To accommodate these extra inputs only the output of the last stage is available. The asynchronous Master Reset (MR) is active HIGH. When MR is HIGH, it overrides the clock and clears the register, forcing Q_d LOW.

Four flip-flops are connected so that shifting is synchronous; they change state when the clock goes from LOW-to-HIGH. Data is accepted at the serial D_S input prior to this clock transition. Two Parallel Load inputs and Parallel Data inputs allow an asynchronous ones transfer from two sources. The flip-flops can be set independently to the HIGH state when the appropriate Parallel input is activated. Parallel inputs D_{0a} through D_{0d} are activated during the time the PL_0 is HIGH and Parallel inputs D_{1a} through D_{1d} are activated when PL_1 is HIGH. If both sets of inputs are activated, a HIGH on either input will set the flip-flops to a HIGH. The register should not be clocked while the Parallel Load inputs are activated. The Parallel Load and Parallel Data inputs will override the MR if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

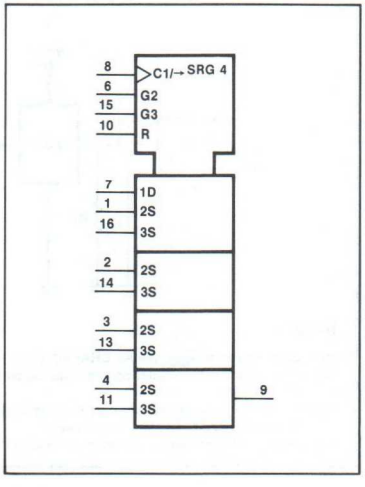
PIN CONFIGURATION



LOGIC SYMBOL

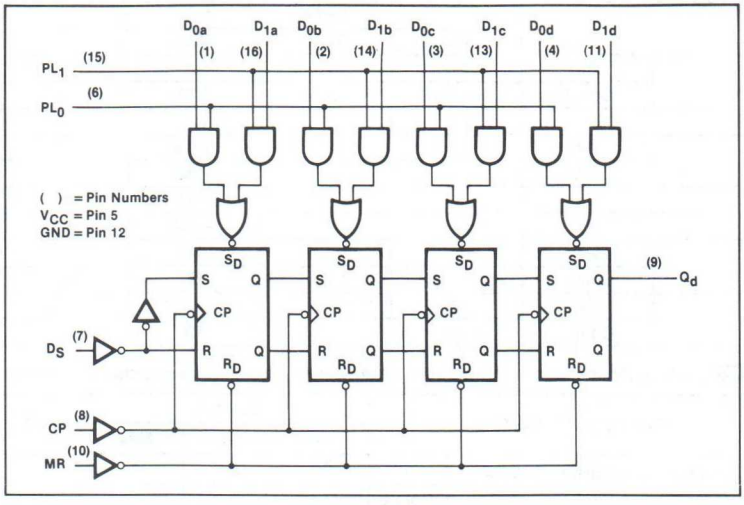


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/7494

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	PL_0	PL_1	D_{0n}	D_{1n}	MR	CP	D_S	Q_a	Q_b	Q_c	Q_d
Parallel load	H	L	L	X	X	X	X	Q_a	Q_b	Q_c	Q_d
	H	L	H	X	X	X	X	H	H	H	H
	L	H	X	L	X	X	X	Q_a	Q_b	Q_c	Q_d
	L	H	X	H	X	X	X	H	H	H	H
Reset (clear)	L	L	X	X	H	X	X	L	L	L	L
Shift right	L	L	X	X	L	↑	l	L	q_a	q_b	q_c
	L	L	X	X	L	↑	h	H	q_a	q_b	q_c

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 12	mA
I_{OH}	HIGH-level output current				− 400	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/7494			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'L	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		Mil		0.2	0.4	V
				Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	PL_0, PL_1 inputs				160	μA
			Other inputs				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	PL_0, PL_1 inputs				− 6.4	mA
			Other inputs				− 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	− 20		− 57	mA
				Com'l	− 18		− 57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		35	50	mA
				Com'l		35	58	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Parallel Load inputs grounded, Master Reset grounded following momentary application of 4.5V, all other inputs at 4.5V and outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	10		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		40 40	ns
t_{PLH}	Propagation delay Parallel Load or Parallel Data to output	Waveform 2		35	ns
t_{PHL}	Propagation delay MR to output	Waveform 2		40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SHIFT REGISTER 54/7494

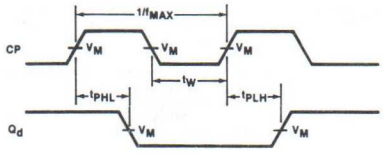
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		UNIT
			Min	Max	
$t_W(L)$	Clock pulse width, LOW	Waveform 1	35		ns
$t_W(H)$	MR pulse width, HIGH	Waveform 2	30		ns
$t_W(H)$	Parallel Load or Data pulse width, HIGH	Waveform 2	30		ns
$t_s(H)$	Setup time HIGH, D_S to CP	Waveform 3	35		ns
$t_s(L)$	Setup time LOW, D_S to CP	Waveform 3	25		ns
t_h	Hold time HIGH or LOW, D_S to CP	Waveform 3	0		ns

3

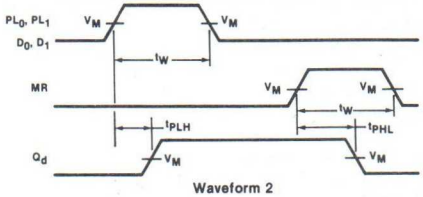
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

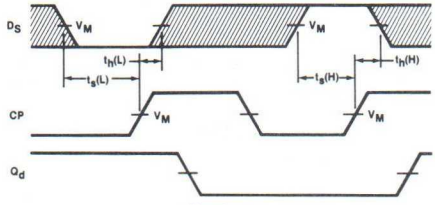
PARALLEL LOAD AND PARALLEL DATA TO OUTPUT DELAYS AND MASTER RESET TO OUTPUT DELAY



Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

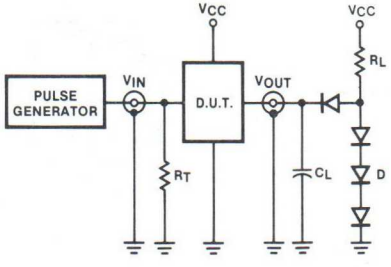
SERIAL DATA SETUP AND HOLD TIMES



Waveform 3

TEST CIRCUITS AND WAVEFORMS

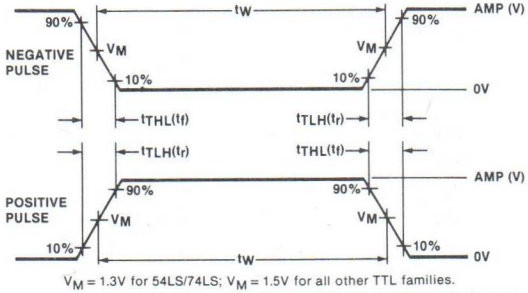
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTERS 54/7495, LS95B

4-Bit Shift Register

- **Separate negative-edge-triggered shift and parallel load clocks**
- **Common mode control input**
- **Shift right serial input**
- **Synchronous shift or load capabilities**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
7495	36MHz	39mA
74LS95B	36MHz	13mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7495N • N74LS95BN	
Ceramic DIP	N7495F • N74LS95BF	S5495F • S54LS95BF
Flatpack		S5495W • S54LS95BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
S	Input	2ul	1LSul
Other	Inputs	1ul	1LSul
Q	Output	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

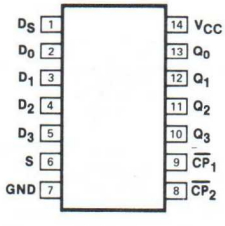
DESCRIPTION

The '95 is a 4-Bit Shift Register with serial and parallel synchronous operating modes. It has serial Data (D_S) and four parallel Data (D_0-D_3) inputs and four Parallel outputs (Q_0-Q_3). The serial or parallel mode of operation is controlled by a Mode Select input (S) and two Clock inputs ($\overline{CP}_1$ and $\overline{CP}_2$). The serial (shift right) or parallel data transfers occur synchronously with the HIGH-to-LOW transition of the selected Clock input.

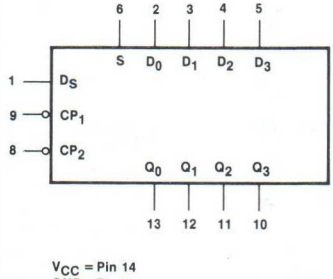
When the Mode Select input (S) is HIGH, $\overline{CP}_2$ is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_2$ loads parallel data from the D_0-D_3 inputs into the register. When S is LOW, CP_1 is enabled. A HIGH-to-LOW transition on enabled $\overline{CP}_1$ shifts the data from Serial input D_S to Q_0 and transfers the data in Q_0 to Q_1, Q_1 to Q_2, and Q_2 to Q_3 respectively (shift right). Shift left is accomplished by externally connecting Q_3 to D_2, Q_2 to D_1, Q_1 to D_0, and operating the '95 in the parallel mode (S = HIGH).

In normal operations the Mode Select (S) should change states only when both Clock inputs are LOW. However, changing S from HIGH-to-LOW while $\overline{CP}_2$ is LOW, or changing S from LOW-to-HIGH while $\overline{CP}_1$ is LOW will not cause any changes on the register outputs.

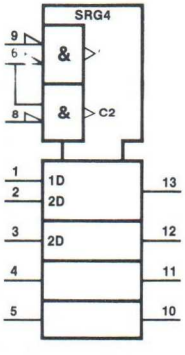
PIN CONFIGURATION



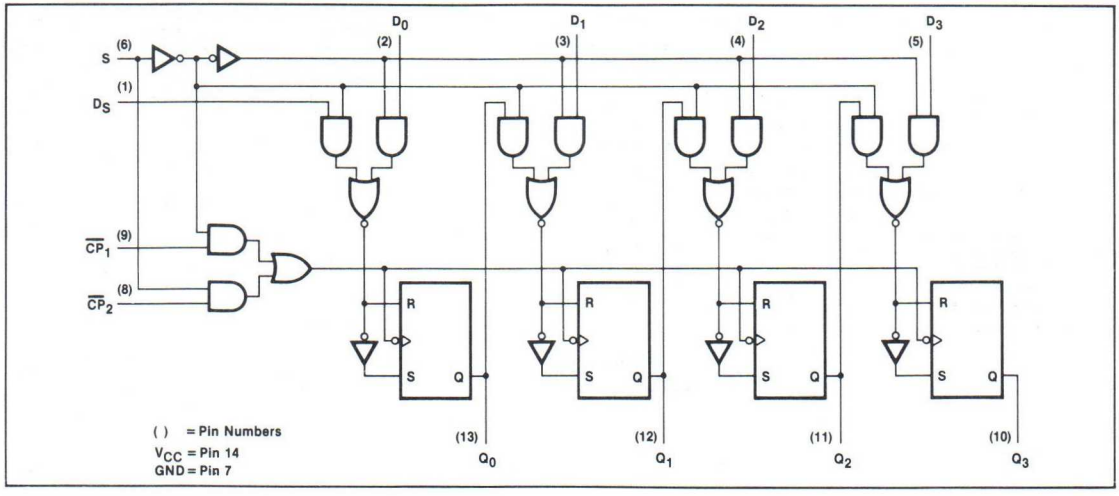
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	+0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	S	CP_1	CP_2	D_S	D_N	Q_0	Q_1	Q_2	Q_3
Parallel load	H	X	↓	X	l	L	L	L	L
	H	X	↓	X	h	H	H	H	H
Shift right	L	↓	X	l	X	L	q_0	q_1	q_2
	L	↓	X	h	X	H	q_0	q_1	q_2
Mode change	↑	L	X	X	X	no change			
	↑	H	X	X	X	undetermined			
	↓	X	L	X	X	no change			
	↓	X	H	X	X	undetermined			

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition.
X = Don't care.
↓ = HIGH-to-LOW transition of Clock or Mode Select.
↑ = LOW-to-HIGH transition of Mode Select.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7495			54/74LS95B			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	S input			80				μA
				Other inputs			40				μA
			V_I = 2.7V	S input						20	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	S input			– 3.2			– 0.4	mA
				Other inputs			– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 18		– 57	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				39	63		13	21	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Serial Data input and all outputs open; Parallel Data inputs grounded; Mode Select input at 4.5V and a momentary 3V, then ground, applied to the Clock inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 32		27 32	ns

NOTE

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

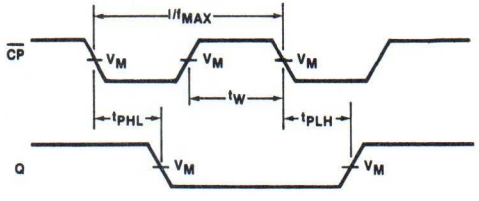
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width, HIGH	Waveform 1	20		25		ns
t_s	Setup time, Data to Clock	Waveform 2	15		20		ns
t_h	Hold time, Data to Clock	Waveform 2	0		10		ns
$t_{en}(L)$	Enable time, LOW mode Select to $\overline{CP}_1$	Waveform 3	30		20		ns
$t_{en}(H)$	Enable time, HIGH mode Select to $\overline{CP}_2$	Waveform 3	30		20		ns
$t_{inh}(H)$	Inhibit time, HIGH mode Select to $\overline{CP}_1$ (L→H)	Waveform 3	5		20		ns
$t_{inh}(L)$	Inhibit time, LOW Mode Select to $\overline{CP}_2$ (L→H)	Waveform 3	5		20		ns

3

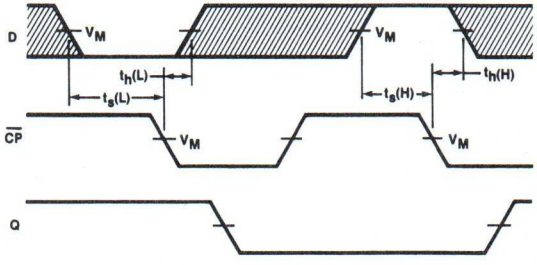
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



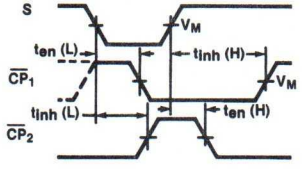
Waveform 1

DATA SETUP AND HOLD TIMES



Waveform 2

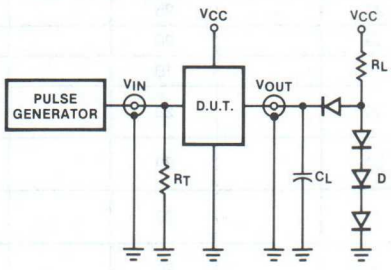
V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded ares indicate when the input is permitted to change for predictable output performance.



Waveform 3

TEST CIRCUITS AND WAVEFORMS

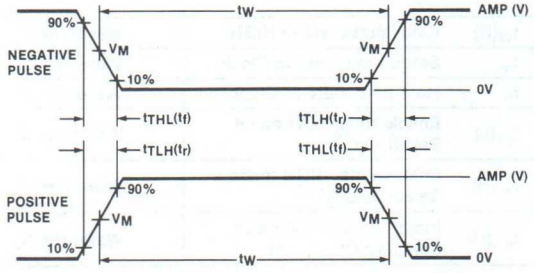
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTERS 54/7496, LS96

5-Bit Shift Register

- 5-bit parallel-to-serial or serial-to-parallel converter
- Asynchronous ones transfer preset entry
- Buffered positive-triggered clock
- Buffered active LOW Clear

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
7496	25ns	48mA
74LS96	25ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N7496N • N74LS96N	
Ceramic DIP	N7496F • N74LS96F	S5496F • S54LS96F
Flatpack		S5496W • S54LS96W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
Preset Enable	Inputs	5ul	5LSul
All other	Inputs	1ul	1LSul
Q	Outputs	10ul	10LSul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

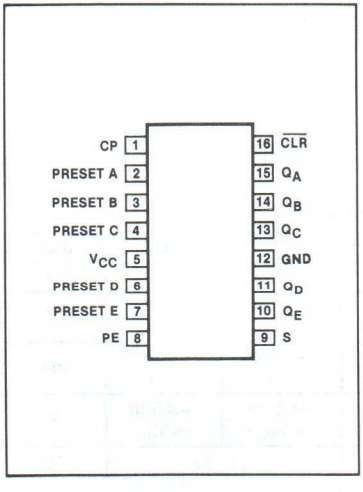
The '96 is a 5-bit shift register with both serial and parallel (ones transfer) data entry. Since the '96 has the output of each stage available as well as a D-type serial input and ones transfer inputs on each stage, it can be used in 5-bit serial-to-parallel, serial-to-serial and some parallel-to-serial data operations.

The '96 is five master/slave flip-flops connected to perform right shift. The flip-flops change state on the LOW-to-HIGH transition of the clock. The Serial (S) input is edge-triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

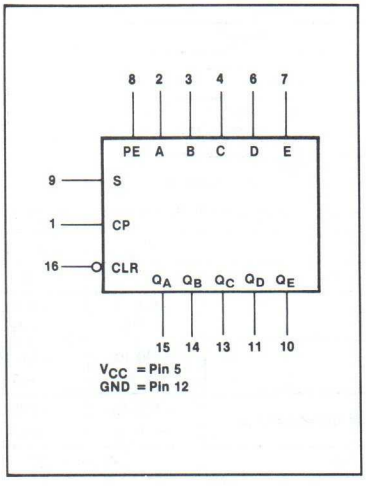
Each flip-flop has asynchronous set inputs, allowing them to be independently set HIGH. The set inputs are controlled by a common active HIGH Preset Enable (PE) input. The PE input is not buffered, and care must be taken not to overload the driving element. When the PE is HIGH, a HIGH on the Preset (A-E) inputs will set the associated flip-flops HIGH. A LOW on the A-E inputs will cause "no change" in the appropriate flip-flops.

The asynchronous active LOW Clear ($\overline{CLR}$) is buffered. When LOW, the $\overline{CLR}$ overrides the clock and clears the register if the PE is not active. The Preset inputs override the $\overline{CLR}$, forcing the flip-flops HIGH if both are activated simultaneously. However, for predictable operation, both signals should not be deactivated simultaneously.

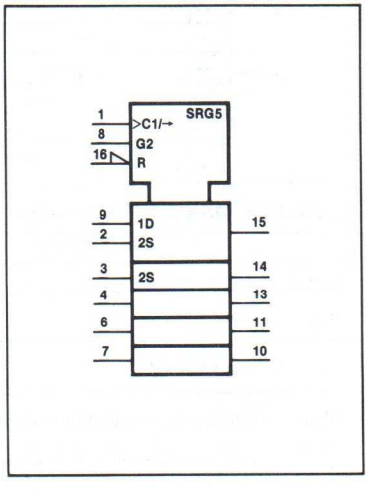
PIN CONFIGURATION



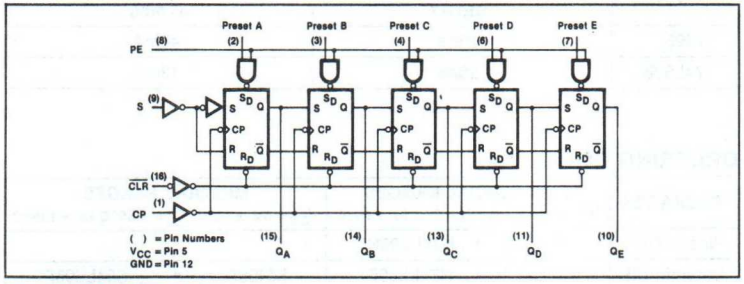
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



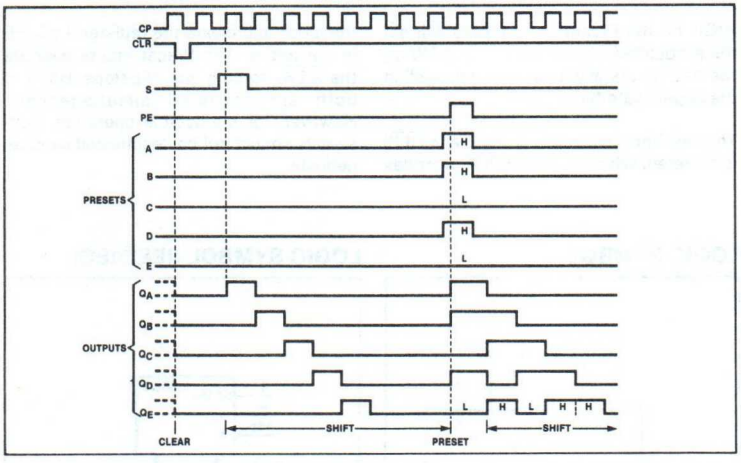
FUNCTION TABLE

INPUTS								OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	PRESET B	PRESET C	PRESET D	PRESET E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = HIGH voltage level, (steady state)
L = LOW voltage level (steady state)
X = Irrelevant (any input, including transitions)
↑ = Transition from LOWt-to-HIGH level

Q_{A0}, Q_{B0}, etc = The level of Q_A, Q_B, ect, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = The level of Q_A, Q_B, etc, respectively before the most recent ↑ transition of the clock.

TYPICAL CLEAR, SHIFT, PRESET, AND SHIFT SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7	V
		Com'l			+ 0.8			+ 0.8	V
I_{IK}	Input clamp current				− 12			− 18	mA
I_{OH}	HIGH-level output current				− 400			− 400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	− 55		+ 125	°C
		Com'l	0		70	0		70	°C

3

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/7496			54/74LS96			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	PE inputs						0.5	mA
				Other inputs						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	PE inputs			200				μA
				Other inputs			40				μA
			V_I = 2.7V	PE inputs						100	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX V_I = 0.4V		PE inputs			− 8			− 2	mA
				Other inputs			− 1.6			− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	− 20		− 57	− 20		− 100	mA
				Com'l	− 18		− 57	− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		48	68		12	20	mA
				Com'l		48	79		12	20	mA

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Clear grounded and all other inputs and outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	10		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		40 40		40 40	ns
t_{PLH}	Propagation delay Preset or Preset Enable to output	Waveform 2		35		35	ns
t_{PHL}	Propagation delay $\overline{CLR}$ to output	Waveform 2		55		55	ns

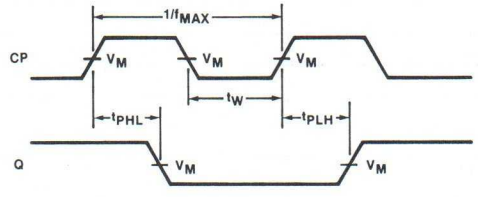
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width, LOW	Waveform 1	35		20		ns
$t_W(L)$	$\overline{CLR}$ pulse width, LOW	Waveform 2	30		30		ns
$t_W(H)$	Preset or Preset Enable pulse width, HIGH	Waveform 2	30		30		ns
t_s	Setup time, S to CP	Waveform 3	30		30		ns
t_h	Hold time, S to CP	Waveform 3	0		0		ns

AC WAVEFORMS

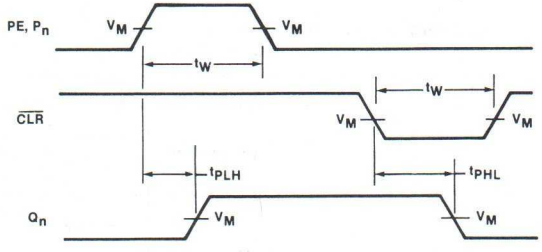
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

Waveform 1

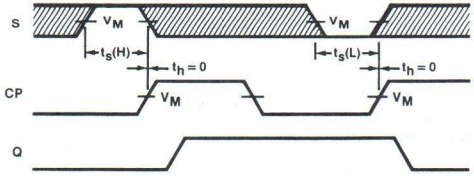
PARALLEL LOAD AND PARALLEL DATA TO OUTPUT DELAYS AND MASTER RESET TO OUTPUT DELAY



$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

Waveform 2

DATA SETUP AND HOLD TIME

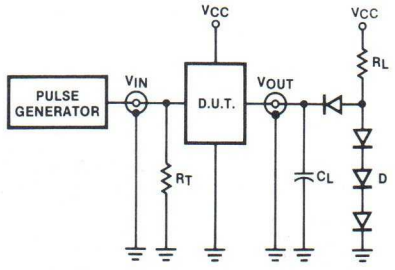


$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

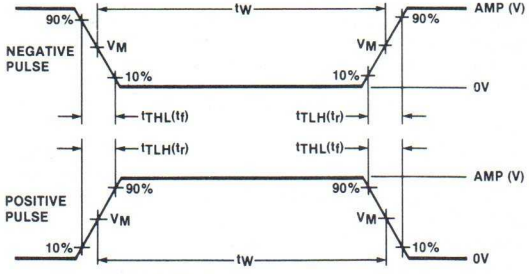
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

FLIP-FLOPS 54/74107, LS107

Dual J-K Flip-Flop

DESCRIPTION

The '107 is a dual flip-flop with individual J, K, Clock and direct Reset inputs. The 74107 is a positive pulse-triggered flip-flop. JK information is loaded into the master while the Clock is HIGH and transferred to the slave on the HIGH-to-LOW Clock transition. For these devices the J and K inputs should be stable while the Clock is HIGH for conventional operation.

The 74LS107 is a negative edge-triggered flip-flop. The J and K inputs must be stable one setup time prior to the HIGH-to-LOW Clock transition for predictable operation.

The Reset ($\overline{R}_D$) is an asynchronous active LOW input. When LOW, it overrides the Clock and Data inputs, forcing the Q output LOW and the $\overline{Q}$ output HIGH.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74107	20MHz	20mA
74LS107	45MHz	4mA

ORDERING CODE

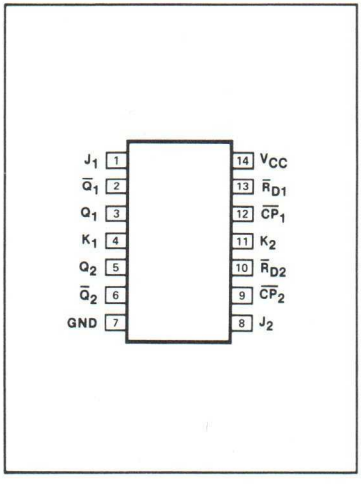
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74107N • N74LS107N	
Ceramic DIP	N74107F • N74LS107F	S54LS107F
Flatpack		S54LS107W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

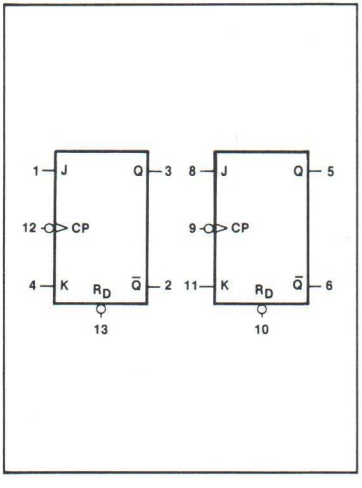
PINS	DESCRIPTION	54/74	54/74LS
$\overline{CP}$	Clock input	2ul	4LSul
$\overline{R}_D$	Reset input	2ul	3LSul
J, K	Data inputs	1ul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

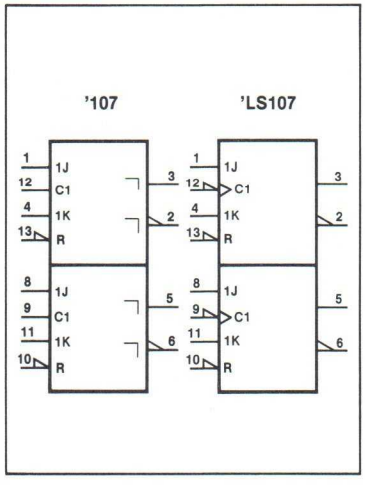
PIN CONFIGURATION



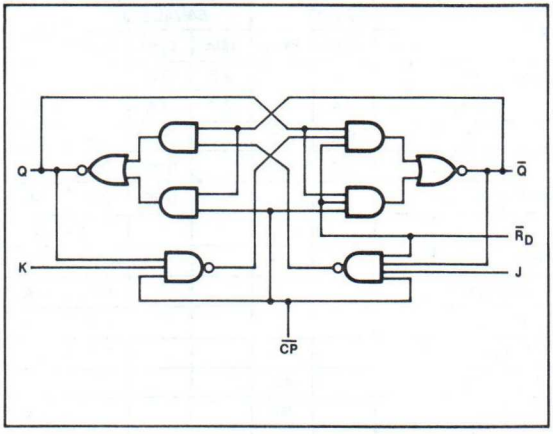
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{R}_D$	$\overline{CP}$[b]	J	K	Q	$\overline{Q}$
Asynchronous Reset (Clear)	L	X	X	X	L	H
Toggle	H	⎍	h	h	$\overline{q}$	q
Load "0" (Reset)	H	⎍	l	h	L	H
Load "1" (Set)	H	⎍	h	l	H	L
Hold "no change"	H	⎍	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.[b]
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.[b]
q = Lower case letters indicate the state of the referenced output prior to the HIGH-to-LOW Clock transition.
X = Don't care.
⎍ = Positive Clock pulse.

NOTES
a. The J and K inputs of the 54/74107 must be stable while the Clock is HIGH for conventional operation.
b. The 54/74LS107 is edge-triggered. Data must be stable one setup time prior to the negative edge of the Clock for predictable operation.

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74107			54/74LS107			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	J, K Inputs						0.1	mA
				$\overline{R}_D$ Inputs						0.3	mA
				$\overline{CP}$ Inputs						0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	J, K Inputs			40				μA
				$\overline{R}_D$ Inputs			80				μA
				$\overline{CP}$ Inputs			80				μA
			V_I = 2.7V	J, K Inputs						20	μA
				$\overline{R}_D$ Inputs						60	μA
				$\overline{CP}$ Inputs						80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		J, K Inputs			– 1.6			– 0.4	mA
				$\overline{R}_D$ Inputs			– 3.2			– 0.8	mA
				$\overline{CP}$ Inputs			– 3.2			– 0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX					40			8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 3	15		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Output	Waveform 1, 'LS107 Waveform 3, '107		25 40		20 30	ns
t_{PLH} t_{PHL}	Propagation delay Reset to Output	Waveform 2		25 40		20 30	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

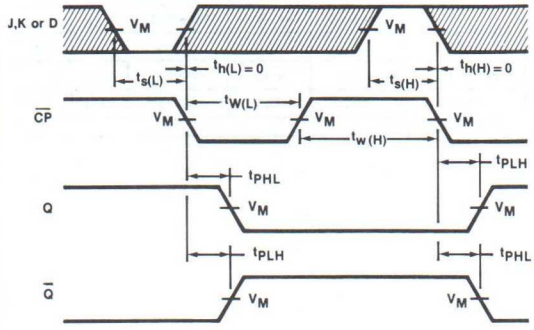
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		20		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	47		13		ns
$t_W(L)$	Reset pulse width (LOW)	Waveform 2	25		25		ns
t_s	Setup time J or K to Clock[b]	Waveform 1	0		20		ns
t_h	Hold time J or K to Clock	Waveform 1	0		0		ns

3

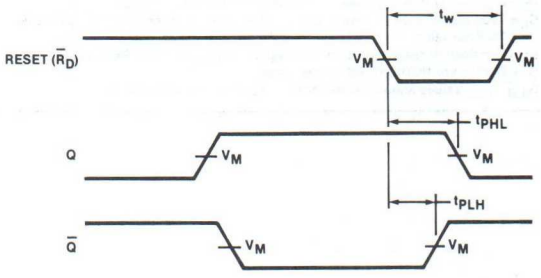
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



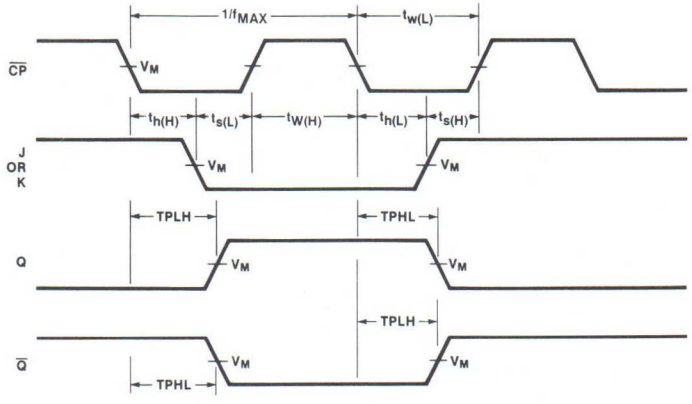
Waveform 1

RESET TO OUTPUT DELAYS, RESET PULSE WIDTHS



Waveform 2

PROPAGATION DELAY AND f_{MAX}

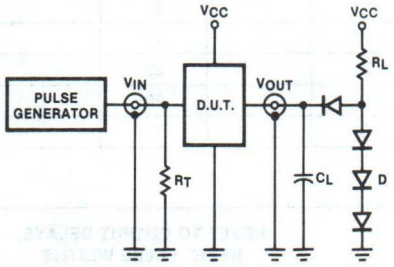


Waveform 3

$V_M = 1.3V$ for 54LS/74S: $V_M = 1.5V$ for all other TTL famillies.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

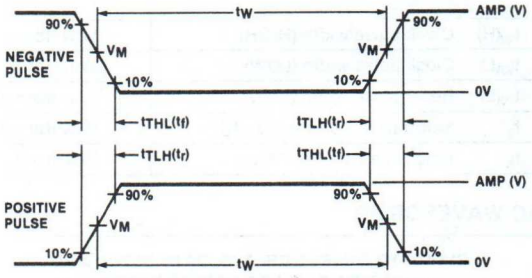
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual J-$\overline{K}$ Positive Edge-Triggered Flip-Flop

DESCRIPTION

The '109 is a dual positive edge-triggered J$\overline{K}$-type flip-flop featuring individual J, $\overline{K}$, Clock, Set and Reset inputs; also complementary Q and $\overline{Q}$ outputs.

Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) are asynchronous active LOW inputs and operate independently of the Clock input.

The J and $\overline{K}$ are edge-triggered inputs which control the state changes of the flip-flops as described in the Mode Select-Truth Table.

The J and $\overline{K}$ inputs must be stable just one setup time prior to the LOW-to-HIGH transition of the Clock for predictable operation. The J$\overline{K}$ design allows operation as a D flip-flop by tying the J and $\overline{K}$ inputs together.

Although the Clock input is level sensitive, the positive transition of the Clock pulse between the 0.8V and 2.0V levels should be equal to or less than the Clock to output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74109	33MHz	9mA
74LS109	33MHz	4mA

3

ORDERING CODE

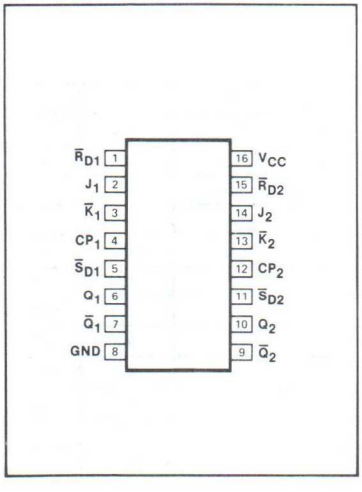
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74109N • N74LS109N	
Ceramic DIP	N74109F • N74LS109F	S54109F • S54LS109F
Flatpack		S54109W • S54LS109W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

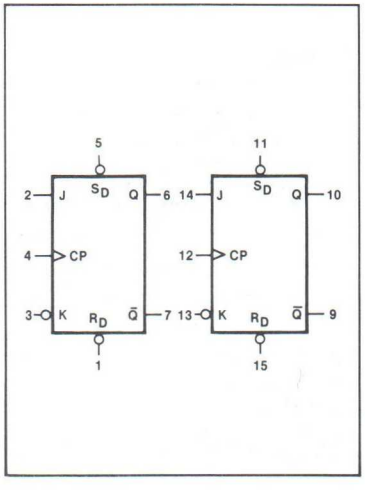
PINS	DESCRIPTION	54/74	54/74LS
CP	Clock input	2ul	1LSul
$\overline{R}_D$	Reset input	4ul	2LSul
$\overline{S}_D$	Set input	2ul	2LSul
J, $\overline{K}$	Data inputs	1ul	1LSul
Q, $\overline{Q}$	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

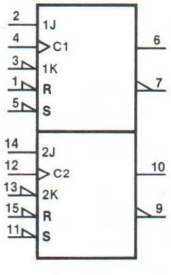
PIN CONFIGURATION



LOGIC SYMBOL

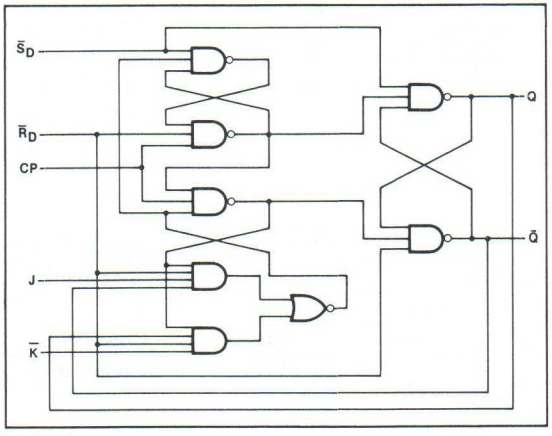


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS 54/74109, LS109

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined (Note)	L	L	X	X	X	H	H
Toggle	H	H	↑	h	l	$\overline{q}$	q
Load "0" (Reset)	H	H	↑	l	l	L	H
Load "1" (Set)	H	H	↑	h	h	H	L
Hold "no change"	H	H	↑	l	h	q	$\overline{q}$

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH Clock transition.
↑ = LOW-to-HIGH Clock transition.

NOTE
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74109			54/74LS109			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	J, $\overline{K}$ Inputs						0.1	mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs						0.2	mA
				CP Inputs						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	J, $\overline{K}$ Inputs			40				μA
				$\overline{R}_D$ Inputs			160				μA
				$\overline{S}_D$, CP Inputs			80				μA
			V_I = 2.7V	J, $\overline{K}$ Inputs						20	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs						40	μA
				CP Inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		J, $\overline{K}$ Inputs			− 1.6			− 0.4	mA
				$\overline{R}_D$ Inputs			− 4.8			− 0.8	mA
				$\overline{S}_D$ Inputs			− 3.2			− 0.8	mA
				CP Inputs			− 3.2			− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 30		− 85	− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				9	30		4	8	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		54/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		16 28		25 40	ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Waveform 2		15 25		25 40	ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		15 35		25 40	ns

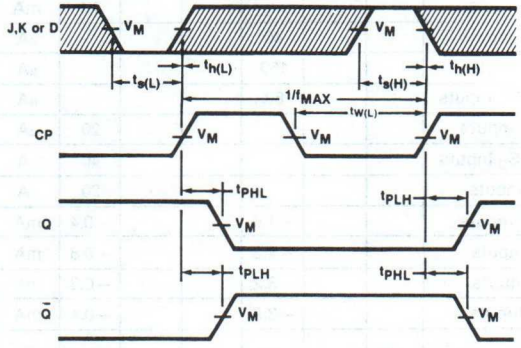
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		25		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	20		15		ns
$t_W(L)$	Set or Reset pulse width (LOW)	Waveform 2	20		25		ns
t_s	Setup time J or K to Clock	Waveform 1	10		20		ns
t_h	Hold time J or K to Clock	Waveform 1	6.0		5.0		ns

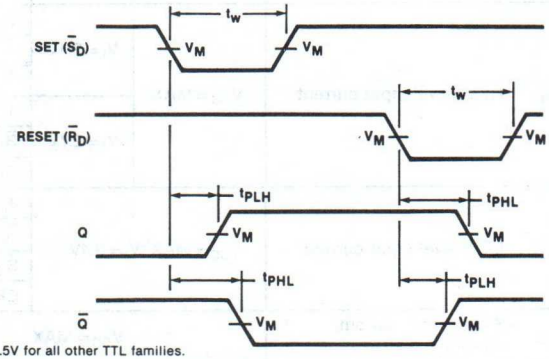
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

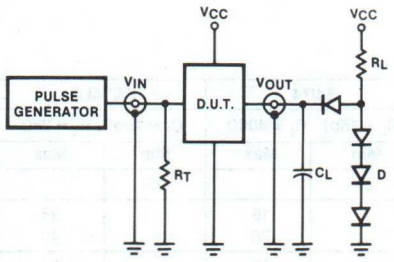


Waveform 2

$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

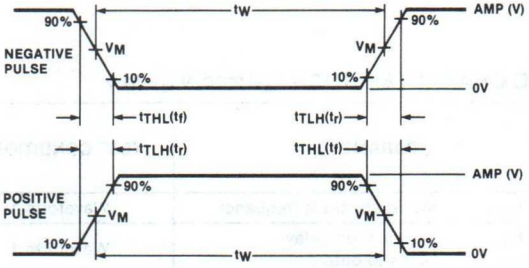
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOPS 54/74LS112, S112

Dual J-K Edge-Triggered Flip-Flop

DESCRIPTION

The '112 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Clock, Set and Reset inputs. The Set ($\overline{S}_D$) and Reset ($\overline{R}_D$) inputs, when LOW, set or reset the outputs as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS112	45MHz	4mA
74S112	125MHz	15mA

ORDERING CODE

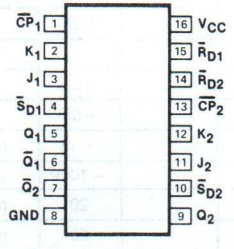
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S112N • N74LS112N	
Ceramic DIP	N74S112F • N74LS112F	S54S112F • S54LS112F
Flatpack		S54S112W • S54LS112W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

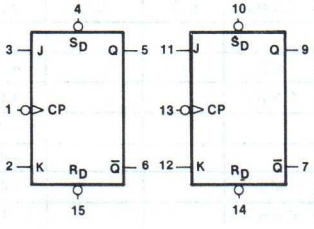
PINS	DESCRIPTION	54/74S	54/74LS
$\overline{CP}$	Clock input	2Sul	4LSul
$\overline{R}_D$, $\overline{S}_D$	Reset and Set inputs	3.5Sul	3LSul
J, K	Data inputs	1Sul	2LSul
Q, $\overline{Q}$	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

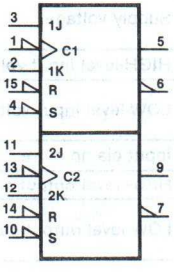
PIN CONFIGURATION



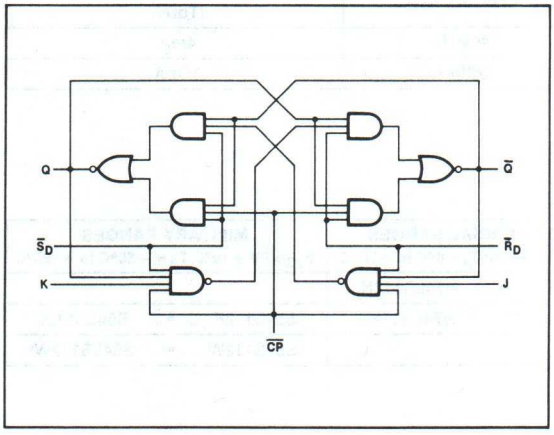
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	H	X	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	H
Toggle	H	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	H	↓	l	h	L	H
Load "1" (Set)	H	H	↓	h	l	H	L
Hold "no change"	H	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.

NOTE
Both outputs will be HIGH while both $\overline{S}_D$ and $\overline{R}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{R}_D$ go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to −7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS112			54/74S112			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V	J, K Inputs			0.1				mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			0.3				mA
				$\overline{CP}$ Inputs			0.4				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	J, K Inputs			20			50	μA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			60			100	μA
				$\overline{CP}$ Inputs			80			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	J, K Inputs			– 0.4				mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs			– 0.8				mA
				CP Inputs			– 0.8				mA
			V_I = 0.5V	J, K Inputs						– 1.6	mA
				$\overline{R}_D$, $\overline{S}_D$ Inputs						– 7	mA
				$\overline{CP}$ Inputs						– 4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				4	8		15	50	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS C_L = 15pF, R_L = 2kΩ		54/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		20 30		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}_D$ or $\overline{R}_D$ to output	Waveform 2		20 30		7.0 7.0	ns

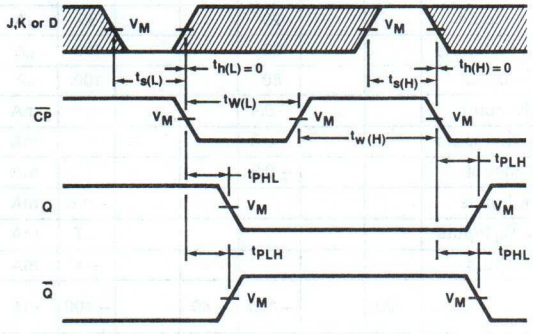
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_W(L)$	Set or Reset pulse width (LOW)	Waveform 2	25		8.0		ns
t_s	Setup time J or K to Clock	Waveform 1	20		3.0		ns
t_h	Hold time J or K to Clock	Waveform 1	0		0		ns

AC WAVEFORMS

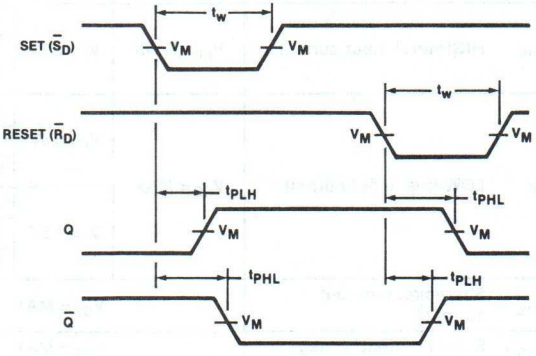
CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

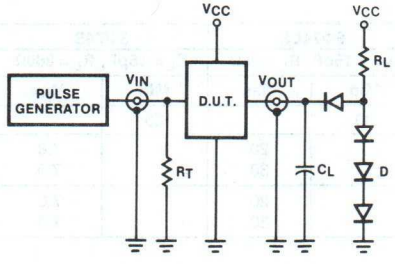


$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.

Waveform 2

TEST CIRCUITS AND WAVEFORMS

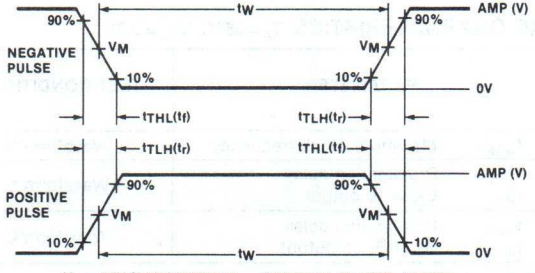
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual J-K Edge-Triggered Flip-Flop

DESCRIPTION

The '113 is a dual J-K negative edge-triggered flip-flop featuring individual J, K, Set and Clock inputs. The asynchronous Set ($\overline{S}_D$) input, when LOW, forces the outputs to the steady state levels as shown in the Function Table regardless of the levels at the other inputs.

A HIGH level on the Clock ($\overline{CP}$) input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change while the $\overline{CP}$ is HIGH and the flip-flop will perform according to the Function Table as long as minimum setup and hold times are observed. Output state changes are initiated by the HIGH-to-LOW transition of $\overline{CP}$.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS113	45MHz	4mA
74S113	125MHz	15mA

ORDERING CODE

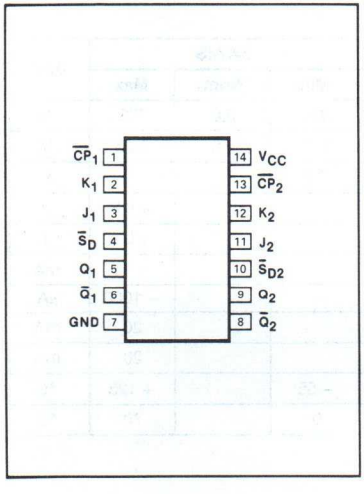
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S113N • N74LS113N	
Ceramic DIP	N74S113F • N74LS113F	S54S113F • S54LS113F
Flatpack		S54S113W • S54LS113W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

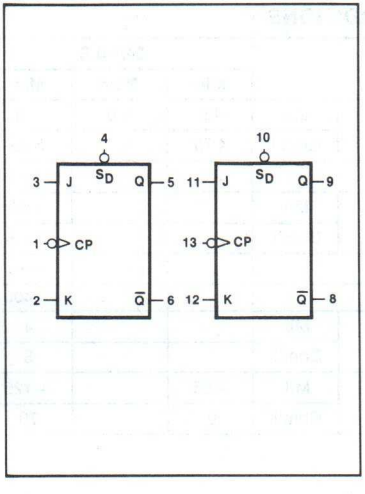
PINS	DESCRIPTION	54/74S	54/74LS
$\overline{CP}$	Clock input	2SuI	4LSuI
$\overline{S}_D$	Set inputs	3.5SuI	3LSuI
J, K	Data inputs	1SuI	1LSuI
Q, $\overline{Q}$	Outputs	10SuI	10LSuI

NOTE
A 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

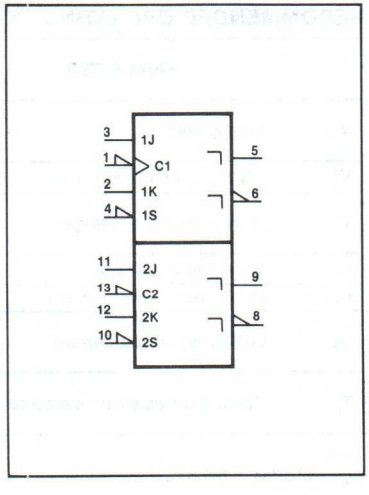
PIN CONFIGURATION



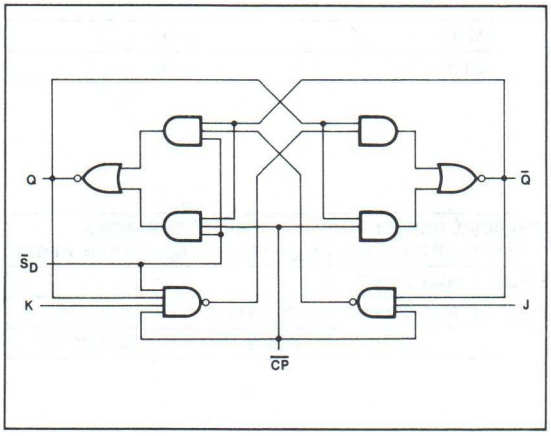
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS	
	$\overline{S}_D$	$\overline{CP}$	J	K	Q	$\overline{Q}$
Asynchronous Set	L	X	X	X	H	L
Toggle	H	↓	h	h	$\overline{q}$	q
Load "0" (Reset)	H	↓	l	h	L	H
Load "1" (Set)	H	↓	h	l	H	L
Hold "no change"	H	↓	l	l	q	$\overline{q}$

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW Clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the HIGH-to-LOW Clock transition.
q = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW Clock transition.
X = Don't care.
↓ = HIGH-to-LOW Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to −7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS113			54/74S113			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V	J, K Inputs			0.1				mA
				$\overline{S}_D$ Inputs			0.3				mA
				$\overline{CP}$ Inputs			0.4				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	J, K Inputs			20			50	μA
				$\overline{S}_D$ Inputs			60			100	μA
				$\overline{CP}$ Inputs			80			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	J, K Inputs			– 0.4				mA
				$\overline{S}_D$ Inputs			– 0.8				mA
				$\overline{CP}$ Inputs			– 0.8				mA
			V_I = 0.5V	J, K Inputs						– 1.6	mA
				$\overline{S}_D$ Inputs						– 7	mA
				$\overline{CP}$ Inputs						– 4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				4	8		15	50	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the Clock input grounded and all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		80		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		20 30		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 2		20 30		7.0 7.0	ns

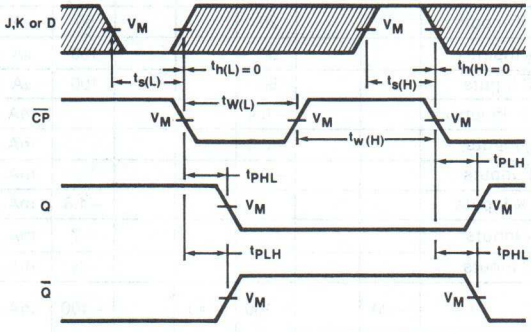
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			Min	Max	Min	Max	
$t_W(H)$	Clock pulse width (HIGH)	Waveform 1	20		6.0		ns
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	13		6.5		ns
$t_W(L)$	Set pulse width (LOW)	Waveform 2	25		8.0		ns
t_s	Setup time J or K to Clock	Waveform 1	20		3.0		ns
t_h	Hold time J or K to Clock	Waveform 1	0		0		ns

AC WAVEFORMS

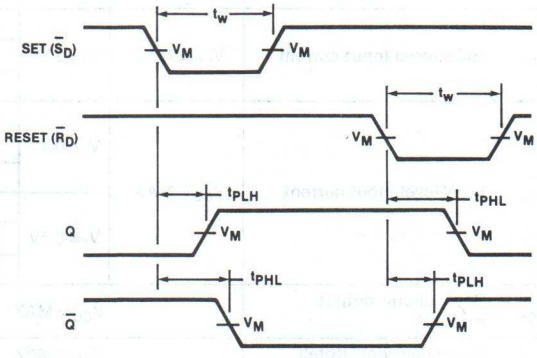
CLOCK TO OUTPUT DELAYS, DATA SETUP AND HOLD TIMES, CLOCK PULSE WIDTH



$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 1

SET AND RESET TO OUTPUT DELAYS, SET AND RESET PULSE WIDTHS

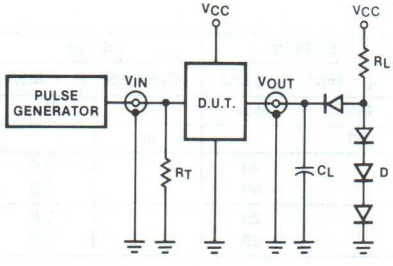


$V_M = 1.3V$ for 54LS/74LS: $V_M = 1.5V$ for all other TTL families.

Waveform 2

TEST CIRCUITS AND WAVEFORMS

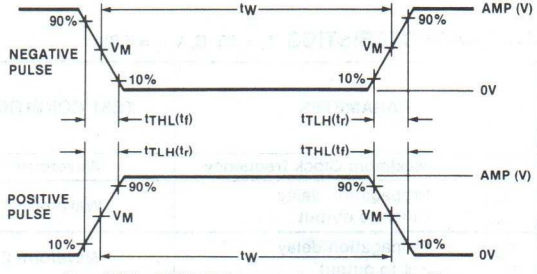
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74116

Dual 4-Bit Transparent Latch

DESCRIPTION

The '116 has two independent 4-bit transparent latches. Each 4-bit latch is controlled by a two-input active LOW Enable gate ($\overline{E}_0$ and $\overline{E}_1$). When both $\overline{E}_0$ and $\overline{E}_1$ are LOW, the data enters the latch and appears at the output. The outputs follow the Data inputs as long as $\overline{E}_0$ and $\overline{E}_1$ are LOW. The data on the D inputs one setup time before the LOW-to-HIGH transition of $\overline{E}_0$ or $\overline{E}_1$ will be stored in the latch. The Latched outputs remain stable as long as either $\overline{E}_0$ or $\overline{E}_1$ is HIGH.

Each 4-bit latch has an active LOW asynchronous Master Reset ($\overline{MR}$) input. When LOW, the $\overline{MR}$ input overrides the Data and Enable inputs and sets the four Latch outputs LOW.

TYPE	TYPICAL PROPAGATION DELAY—DATA TO OUTPUT	TYPICAL SUPPLY CURRENT (Total)
74116	11ns	50mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74116N	
Ceramic DIP	N74116F	S54116F
Flatpack		S54116W

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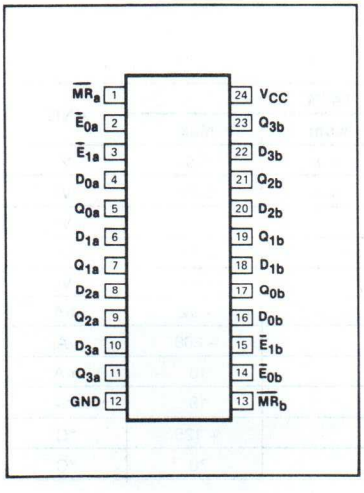
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

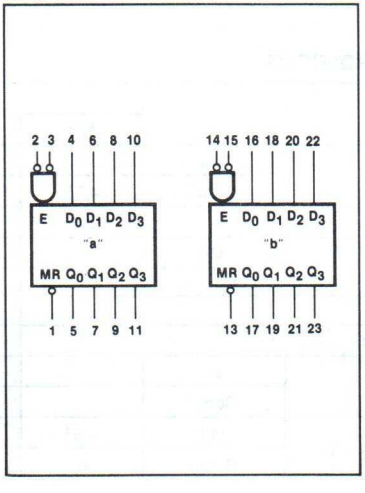
PINS	DESCRIPTION	54/74
$\overline{E}_0$, $\overline{E}_1$	Enable inputs	1ul
D_0-D_3	Data inputs	1.5ul
$\overline{MR}$	Master Reset input	1ul
Q_0-Q_3	Latch outputs	10ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

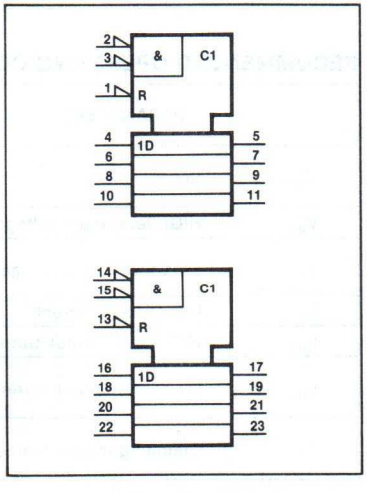
PIN CONFIGURATION



LOGIC SYMBOL

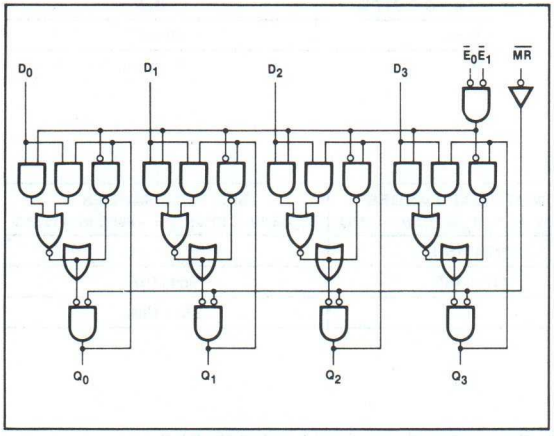


LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74116

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D_n	Q_n
Reset (clear)	L	X	X	X	L
Enable latch	H	L	L	L	L
	H	L	L	H	H
Latch data	H	↑	L	l	L
	H	L	↑	h	H

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Enable transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Enable transition.
X = Don't care.
↑ = LOW-to-HIGH Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +15	−0.5 to +15	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74116			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		Mil		0.2	0.4	V
				Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{E}$, $\overline{MR}$ Inputs				40	μA
			D Inputs				60	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{E}$, $\overline{MR}$ Inputs				– 1.6	mA
			D Inputs, initial peak				– 2.4	mA
			D Inputs, steady-state				– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	mA
				Com'l	– 18		– 57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1			60	100	mA
			Condition 2			40	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. *Condition 1.* Measure I_{CC} with all inputs grounded and all outputs open. *Condition 2.* Measure I_{CC} with $\overline{E}$ inputs grounded, all other inputs at 4.5V and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

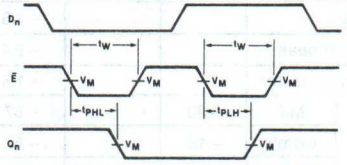
PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		30 22	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		15 18	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 3		22	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 1	18		ns
t_W	Master Reset pulse width	Waveform 3	18		ns
$t_s(H)$	Setup time HIGH Data to Enable	Waveform 4	8.0		ns
$t_h(H)$	Hold time HIGH Data to Enable	Waveform 4		– 2.0	ns
$t_s(L)$	Setup time LOW Data to Enable	Waveform 4	14.0		ns
$t_h(L)$	Hold time LOW Data to Enable	Waveform 4	8.0		ns
$t_h(L)$	Hold time LOW Enable to Master Reset to load HIGH	Waveform 3	8.0		ns

AC WAVEFORMS

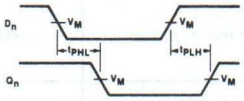
PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

Waveform 1

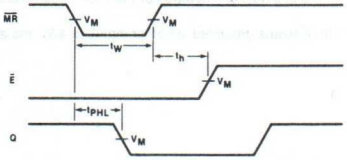
PROPAGATION DELAY DATA TO OUTPUT



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

Waveform 2

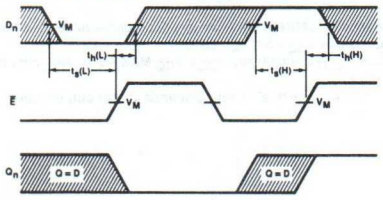
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND LOW ENABLE TO MASTER RESET HOLD TIME



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

Waveform 3

DATA SETUP AND HOLD TIMES



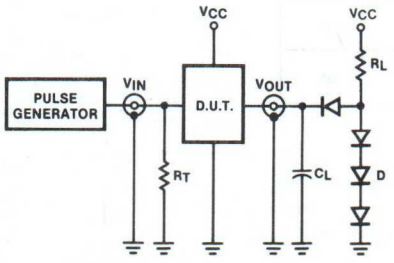
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.

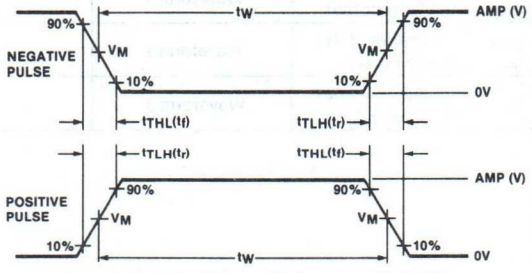
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIVIBRATOR 54/74121

Monostable Multivibrator

- **Very good pulse width stability**
- **Virtually immune to temperature and voltage variations**
- **Schmitt trigger input for slow input transitions**
- **Internal timing resistor provided**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74121	43ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74121N	
Ceramic DIP	N74121F	S54121F
Flatpack		S54121W

3

DESCRIPTION

These multivibrators feature dual active LOW going edge inputs and a single active HIGH going edge input which can be used as an active HIGH enable input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry. Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 20 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{A}_1$	$\overline{A}_2$	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
$\overline{A}_1$, $\overline{A}_2$	Inputs	1ul
B	Input	2ul
Q, $\overline{Q}$	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

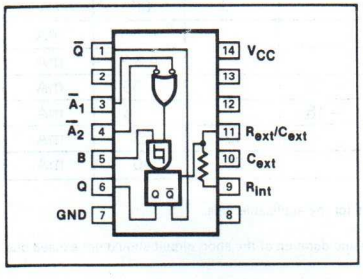
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ for the 54121 and 2KΩ to 40kΩ for the 74121). Throughout these ranges, pulse width is defined by the relationship: (see Figure 1)

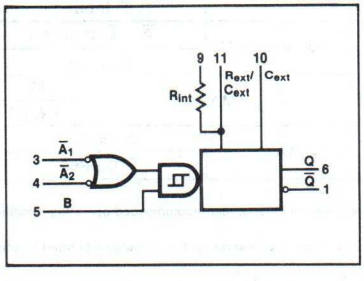
$$t_W(out) = C_{ext} R_{ext} \ln 2$$
$$t_W(out) \cong 0.7 C_{ext} R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.

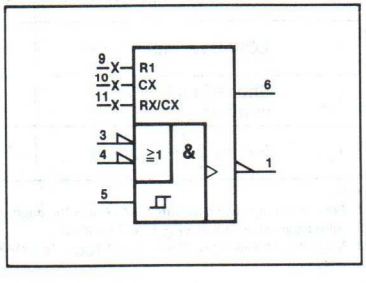
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR 54/74121

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
dv/dt	Rate of rise or fall of input pulse	B input	1			V/s
		$\overline{A}_1$,$\overline{A}_2$ inputs	1			V/μs
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74121			UNIT
					Min	Typ[2]	Max	
V_{T+}	Positive-going threshold at $\overline{A}$ and B	V_{CC} = MIN					2.0	V
V_{T-}	Negative-going threshold at $\overline{A}$ and B	V_{CC} = MIN			0.8			V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		Mil		0.2	0.4	V
				Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{A}_1$, $\overline{A}_2$ inputs				40	μA
			B input				80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{A}_1$, $\overline{A}_2$ inputs				−1.6	mA
			B input				−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	−20		−55	mA
				Com'l	−18		−55	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	Quiescent			13	25	mA
			Triggered			23	40	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$ Min	54/74 $C_L = 15pF$, $R_L = 400\Omega$ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 $C_{ext} = 80pF$, R_{int} to V_{CC}		70 80	ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 $C_{ext} = 80pF$, R_{int} to V_{CC}		55 65	ns
t_W	Minimum output pulse width	$C_{ext} = 0pF$, R_{int} to V_{CC}	20	50	ns
t_W	Output pulse width	$C_{ext} = 80pF$, R_{int} to V_{CC}	70	150	ns
		$C_{ext} = 100pF$, $R_{ext} = 10k\Omega$	600	800	ns
		$C_{ext} = 1\mu F$, $R_{ext} = 10k\Omega$	6.0	8.0	ms

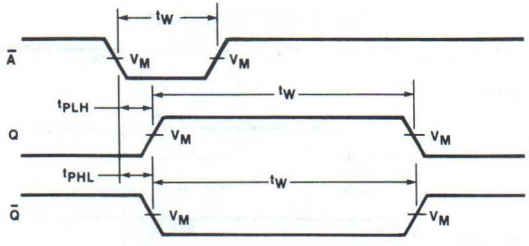
3

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		54/74 Min	54/74 Max	UNIT
t_W	Minimum input pulse width to trigger	Waveforms 1 & 2		50		ns
R_{ext}	External timing resistor range		Mil	1.4	30	kΩ
			Com'l	1.4	40	kΩ
C_{ext}	External timing capacitance range			0	1000	pF
	Output duty cycle	$R_{ext} = 2k\Omega$			67	%
		$R_{ext} = R_{ext}(Max)$			90	%

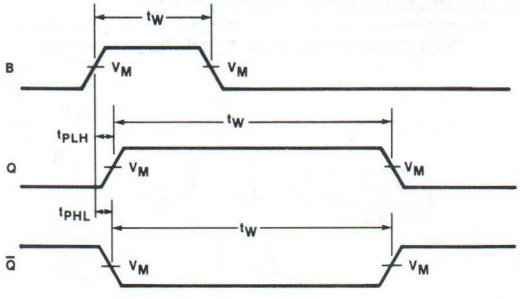
AC WAVEFORMS

PROPAGATION DELAY $\overline{A}$ INPUT TO Q AND $\overline{Q}$ OUTPUTS, INPUT AND OUTPUT PULSE WIDTHS



Waveform 1

PROPAGATION DELAY B INPUT TO Q AND $\overline{Q}$ OUTPUT, INPUT AND OUTPUT PULSE WIDTHS



Waveform 2

V_M = 1.5 for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

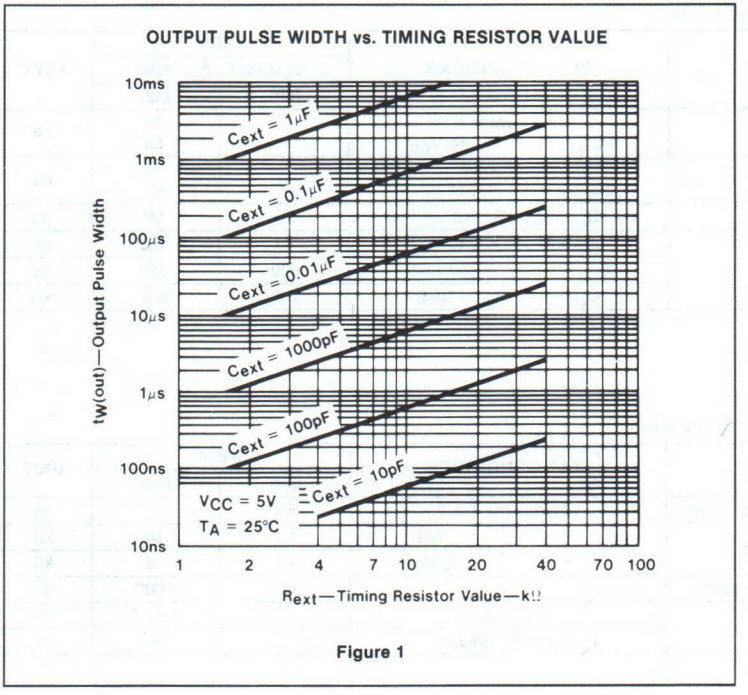
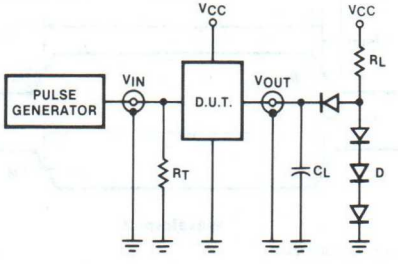


Figure 1

TEST CIRCUITS AND WAVEFORMS

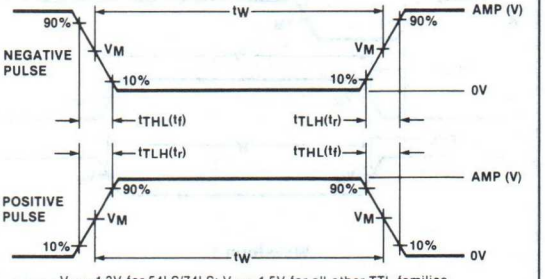
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIVIBRATOR 54/74123

Dual Retriggerable Monostable Multivibrator

- **DC triggered from active HIGH or active LOW inputs**
- **Retriggerable for very long pulses—up to 100% duty cycle**
- **Direct reset terminates output pulse**
- **Compensated for V_{CC} and temperature variations**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74123	24ns	46mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74123N	
Ceramic DIP	N74123F	S54123F
Flatpack		S54123W

3

DESCRIPTION

The '123 is a dual retriggerable monostable multivibrator with output pulse width control by three methods. The basic pulse time is programmed by selection of external resistance (R_{ext}) and capacitance (C_{ext}) values. Once triggered, the basic pulse width may be extended by retriggering the gated active LOW going edge input ($\overline{A}$) or the active HIGH going edge input (B), or be reduced by use of the overriding active LOW reset.

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when $C_{ext} \leq 1000pF$, see Figure A.

When $C_{ext} > 1000pF$, the output pulse width is defined as:

$$t_W = 0.28\ R_{ext}/C_{ext}\ (1 + \frac{0.7}{R_{ext}})$$

The external resistance and capacitance are normally connected as shown in Figure B. If an electrolytic capacitor is to be used with an inverse voltage rating of less than 1V then Figure C should be used. (Inverse voltage rating of an electrolytic is normally specified at 5% of the forward voltage rating.) If the inverse voltage rating is 1V or more (this includes a 100% safety margin) then Figure B can be used. Note that if Figure C is used the timing equations change as follows:

$$t_W \cong 0.25\ R_{ext}/C_{ext}\ (1 + \frac{0.7}{R_{ext}})$$

FUNCTION TABLE

INPUTS			OUTPUTS	
R_D	$\overline{A}$	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

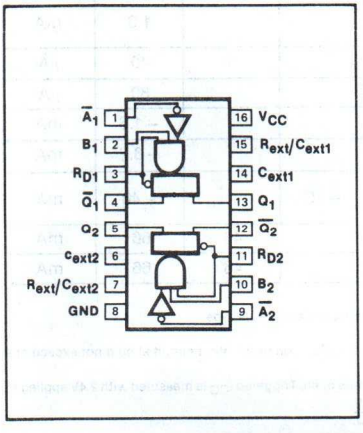
H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = One HIGH-level pulse
⎍ = One LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

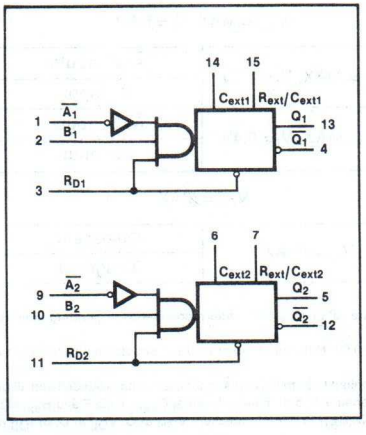
PINS	DESCRIPTION	54/74
$\overline{A}$, B	Inputs	1ul
R_D	Input	2ul
Q, $\overline{Q}$	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

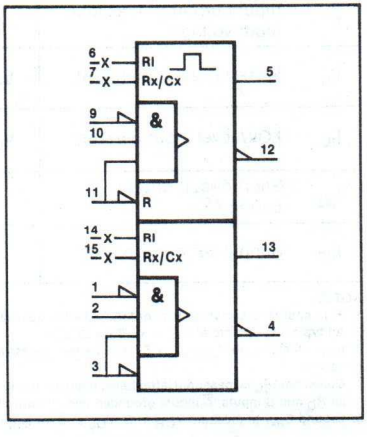
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR 54/74123

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74123			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage[5]	V_{CC} = MIN, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage[5]	V_{CC} = MIN, I_{OL} = MAX		Mil		0.2	0.4	V
				Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{A}$, B inputs				40	μA
			R_D input				80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{A}$, B inputs				−1.6	mA
			R_D input				−3.2	mA
I_{OS}	Short-circuit output current[3,5]	V_{CC} = MAX			−10		−40	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Quiescent			46	66	mA
			Triggered			46	66	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Quiescent I_{CC} is measured (after being reset) with 2.4V applied to both R_D and $\overline{A}$ inputs, B inputs grounded and all outputs open. Triggered I_{CC} is measured with 2.4V applied to all R_D and B inputs, $\overline{A}$ inputs grounded and all outputs open. For both measurements, C_{ext} = 0.02μF and R_{ext} = 25kΩ.
5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.

MULTIVIBRATOR 54/74123

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

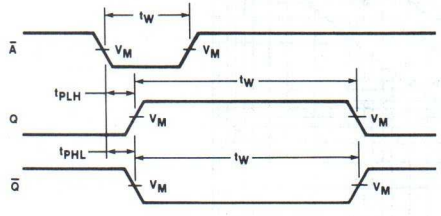
PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$ Min	54/74 $C_L = 15pF$, $R_L = 400\Omega$ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		33 40	ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		28 36	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		40 27	ns
t_W Q	Minimum Q pulse width	Waveforms 1 & 2 $C_{ext} = 0pF$, $R_{ext} = 5k\Omega$		65	ns
t_W Q	Output pulse width	Waveforms 1 & 2 $C_{ext} = 1000pF$, $R_{ext} = 10k\Omega$	2.76	3.37	μs

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		54/74 Min	54/74 Max	UNIT
t_W	Minimum input pulse width to trigger	Waveforms 1 & 2		40		ns
R_{ext}	External timing resistor range		Mil	5.0	25	kΩ
			Com'l	5.0	50	
C_{ext}	External timing capacitance range			No restriction		pF
$C_{Rx/Cx}$	Stray capacitance to GND at R_{ext}/C_{ext} terminal				50	pF

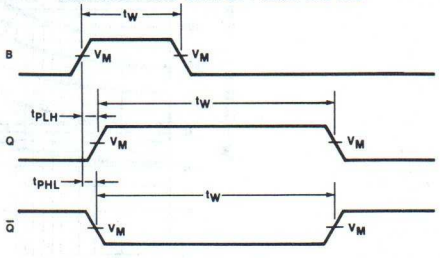
AC WAVEFORMS

PROPAGATION DELAY $\overline{A}$ INPUT TO Q AND $\overline{Q}$ OUTPUTS, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 1

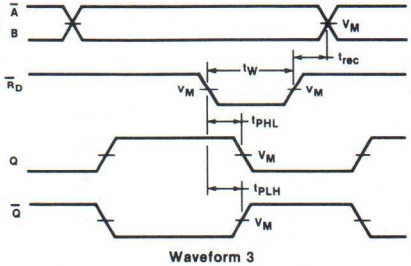
PROPAGATION DELAY B INPUT TO Q AND $\overline{Q}$ OUTPUT, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

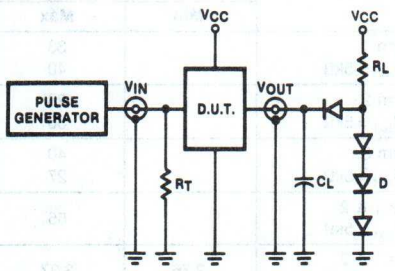
DIRECT RESET DELAYS AND RECOVERY TIME



Waveform 3

TEST CIRCUITS AND WAVEFORMS

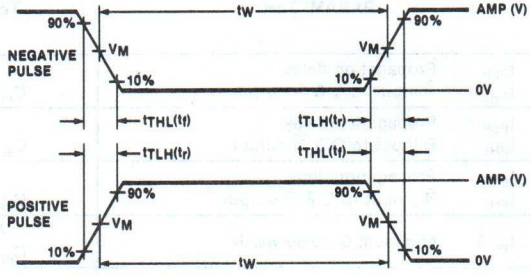
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

TYPICAL PERFORMANCE CHARACTERISTICS

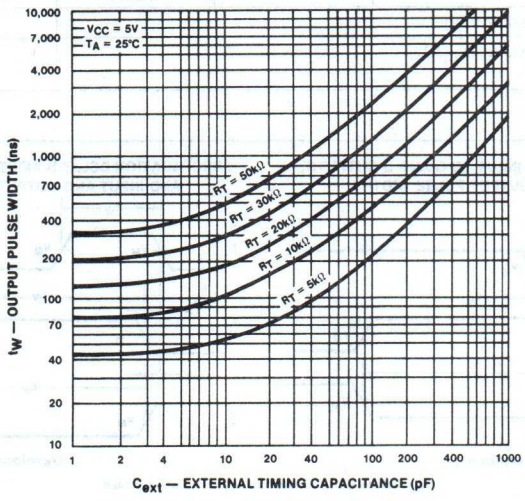


Figure A

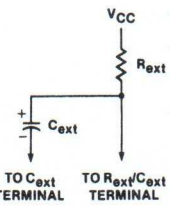


Figure B

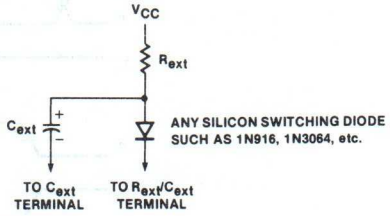


Figure C

Quad 3-State Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74125	10ns	32mA
74LS125	8ns	11mA
74126	10ns	36mA
74LS126	9ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74125N • N74LS125N N74126N • N74LS126N	
Ceramic DIP	N74125F • N74LS125F N74126F • N74LS126F	S54LS125F S54126F • S54LS126F
Flatpack		S54LS125W S54126W • S54LS126W

FUNCTION TABLE '125

INPUTS		OUTPUT
C	A	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE '126

INPUTS		OUTPUT
C	A	Y
H	L	L
H	H	H
L	X	(Z)

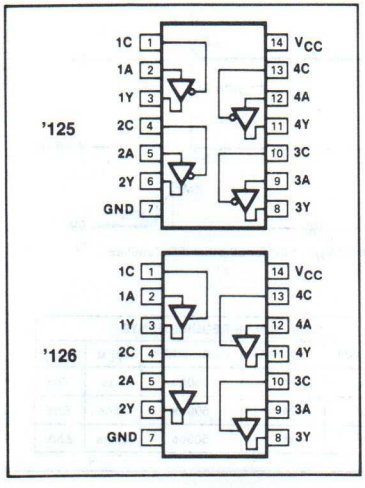
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off)

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

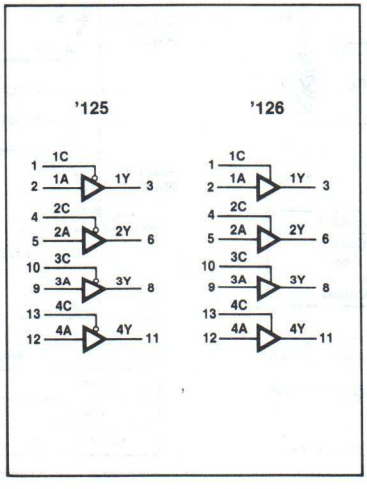
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

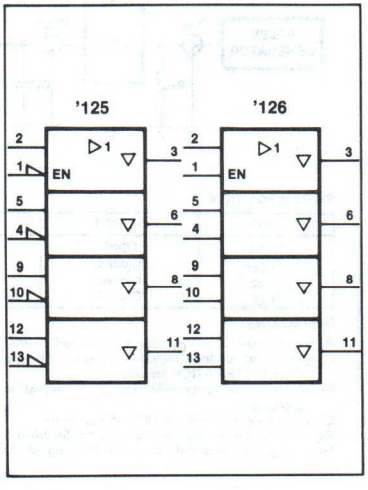
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

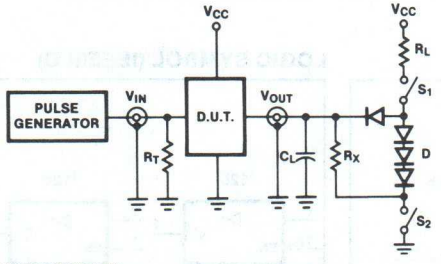
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0			−1.0	mA
		Com'l			−5.2			−2.6	mA
I_{OL}	LOW-level output current	Mil			16			12	mA
		Com'l			16			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



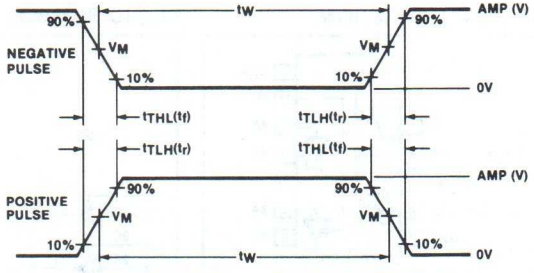
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

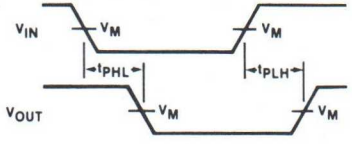
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74125 54/74126			54/74LS125 54/74LS126			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.3		2.4			V
				Com'l	2.4	3.1		2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V					40			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					– 40			– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 30		– 70	– 40		– 130	mA
				Com'l	– 28		– 70	– 40		– 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX		'125		32	54		11	20	mA
				'126		36	62		12	22	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

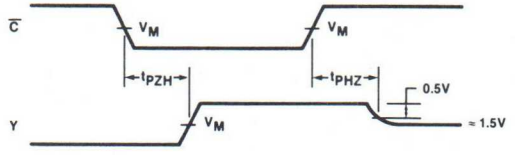
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

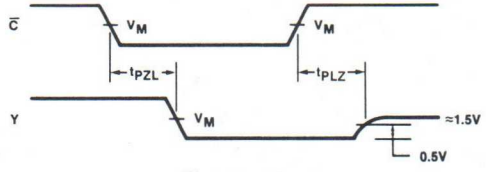
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74125 $C_L = 50pF$ $R_L = 400\Omega$		54/74LS125 $C_L = 45pF$ $R_L = 667\Omega$		54/74126 $C_L = 50pF$ $R_L = 400\Omega$		54/74LS126 $C_L = 45pF$ $R_L = 667\Omega$		UNIT
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		13 18		15 18		13 18		15 18	ns
t_{PZH}	Enable to HIGH	Waveform 2		17		20		18		25	ns
t_{PZL}	Enable to LOW	Waveform 3		25		25		25		35	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		8.0		20		16		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		12		20		18		25	ns

Quad Two-Input NOR Buffer

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74128	7ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74128N	
Ceramic DIP	N74128F	

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

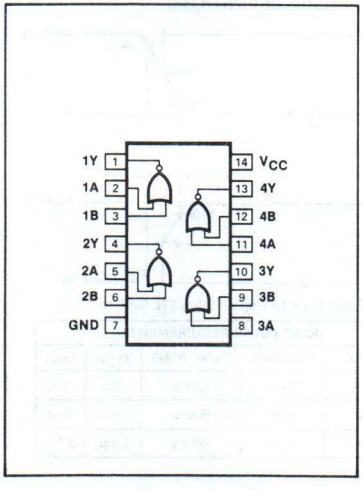
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

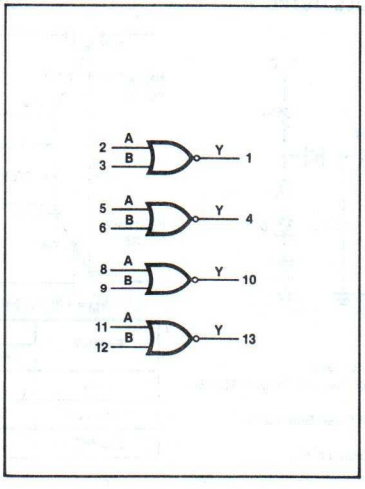
PINS	DESCRIPTION	54/74
A, B	Inputs	1ul
Y	Output	30ul

NOTE
Where a 54/74 unit load is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

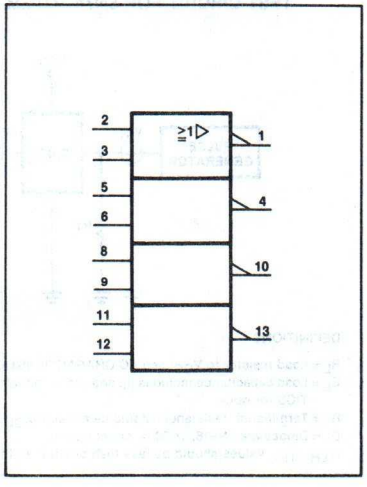
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

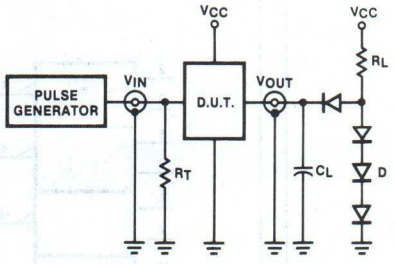
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current	Mil			−29	mA
		Com'l			−42.4	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com	0		70	°C

TEST CIRCUITS AND WAVEFORMS

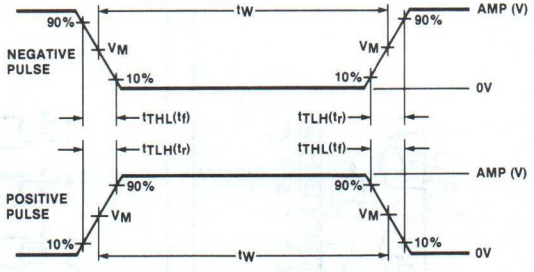
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

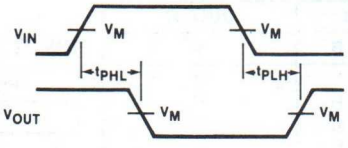
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74128 Min	54/74128 Typ[2]	54/74128 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = 0.8V, I_{OH} = −2.4mA		2.4	3.4		V
		V_{CC} = MIN, V_{IL} = 0.4V, I_{OH} = −13.2mA		2.4			V
		V_{CC} = MIN, V_{IL} = 0.4V, I_{OH} = MAX	Mil	2.0			V
			Com'l	2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−70		−180	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		12	21	mA
			I_{CCL} Outputs LOW		33	57	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 R_L = 133Ω Min	54/74 R_L = 133Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, C_L = 50pF		9 12	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, C_L = 150pF		15 18	ns

Quad 2-Input NAND Schmitt Trigger

DESCRIPTION

The '132 contains four 2-input NAND gates which accept standard TTL input signals and provide standard TTL output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have greater noise margin than conventional NAND gates.

Each circuit contains a 2-input Schmitt trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt trigger uses positive feedback to effectively speed-up slow input transition, and provide different input threshold voltages for positive and negative-going transitions. This hysteresis between the positive-going and negative-going input threshold (typically 800mW) is determined internally by resistor ratios and is essentially insensitive to temperature and supply voltage variations. As long as one input remains at a more positive voltage than V_{T+MAX}, the gate will respond to the transitions of the other input as shown in Waveform 1.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74132	15ns	21mA
74LS132	15ns	7mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74132N • N74LS132N	
Ceramic DIP	N74132F • N74LS132F	S54132F • S54LS132F
Flatpack		S54132W • S54LS132W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

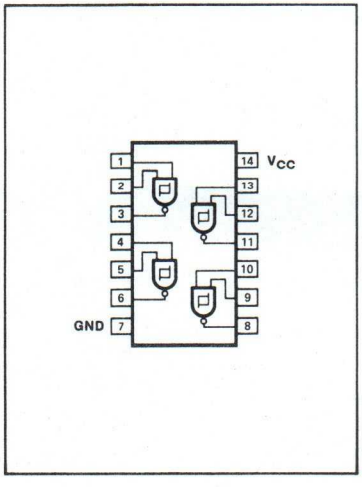
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

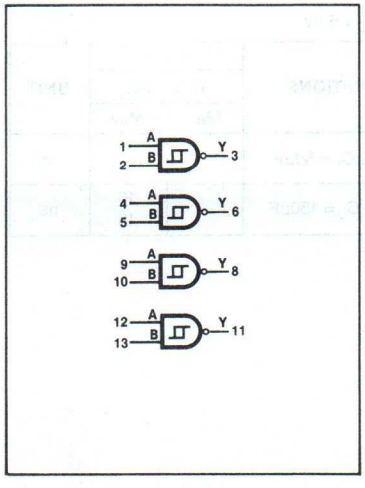
PINS	DESCRIPTION	54/74	54/74LS
A, B	Inputs	1ul	1LSul
Y	Ouput	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

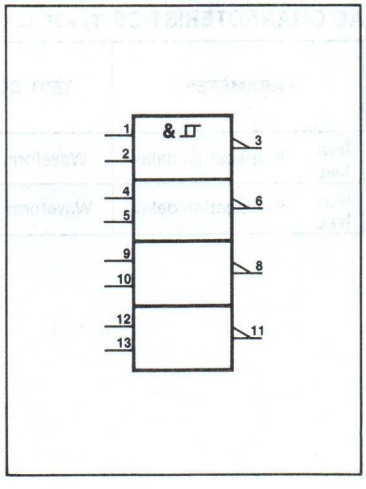
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

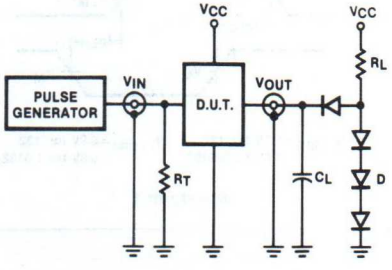
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

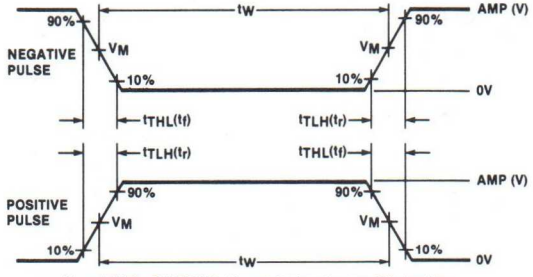
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

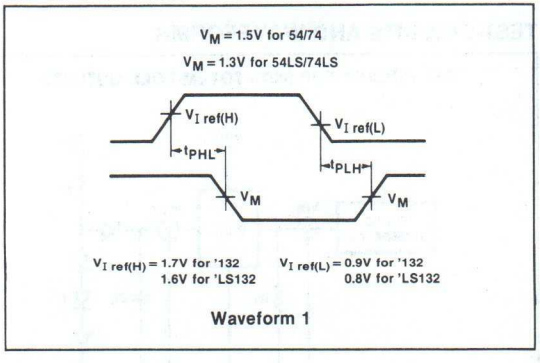
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74132			54/74LS132			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{T+}	Positive-going threshold	V_{CC} = 5.0V			1.5	1.7	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-going threshold	V_{CC} = 5.0V			0.6	0.9	1.1	0.5	0.8	1.0	V
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5.0V			0.4	0.8		0.4	0.8		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, $V_I = V_{T-MIN}$, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, $V_I = V_{T+MAX}$	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, $I_I = I_{IK}$					-1.5			-1.5	V
I_{T+}	Input current at positive-going threshold	V_{CC} = 5.0V, $V_I = V_{T+}$				-0.43			-0.14		mA
I_{T-}	Input current at negative-going threshold	V_{CC} = 5.0V, $V_I = V_{T-}$				-0.56			-0.18		mA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.2			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-18		-55	-20		-100	mA
				Com'l	-18		-55	-20		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		15	24		5.9	11	mA
			I_{CCL}	Outputs LOW		26	40		8.2	14	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



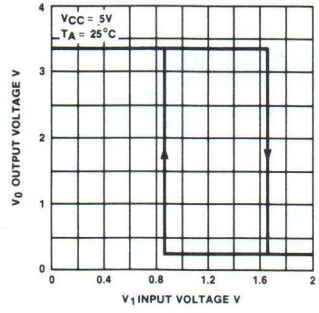
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

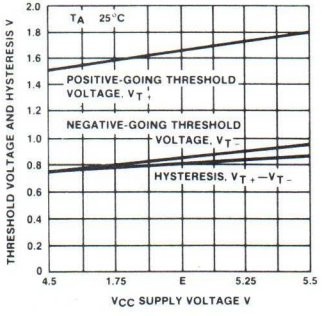
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		22 22		22 22	ns

TYPICAL CHARACTERISTICS

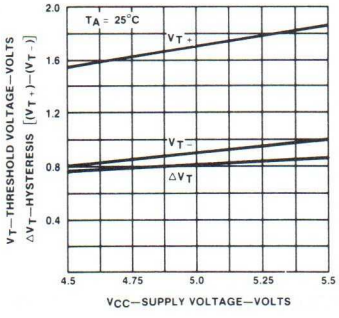
(54/74, 54LS/74LS)
V_{IN} vs V_{OUT} TRANSFER FUNCTION



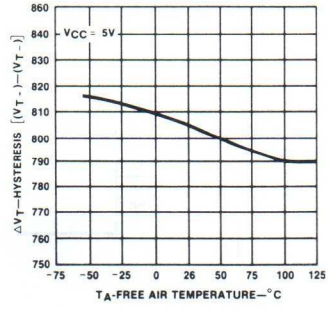
(54/74)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



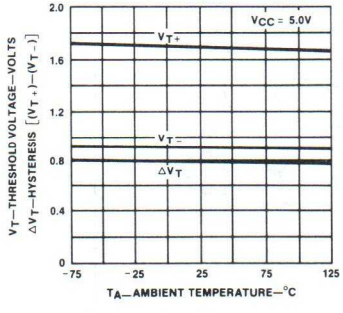
(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs POWER SUPPLY VOLTAGE



(54/74)
HYSTERESIS vs TEMPERATURE



(54LS/74LS)
THRESHOLD VOLTAGE AND HYSTERESIS vs AMBIENT TEMPERATURE



13-Input NAND Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S133	4ns	4mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S133N	
Ceramic DIP	N74S133F	S54S133F
Flatpack		S54S133W

FUNCTION TABLE

INPUTS	OUTPUT
A ••• M	$\overline{Y}$
H ••• H	L
one input = L	H

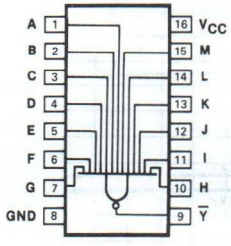
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

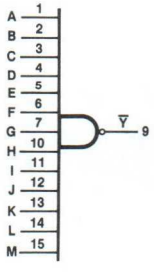
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
$\overline{Y}$	Output	10Sul

NOTE
A 54/74S unit load (Sul) is understood to be 50μA I_{IH} and −2.0mA I_{IL}.

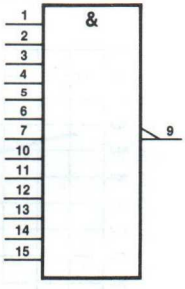
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

3

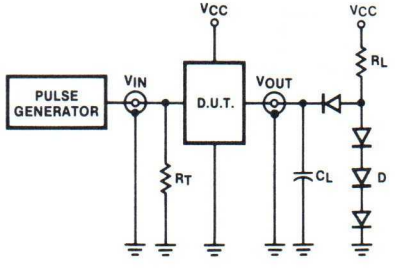
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

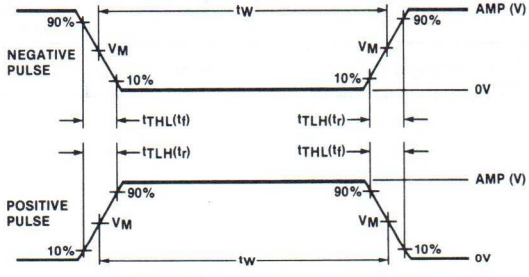
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

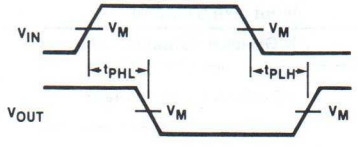
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S133 Min	54/74S133 Typ[2]	54/74S133 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil			0.5[4]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		3	5	mA
			I_{CCL} Outputs LOW		5.5	10	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74LS C_L = 15pF, R_L = 280Ω Min	54S/74LS C_L = 15pF, R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		6.0 7.0	ns

12-Input NAND Gate (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74S134	5ns	10mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74S134N	
Ceramic DIP	N74S134F	

FUNCTION TABLE

INPUTS		OUTPUT
D_0 ••• D_{11}	$\overline{OE}$	$\overline{Y}$
H ••• H	L	L
one input = L	L	H
X ••• X	H	(Z)

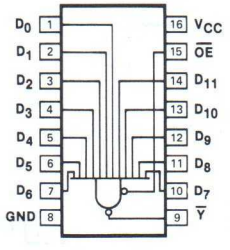
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

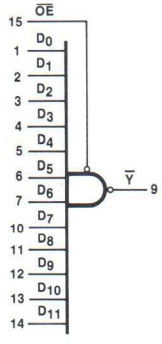
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
$\overline{Y}$	Output	10Sul

NOTE
Where a 54/74S unit load (Sul) is understood to be 50μA I_{IH} and −2.0mA I_{IL}.

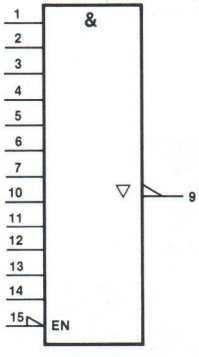
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

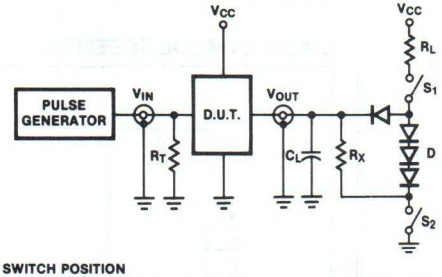
PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



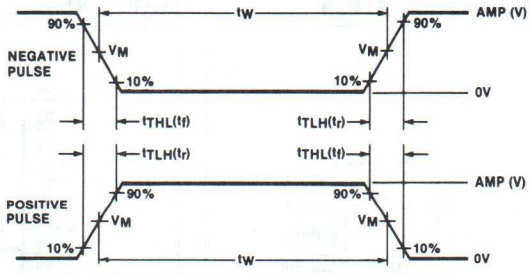
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

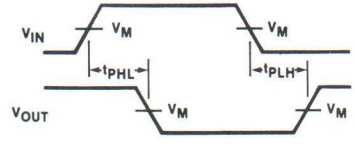
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74S134			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −2mA	Mil	2.4	3.4		V
			I_{OH} = −6.5mA	Com'l	2.4	3.2		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX		Mil			0.5	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.5V					−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		7	13	mA
			I_{CCL}	Outputs LOW		9	16	mA
			I_{CCZ}	Outputs OFF		14	25	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

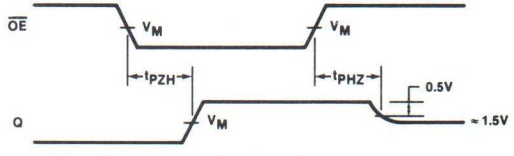
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



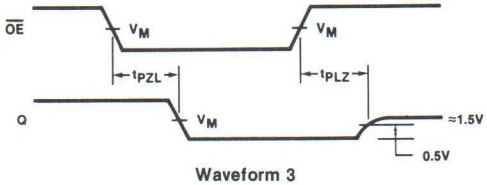
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54S/74S $C_L = 15pF$, $R_L = 280\Omega$		UNIT
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		6.0	ns
t_{PHL}	Propagation delay	Waveform 1		7.5	ns
t_{PZH}	Enable to HIGH	Waveform 2, $C_L = 50pF$		19.5	ns
t_{PZL}	Enable to LOW	Waveform 3, $C_L = 50pF$		21	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		8.5	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		14	ns

Quad Exclusive OR/NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S135	9ns	65mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S135N	
Ceramic DIP	N74S135F	S54S135F
Flatpack		S54S135W

FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

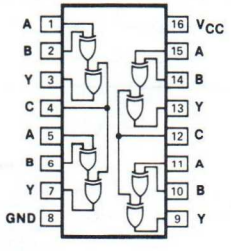
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

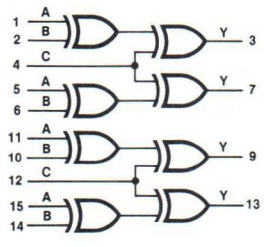
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
A 54/74S unit load (Sul) is understood to be 50μA I_{IH} and −2.0mA I_{IL}.

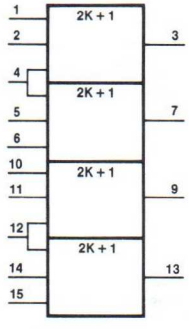
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

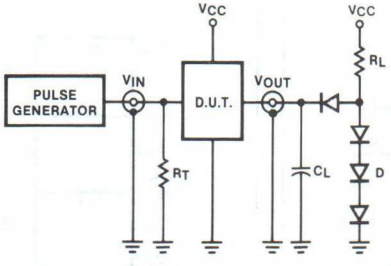
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.45V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

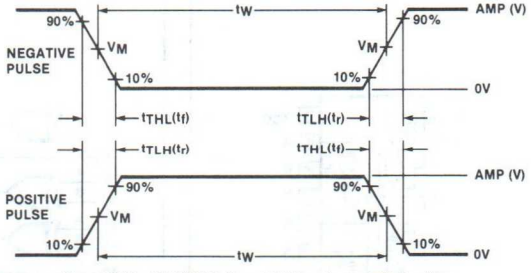
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

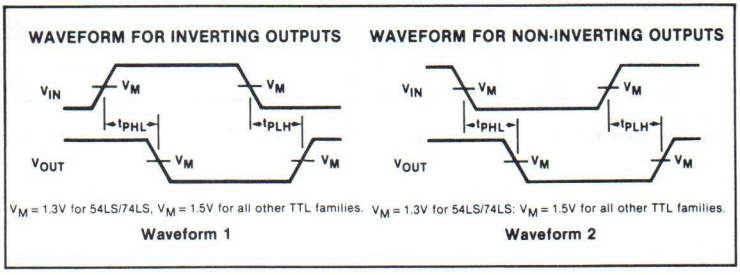
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S135 Min	54/74S135 Typ[2]	54/74S135 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil			0.5[5]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			65	99	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the inputs grounded and the outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



Waveform 1 Waveform 2

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74S C_L = 15pF, R_L = 280Ω Min	54S/74S C_L = 15pF, R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, C = LOW, B or A = LOW		13 15	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, C = LOW, B or A = HIGH		12 13.5	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, C = HIGH, B or A = LOW		15 10	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, C = HIGH, B or A = HIGH		12 11	ns
t_{PLH} t_{PHL}	Propagation delay C to output	Waveform 2, A = B		12 14.5	ns
t_{PLH} t_{PHL}	Propagation delay C to output	Waveform 1, A ≠ B		11.5 12	ns

GATE 54/74LS136

Quad Two-Input Exclusive-OR Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS136	18ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS136N	
Ceramic DIP	N74LS136F	S54LS136F
Flatpack		S54LS136W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

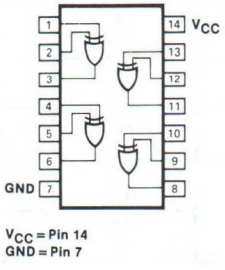
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
Y	Output	10LSul

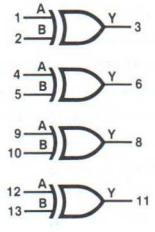
NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

PIN CONFIGURATION

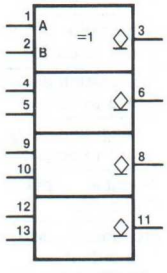


V_{CC} = Pin 14
GND = Pin 7

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

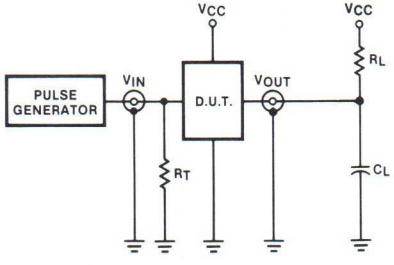
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

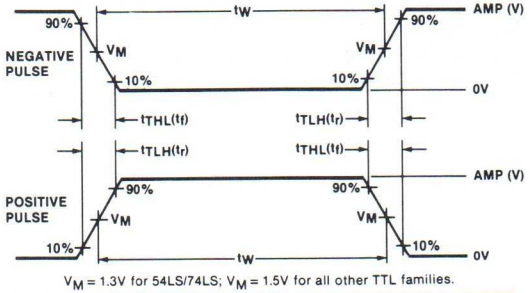
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

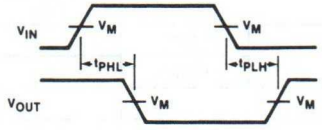
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS136			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = MAX					100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 0.8	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.1	10	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded, and all outputs open.

AC WAVEFORMS

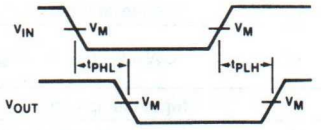
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS: V_M = 1.5V for all other TTL families.

Waveform 2

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input LOW Waveform 2		30 30	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Other input HIGH Waveform 1		30 30	ns

DECODERS/DEMULTIPLEXERS 54/74LS138, S138

1-Of-8 Decoder/Demultiplexer

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel 3205**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS138	20ns	6.3mA
74S138	7ns	49mA

3

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active LOW outputs ($\overline{0}$–$\overline{7}$). The device features three Enable inputs: two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). Every output will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active LOW Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active HIGH or active LOW state.

ORDERING CODE

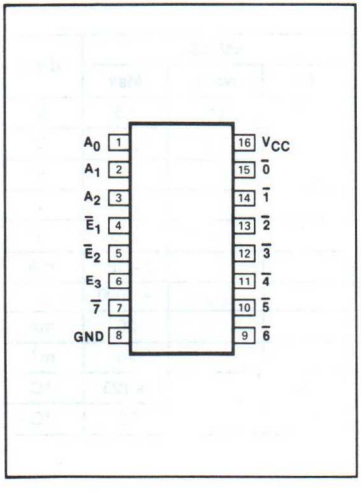
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S138N • N74LS138N	
Ceramic DIP	N74S138F • N74LS138F	S54S138F • S54LS138F
Flatpack		S54S138W • S54LS138W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

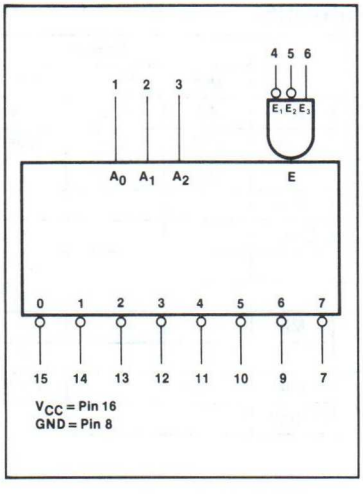
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

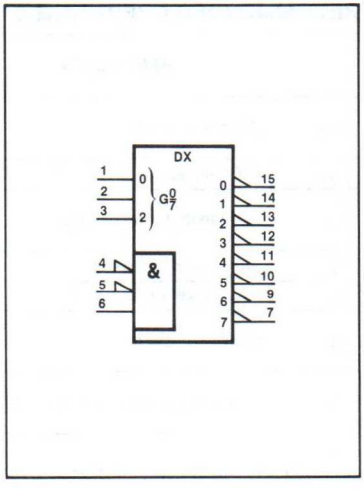
PIN CONFIGURATION



LOGIC SYMBOL

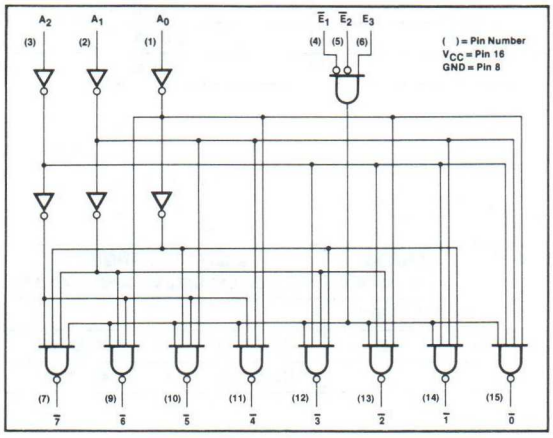


LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS 54/74LS138, S138

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS							
$\bar{E}_1$	$\bar{E}_2$	E_3	A_0	A_1	A_2	$\bar{0}$	$\bar{1}$	$\bar{2}$	$\bar{3}$	$\bar{4}$	$\bar{5}$	$\bar{6}$	$\bar{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

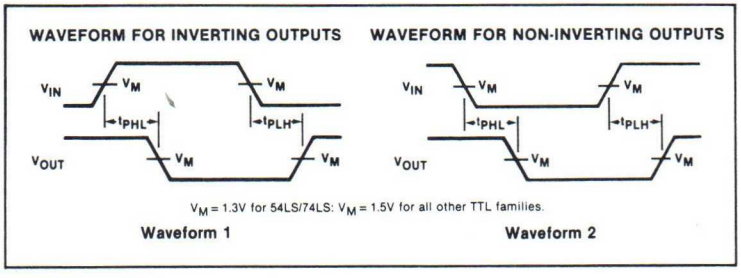
NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS138			54/74S138			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.3	10		49	74	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS

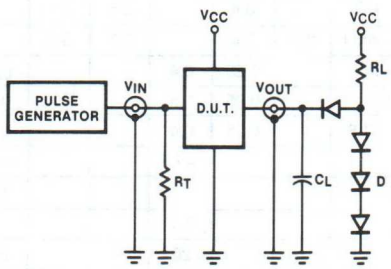


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 41		7 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		27 39		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		18 32		8 11	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		26 38		11 11	ns

TEST CIRCUITS AND WAVEFORMS

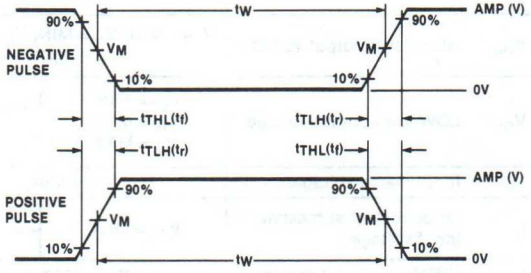
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODERS/DEMULTIPLEXERS 54/74LS139, S139

Dual 1-of-4 Decoder/Demultiplexer

- **Demultiplexing capability**
- **Two independent 1-of-4 decoders**
- **Multifunction capability**
- **Replaces 9321 and 93L21 for higher performance**

TYPE	TYPICAL PROPAGATION DELAY (Enable at 2 logic levels)	TYPICAL SUPPLY CURRENT (Total)
74LS139	19ns	6.8mA
74S139	6ns	60mA

DESCRIPTION

The '139 is a high-speed, dual 1-of-4 decoder/demultiplexer. This device has two independent decoders, each accepting two binary weighted inputs (A_0, A_1) and providing four mutually exclusive active LOW outputs ($\overline{0}$-$\overline{3}$). Each decoder has an active LOW Enable ($\overline{E}$). When $\overline{E}$ is HIGH, every output is forced HIGH. The Enable can be used as the Data input for a 1-of-4 demultiplexer application.

ORDERING CODE

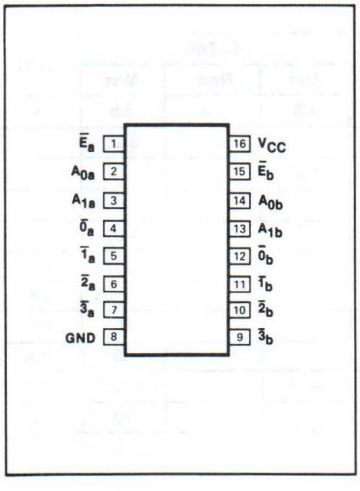
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S139N • N74LS139N	
Ceramic DIP	N74S139F • N74LS139F	S54S139F • S54LS139F
Flatpack		S54S139W • S54LS139W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

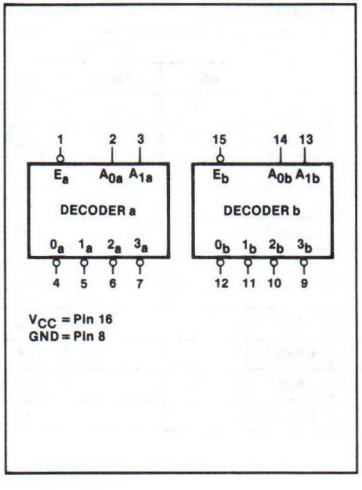
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

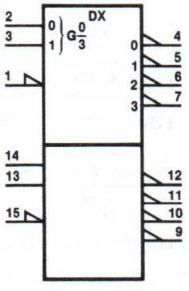
PIN CONFIGURATION



LOGIC SYMBOL

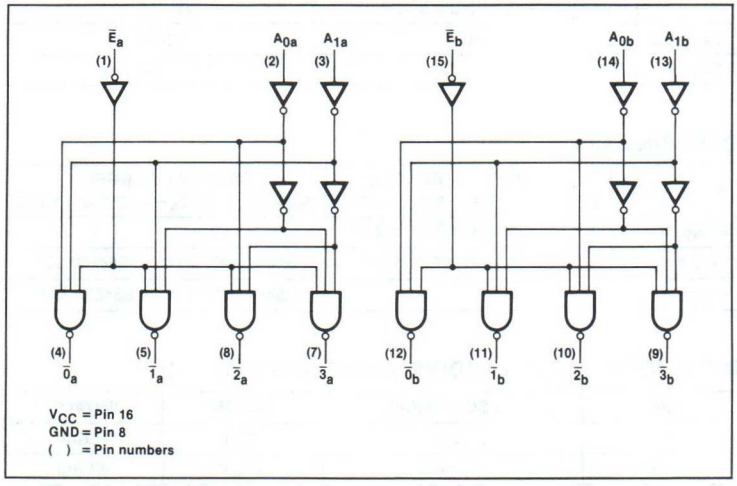


LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS 54/74LS139, S139

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

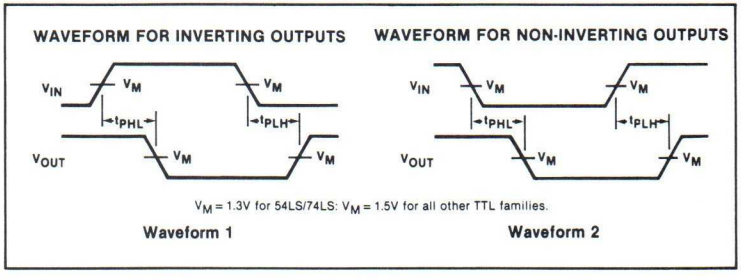
NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS139			54/74S139			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
				Com'l	2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 15		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.8	11		60	90	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS

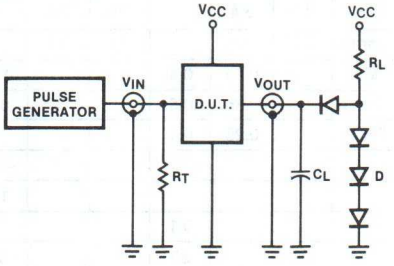


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 33		7.5 10	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		29 38		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		24 32		8 10	ns

TEST CIRCUITS AND WAVEFORMS

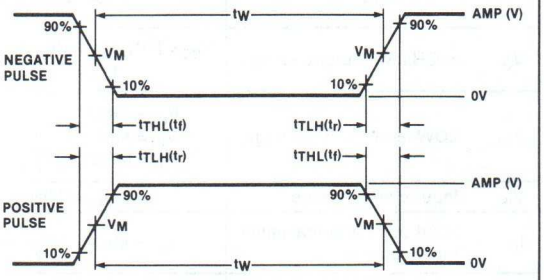
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LINE DRIVER 54/74S140

Dual Four-Input NAND 50-Ohm Line Driver

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S140	4ns	10mA (I_{CCH}) 25mA (I_{CCL})

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S140N	
Ceramic DIP	N74S140F	S54S140F
Flatpack		S54S140W

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	$\overline{Y}$
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

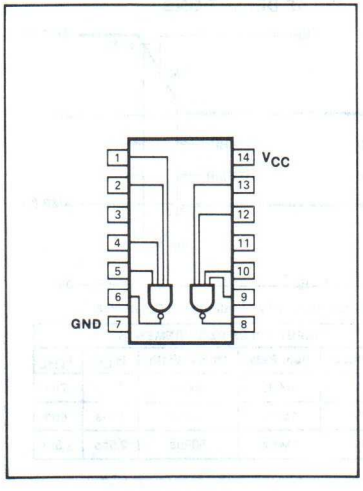
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

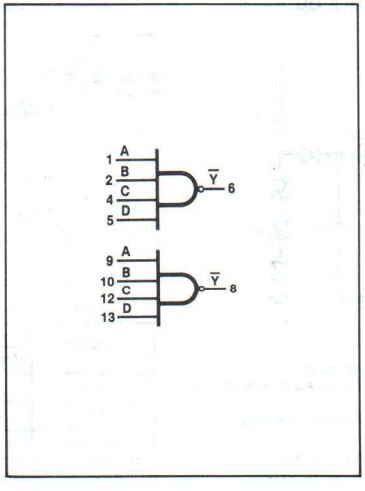
PINS	DESCRIPTION	54/74S
A–D	Inputs	2Sul
$\overline{Y}$	Output	30Sul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

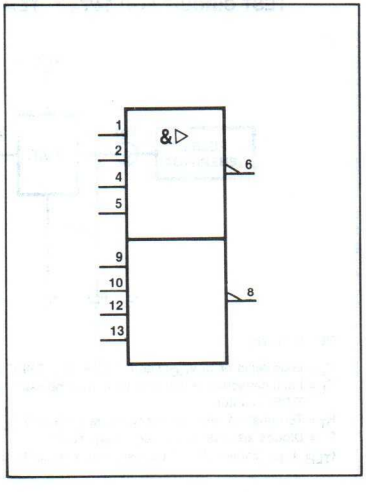
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LINE DRIVER 54/74S140

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

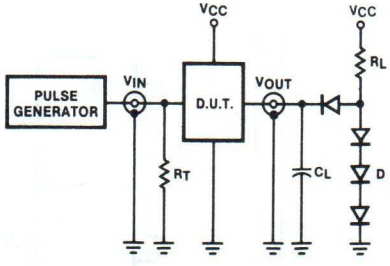
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−40	mA
I_{OL}	LOW-level output current	Mil			60	mA
		Com'l			60	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

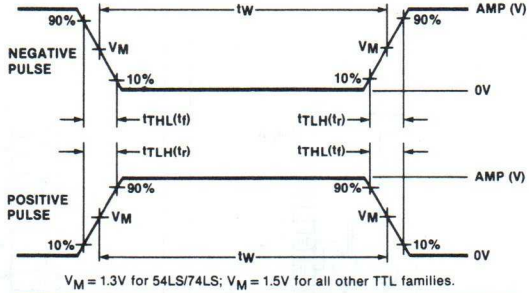
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

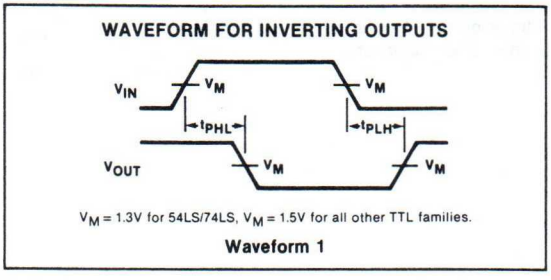
LINE DRIVER 54/74S140

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S140 Min	54/74S140 Typ[2]	54/74S140 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = −3mA	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
		V_{CC} = MIN, V_{IL} = 0.5V, R_0 = 50Ω to ground		2.0			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX	Mil			0.5[4]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−50		−225	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH		10	18	mA
			I_{CCL} Outputs LOW		25	44	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed 100 milliseconds.
4. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74S C_L = 50pF, R_L = 93Ω Min	54/74S C_L = 50pF, R_L = 93Ω Max	UNIT
t_{PLH}	Propagation delay	Waveform 1		6.5	ns
t_{PHL}				6.5	

DECODER/DRIVER 54/74145

BCD-To-Decimal Decoder/Driver (Open Collector)

- **80mA output drive capability**
- **15V output breakdown voltage**
- **See '45 for 30V output voltage**
- **See '42 for standard TTL outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74145	24ns	43mA

DESCRIPTION

The '145 is a 1-of-10 decoder with Open Collector outputs. This decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '145 features an output breakdown voltage of 15V. This device is ideal as a lamp or solenoid driver.

ORDERING CODE

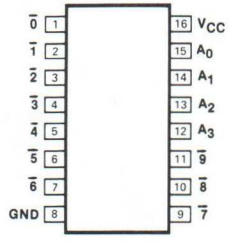
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74145N	
Ceramic DIP	N74145F	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

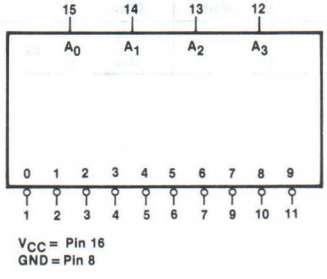
PINS	DESCRIPTION	54/74
All	Inputs	1ul
All	Outputs	12.5ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

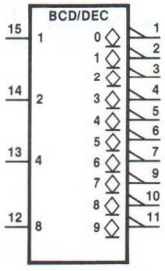
PIN CONFIGURATION



LOGIC SYMBOL

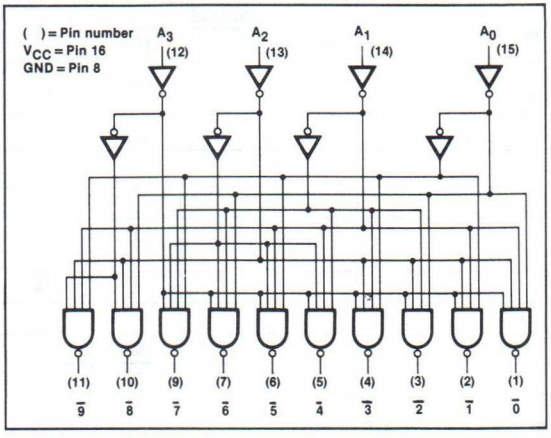


LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER 54/74145

LOGIC DIAGRAM



FUNCTION TABLE

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +15	−0.5 to +15	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
V_{OH}	HIGH-level output voltage				15	V
I_{OL}	LOW-level output current	Mil			80	mA
		Com'l			80	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

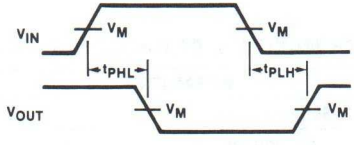
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74145 Min	54/74145 Typ[2]	54/74145 Max	UNIT
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = MAX				250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 80mA		0.5	0.9	V
			I_{OL} = 20mA			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				– 1.6	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	Mil		43	62	mA
			Com'l		43	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are are V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with all inputs grounded and outputs open.

AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

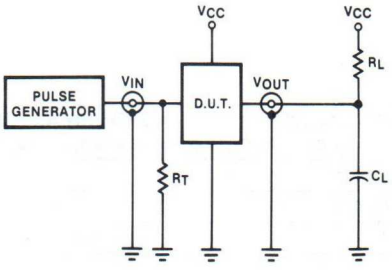
Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 100Ω Min	54/74 C_L = 15pF, R_L = 100Ω Max	UNIT
t_{PLH}	Propagation delay	Waveform 1		50	ns
t_{PHL}	Address to output			50	

TEST CIRCUITS AND WAVEFORMS

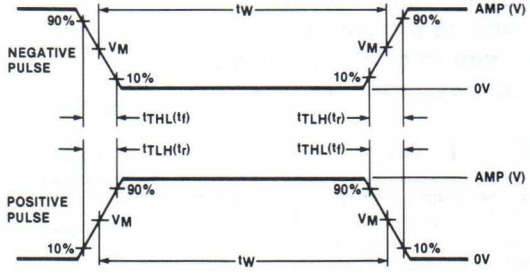
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ENCODER 54/74147

10-Line-To-4-Line Priority Encoder

- **Encodes 10-line decimal to 4-line BCD**
- **Useful for 10-position switch encoding**
- **Used in code converters and generators**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74147	10ns	46mA

DESCRIPTION

The '147 9-input priority encoder accepts data from nine active-LOW inputs ($\overline{I}_1$-$\overline{I}_9$) and provides a binary representation on the four active-LOW outputs (A_0-A_3). A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_9$ having the highest priority.

The device provides the 10-line-to-4-line priority encoding function by use of the implied decimal "zero." The "zero" is encoded when all nine data inputs are HIGH, forcing all four outputs HIGH.

ORDERING CODE

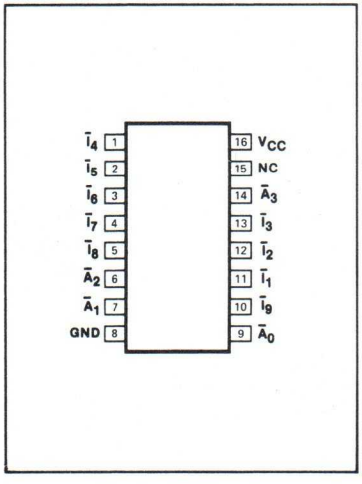
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74147N	
Ceramic DIP	N74147F	S54147F
Flatpack		S54147W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

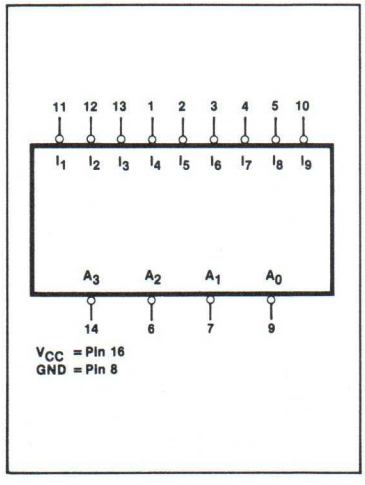
PINS	DESCRIPTION	54/74
All	Inputs	1ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

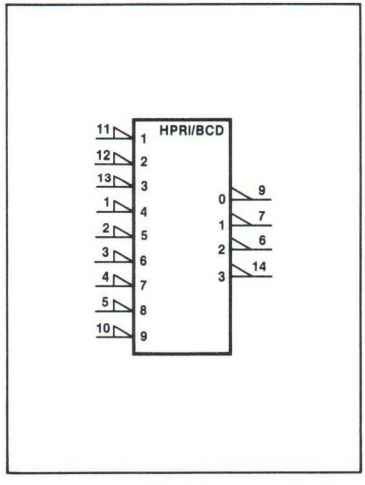
PIN CONFIGURATION



LOGIC SYMBOL

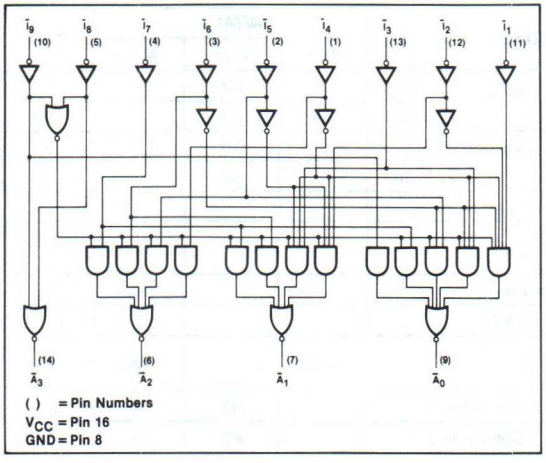


LOGIC SYMBOL (IEEE/IEC)



ENCODER 54/74147

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS			
$\bar{I}_1$	$\bar{I}_2$	$\bar{I}_3$	$\bar{I}_4$	$\bar{I}_5$	$\bar{I}_6$	$\bar{I}_7$	$\bar{I}_8$	$\bar{I}_9$	$\bar{A}_3$	$\bar{A}_2$	$\bar{A}_1$	$\bar{A}_0$
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

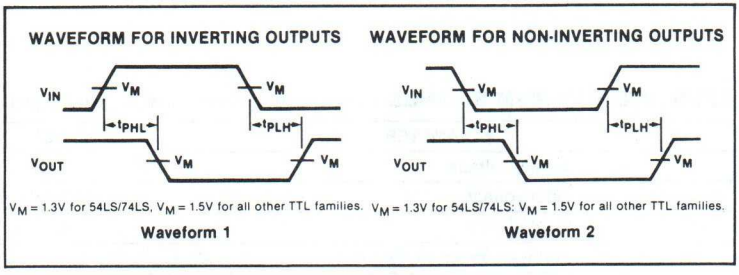
ENCODER 54/74147

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74147 Min	54/74147 Typ[2]	54/74147 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.3		V
			Com'l	2.4	3.3		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−35		−85	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1		50	70	mA
			Condition 2		42	62	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. *Condition 1:* Measure I_{CC} with $\overline{I_7}$ grounded, other inputs and outputs open. *Condition 2:* Measure I_{CC} with all inputs and outputs open.

AC WAVEFORMS

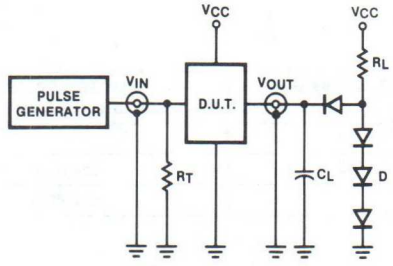


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay	Waveform 1 Out-of-phase output		19 19	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2 In-phase output		14 11	ns

TEST CIRCUITS AND WAVEFORMS

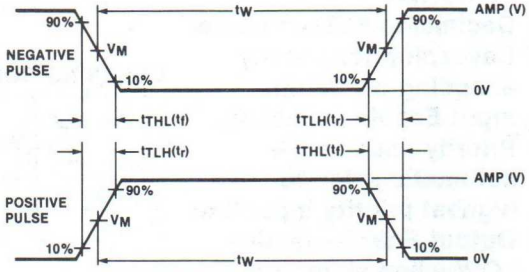
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ENCODER 54/74148

8-Input Priority Encoder

- Code conversions
- Multi-channel D/A converter
- Decimal-to-BCD converter
- Cascading for priority encoding of "N"bits
- Input Enable capability
- Priority encoding—automatic selection of highest priority input line
- Output Enable—active LOW when all inputs HIGH
- Group Signal output—active when any input is LOW

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74148	10ns	38mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74148N	
Ceramic DIP	N74148F	S54148F
Flatpack		S54148W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
$\overline{I}_O$	Input	1ul
$\overline{I}_1$-$\overline{I}_7$	Inputs	2ul
$\overline{EI}$	Input	2ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

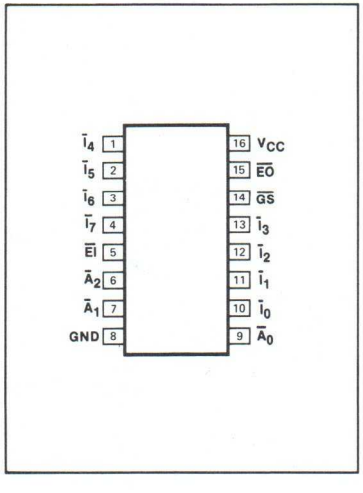
DESCRIPTION

The '148 8-input priority encoder accepts data from eight active-LOW inputs and provides a binary representation on the three active-LOW outputs. A priority is assigned to each input so that when two or more inputs are simultaneously active, the input with the highest priority is represented on the output, with input line $\overline{I}_7$ having the highest priority.

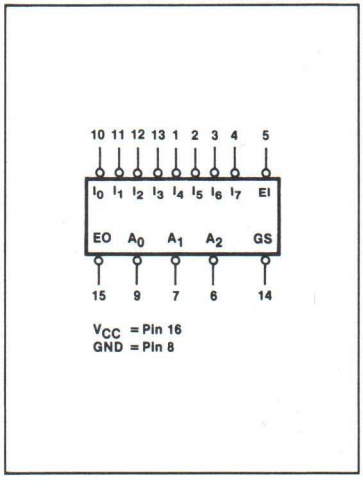
A HIGH on the Enable Input ($\overline{EI}$) will force all outputs to the inactive (HIGH) state and allow new data to settle without producing erroneous information at the outputs.

A Group Signal ($\overline{GS}$) output and an Enable Output ($\overline{EO}$) are provided with the three data outputs. The $\overline{GS}$ is active-LOW when any input is LOW; this indicates when any input is active. The $\overline{EO}$ is active-LOW when all inputs are HIGH. Using the Enable Output along with the Enable Input allows priority encoding of N input signals. Both $\overline{EO}$ and $\overline{GS}$ are active-HIGH when the Enable Input is HIGH.

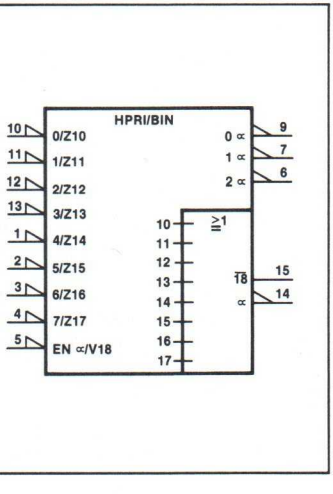
PIN CONFIGURATION



LOGIC SYMBOL

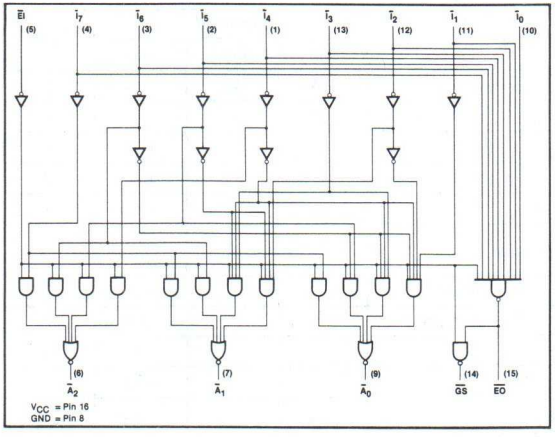


LOGIC SYMBOL (IEEE/IEC)



ENCODER 54/74148

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS				
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	$\overline{GS}$	$\overline{A}_0$	$\overline{A}_1$	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	H	L	L	H
L	X	X	X	X	X	L	H	H	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	L	L	L	H	H
L	X	X	L	H	H	H	H	H	L	H	L	H	H
L	X	L	H	H	H	H	H	H	L	L	H	H	H
L	L	H	H	H	H	H	H	H	L	H	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

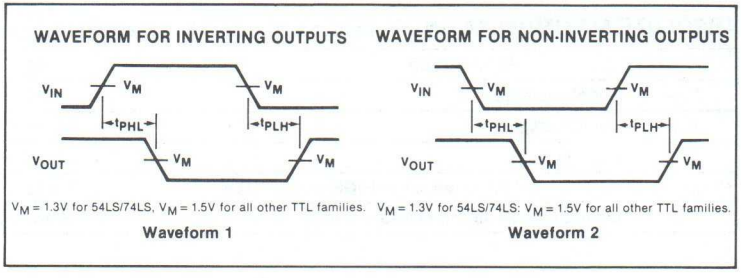
PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74148 Min	54/74148 Typ[2]	54/74148 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.3		V
			Com'l	2.4	3.3		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{I}_O$ input			40	μA
			Other inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{I}_O$ input			– 1.6	mA
			Other inputs			– 3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		– 35		– 85	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1		40	60	mA
			Condition 2		35	55	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. *Condition 1:* Measure I_{CC} with $\overline{I}_O$ and $\overline{EI}$ grounded, other inputs and outputs open. *Condition 2:* Measure I_{CC} with all inputs and outputs open.

AC WAVEFORMS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.
Waveform 1

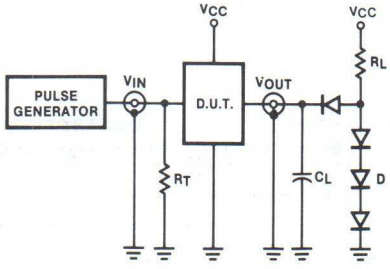
V_M = 1.3V for 54LS/74LS: V_M = 1.5V for all other TTL families.
Waveform 2

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{A}_n$ outputs	Waveform 2, In-phase output		15 14	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{A}_n$ outputs	Waveform 1, Out-of-phase output		19 19	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_N$ input to $\overline{EO}$ output	Waveform 1, Out-of-phase output		10 25	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{I}_n$ input to $\overline{GS}$ output	Waveform 2, In-phase output		30 25	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{A}_n$ outputs	Waveform 2, In-phase output		15 15	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{EO}$ output	Waveform 2, In-phase output		15 30	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{EI}$ input to $\overline{GS}$ output	Waveform 2, In-phase output		12 15	ns

TEST CIRCUITS AND WAVEFORMS

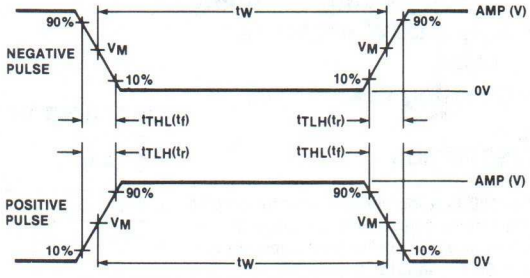
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

MULTIPLEXER 54/74150

16-Input Multiplexer

- **Select data from 16 sources**
- **Demultiplexing capability**
- **Active-LOW enable or strobe**
- **Inverting data output**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74150	17ns	40mA

DESCRIPTION

The '150 is a logical implementation of a single-pole, 16-position switch with the switch position controlled by the state of four Select inputs, S_0, S_1, S_2, S_3. The Multiplexer output ($\overline{Y}$) inverts the selected data. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH the $\overline{Y}$ output is HIGH regardless of all other inputs. In one package the '150 provides the ability to select from 16 sources of data or control information.

ORDERING CODE

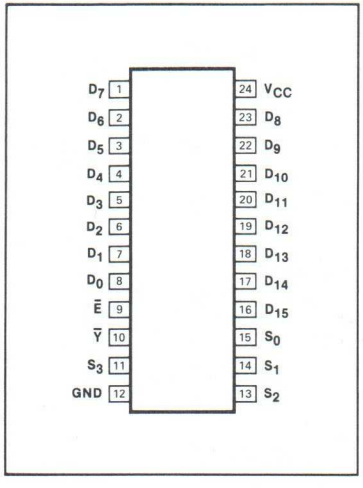
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74150N	
Ceramic DIP	N74150F	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

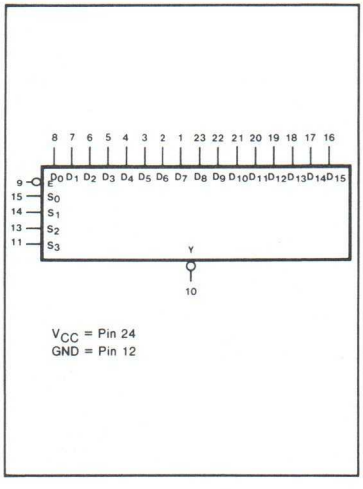
PINS	DESCRIPTION	54/74
All	Inputs	1ul
$\overline{Y}$	Output	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

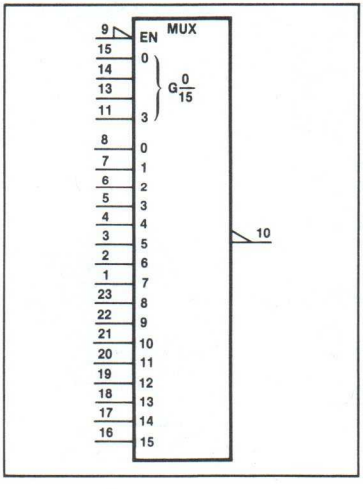
PIN CONFIGURATION



LOGIC SYMBOL

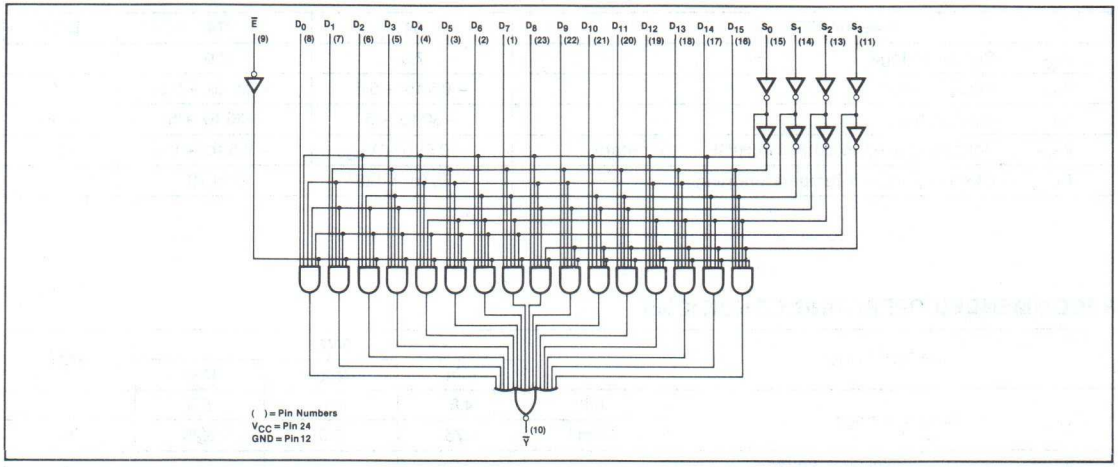


LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXER 54/74150

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS																		OUTPUT
S_3	S_2	S_1	S_0	$\overline{E}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}	D_{11}	D_{12}	D_{13}	D_{14}	D_{15}	$\overline{Y}$
X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	L	L	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	L	H	L	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	L	H	L	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	L	L	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	L	L	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L
L	L	H	H	L	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	X	H
L	L	H	H	L	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	L	L	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	X	H
L	H	L	L	L	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	X	L
L	H	L	H	L	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	X	H
L	H	L	H	L	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	X	L
L	H	H	L	L	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	X	H
L	H	H	L	L	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	X	L
L	H	H	H	L	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	X	H
L	H	H	H	L	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	X	L
H	L	L	L	L	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	X	H
H	L	L	L	L	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	X	L
H	L	L	H	L	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	X	H
H	L	L	H	L	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	X	L
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	X	H
H	L	H	L	L	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	X	L
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	X	H
H	L	H	H	L	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	X	L
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	X	H
H	H	L	L	L	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	X	L
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	X	H
H	H	L	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	X	L
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	X	H
H	H	H	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	X	L
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	L	H
H	H	H	H	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

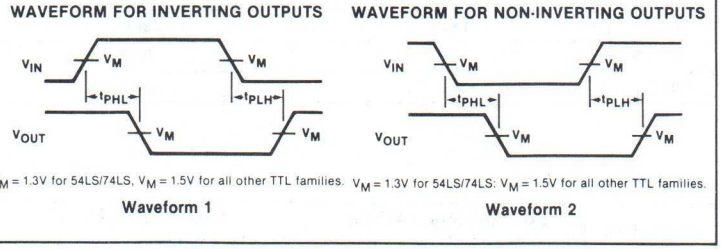
PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74150			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	−20		−55	mA
			Com'l	−18		−55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			40	68	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with $\overline{E}$, S_0-S_3 inputs at 4.5V, all other inputs and outputs open.

AC WAVEFORMS

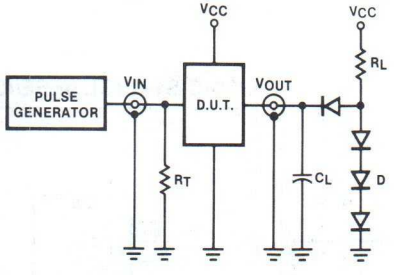


AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		35 33	ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2		24 30	ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		14 20	ns

TEST CIRCUITS AND WAVEFORMS

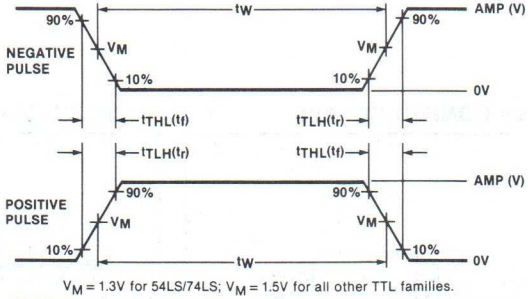
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIPLEXERS 54/74151, LS151, S151

8-Input Multiplexer

- **Multifunction capability**
- **Complementary outputs**
- **See '251 for 3-state version**

TYPE	TYPICAL PROPAGATION DELAY (Enable to $\overline{Y}$)	TYPICAL SUPPLY CURRENT (Total)
74151	18ns	29mA
74LS151	12ns	6mA
74S151	9ns	45mA

DESCRIPTION

The '151 is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. True (Y) and Complement ($\overline{Y}$) outputs are both provided. The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, the $\overline{Y}$ output is HIGH and the Y output is LOW, regardless of all other inputs. The logic function provided at the output is:

$$Y = \overline{E} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

In one package the '151 provides the ability to select from eight sources of data or control information. The device can provide any logic function of four variables and its negation with correct manipulation.

ORDERING CODE

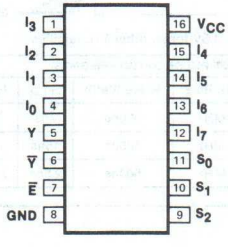
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74151N • N74LS151N N74S151N	
Ceramic DIP	N74151F • N74LS151F N74S151F	S54151F • S54LS151F S54S151F
Flatpack		S54151W • S54LS151W S54S151W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

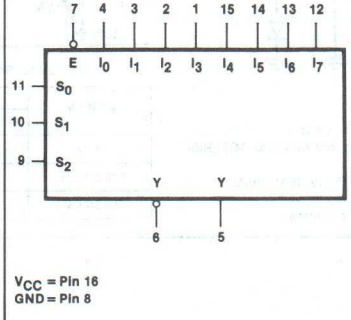
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

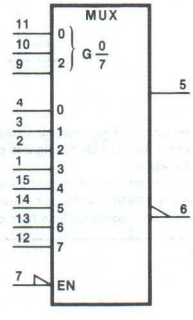
PIN CONFIGURATION



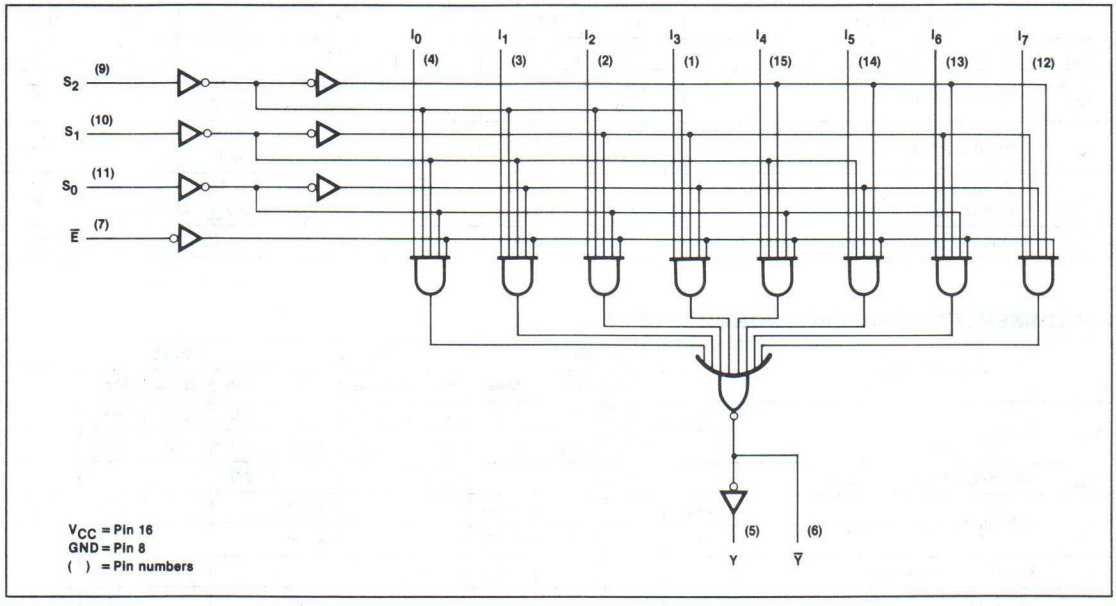
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



3

FUNCTION TABLES

INPUTS												OUTPUTS	
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

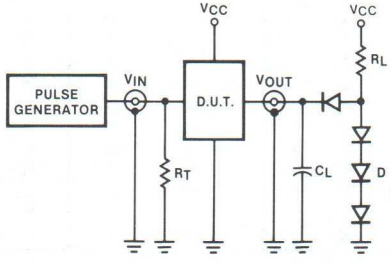
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX FOR 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

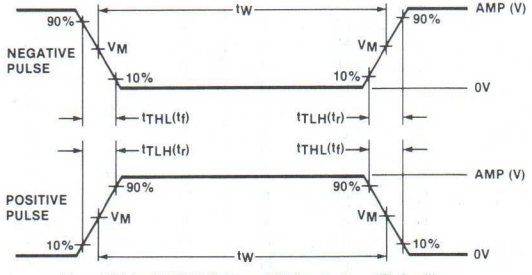
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

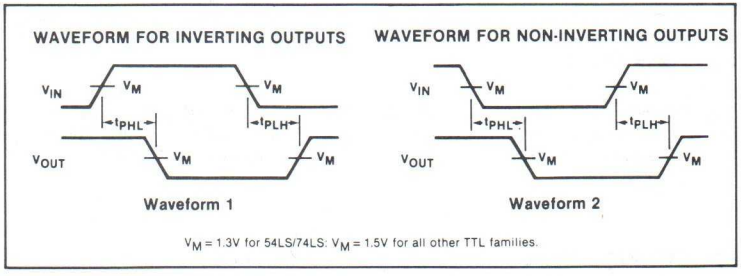
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74151			54/74LS151			54/74S151			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 55	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				29	48		6	10		45	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} on the 54/74151 with $\overline{E}$ and S_0-S_2 at 4.5V, all other inputs and outputs open. Measure I_{CC} on the 54/74LS151 and 54/74S151 with all inputs at 4.5V and outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay Select to Y output	Waveform 2		52		43		18	ns
t_{PHL}				30		30		18	
t_{PLH}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		35		23		15	ns
t_{PHL}				33		32		13.5	
t_{PLH}	Propagation delay Enable to Y output	Waveform 1		52		42		16.5	ns
t_{PHL}				30		32		18	
t_{PLH}	Propagation delay Enable to $\overline{Y}$ output	Waveform 2		24		24		13	ns
t_{PHL}				30		30		12	
t_{PLH}	Propagation delay Data to Y output	Waveform 2		29		32		12	ns
t_{PHL}				24		26		12	
t_{PLH}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		20		21		7.0	ns
t_{PHL}				14		20		7.0	

MULTIPLEXERS 54/74153, LS153, S153

Dual 4-Line To 1-Line Multiplexer

- **Non-inverting outputs**
- **Separate Enable for each section**
- **Common Select inputs**
- **See '253 for 3-State version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74153	18ns	36mA
74LS153	18ns	6.2mA
74S153	9ns	45mA

DESCRIPTION

The '153 is a dual 4-input multiplexer that can select 2 bits of data from up to four sources under control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. Outputs (Y_a, Y_b) are forced LOW when the corresponding Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH.

The device is the logical implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Y_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The '153 can be used to move data to a common output bus from a group of registers. The state of the Select inputs would determine the particular register from which the data came. An alternative application is as a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

ORDERING CODE

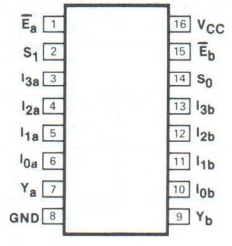
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74153N • N74LS153N N74S153N	
Ceramic DIP	N74153F • N74LS153F N74S153F	S54153F • S54LS153F S54S153F
Flatpack		S54153W • S54LS153W S54S153W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

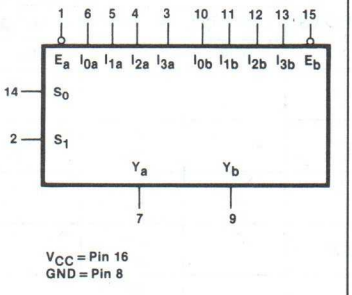
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

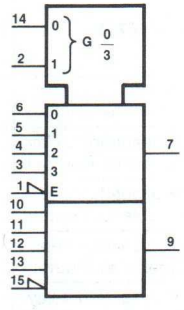
PIN CONFIGURATION



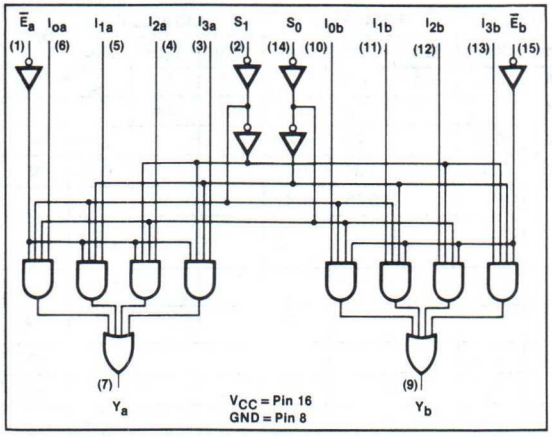
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74153			54/74LS153			54/74S153			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX,	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		36	52		6.2	10		45	70	mA
				Com'l		36	60		6.2	10		45	70	mA

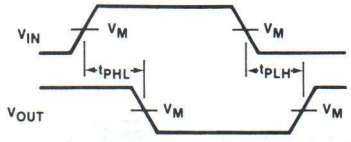
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		54/74S		UNIT
			C_L = 30pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 2		34		29		18	ns
t_{PHL}	Select to output			34		38		18	
t_{PLH}	Propagation delay	Waveform 1		30		24		15	ns
t_{PHL}	Enable to output			23		32		13.5	
t_{PLH}	Propagation delay	Waveform 2		18		15		9.0	ns
t_{PHL}	Data to output			23		26		9.0	

AC WAVEFORMS

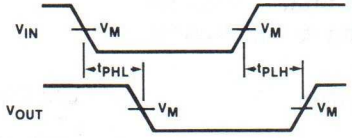
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



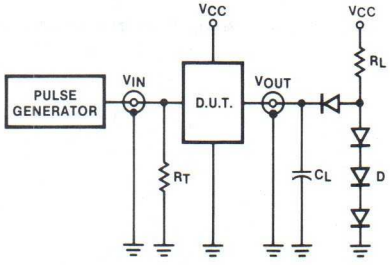
V_M = 1.3V for 54LS/74LS: V_M = 1.5V for all other TTL families.

Waveform 2

3

TEST CIRCUITS AND WAVEFORMS

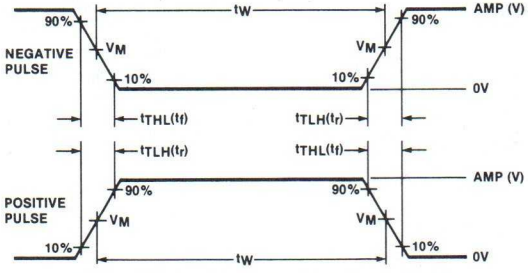
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DECODER/DEMULTIPLEXERS 54/74154, LS154

1-of-16 Decoder/Demultiplexer

- **16-line demultiplexing capability**
- **Mutually exclusive outputs**
- **2-input enable gate for strobing or expansion**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74154	21ns	34mA
74LS154	15ns	9mA

DESCRIPTION

The '154 decoder accepts four active HIGH binary address inputs and provides 16 mutually exclusive active LOW outputs. The 2-input enable gate can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder. The enable gate has two AND'ed inputs which must be LOW to enable the outputs.

The '154 can be used as a 1-of-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable is LOW, the addressed output will follow the state of the applied data.

ORDERING CODE

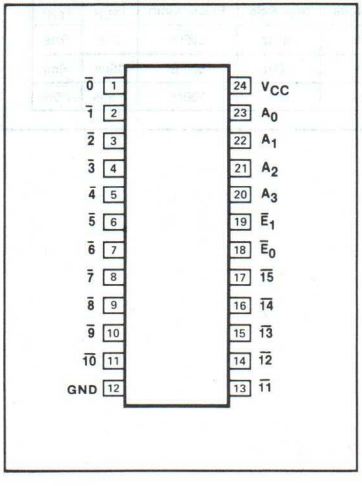
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74154N • N74LS154N	
Ceramic DIP	N74154F • N74LS154F	S54154F • S54LS154F
Flatpack		S54154W • S54LS154W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

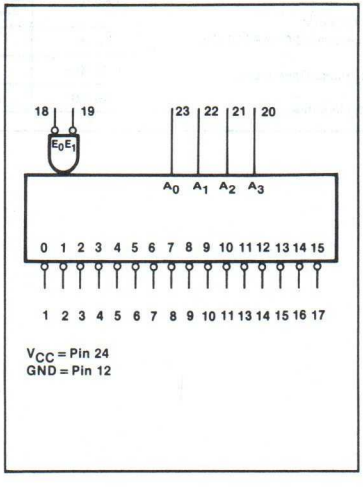
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Ouputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

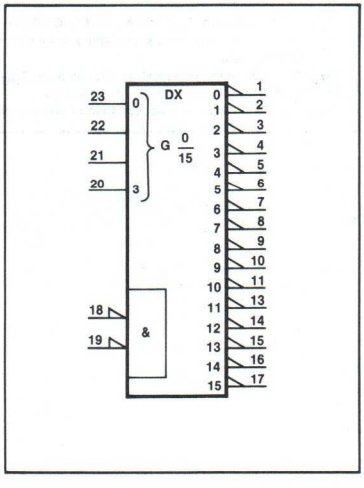
PIN CONFIGURATION



LOGIC SYMBOL

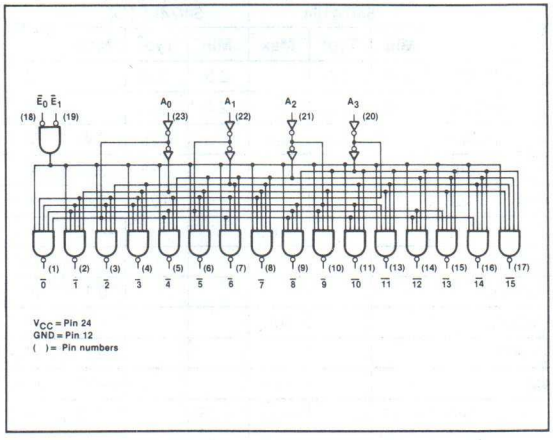


LOGIC SYMBOL (IEEE/IEC)



DECODER/DEMULTIPLEXERS 54/74154, LS154

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS						OUTPUTS															
E_0	E_1	A_3	A_2	A_1	A_0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

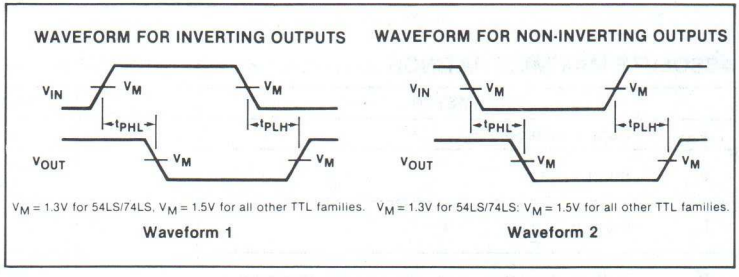
PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74154			54/74LS154			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 15		– 100	mA
				Com'l	– 18		– 57	– 15		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		34	49		9	14	mA
				Com'l		34	56		9	14	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC WAVEFORMS

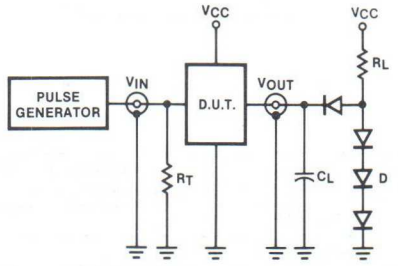


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		36 33		36 33	ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2		30 27		30 27	ns

TEST CIRCUITS AND WAVEFORMS

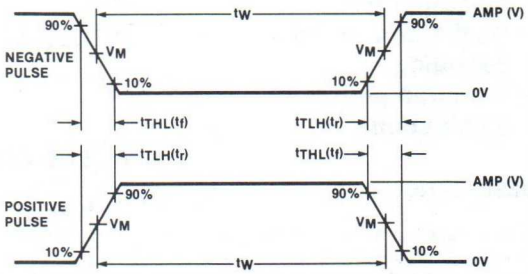
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

DECODERS/DEMULTIPLEXERS 54/74155, LS155

Dual 2-Line To 4-Line Decoder/Demultiplexer

- **Common Address inputs**
- **True or complement data demultiplexing**
- **Dual 1-of-4 or 1-of-8 decoding**
- **Function generator applications**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74155	18ns	25mA
74LS155	17ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74155N • N74LS155N	
Ceramic DIP	N74155F • N74LS155F	

DESCRIPTION

The '155 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and separate gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address input (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\overline{0}$-$\overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

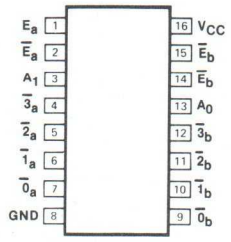
Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

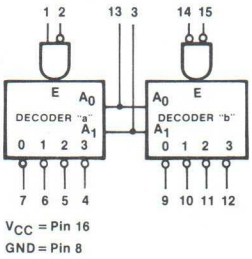
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

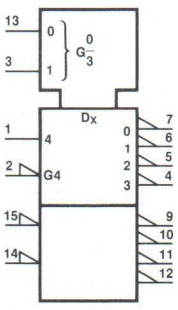
PIN CONFIGURATION



LOGIC SYMBOL

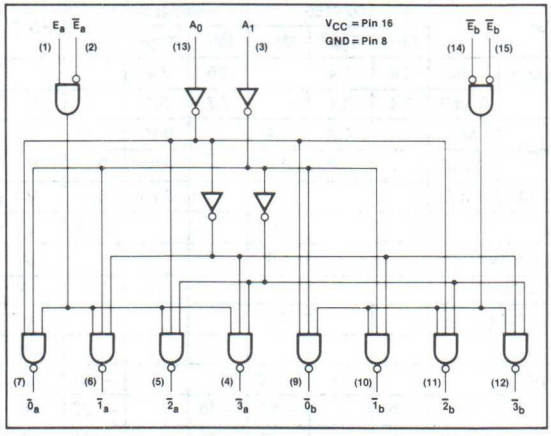


LOGIC SYMBOL (IEEE/IEC)



DECODERS/DEMULTIPLEXERS 54/74155, LS155

LOGIC DIAGRAM



FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	E_b	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

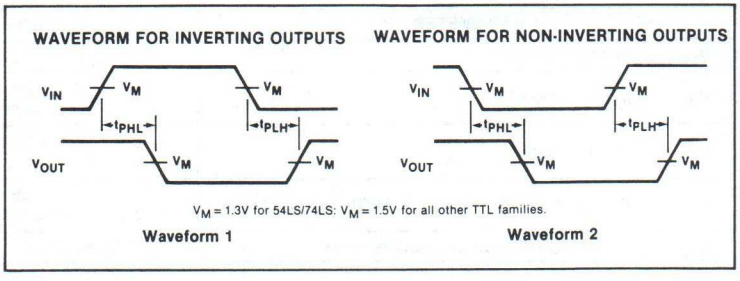
PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74155			54/74LS155			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 55	– 15		– 100	mA
				Com'l	– 18		– 57	– 15		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		25	35		6.1	10	mA
				Com'l		25	40		6.1	10	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with A_1, A_0 and E_a inputs at 4.5V, and $\overline{E}_b$, $\overline{E}_a$ inputs grounded, and outputs open.

AC WAVEFORMS

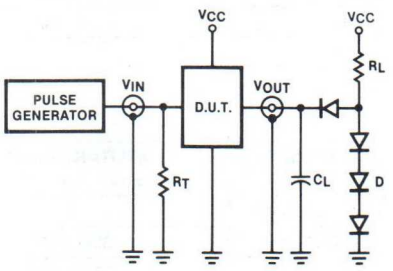


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		32 32		26 30	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_a$ or $\overline{E}_b$ to output	Waveform 2		20 27		15 30	ns
t_{PLH} t_{PHL}	Propagation delay E_a to output	Waveform 1		24 30		27 27	ns

TEST CIRCUITS AND WAVEFORMS

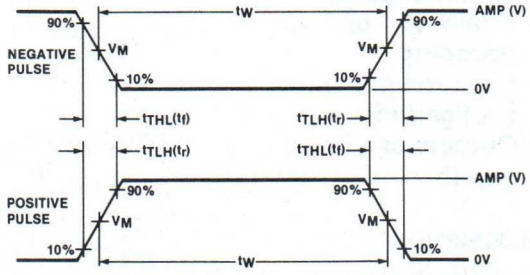
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

DECODERS/DEMULTIPLEXERS 54/74156, LS156

Dual 2-Line To 4-Line Decoder/Demultiplexer (Open Collector)

- **Common Address inputs**
- **True or complement data demultiplexing**
- **Dual 1-of-4 or 1-of-8 decoding**
- **Function generator applications**
- **Outputs can be tied together**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74156	20ns	25mA
74LS156	31ns	6.1mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74156N • N74LS156N	
Ceramic DIP	N74156F • N74LS156F	S54LS156F
Flatpack		S54LS156W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

The '156 is a Dual 1-of-4 Decoder/Demultiplexer with common Address inputs and gated Enable inputs. Each decoder section, when enabled, will accept the binary weighted Address inputs (A_0, A_1) and provide four mutually exclusive active-LOW outputs ($\overline{0}$–$\overline{3}$). When the enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

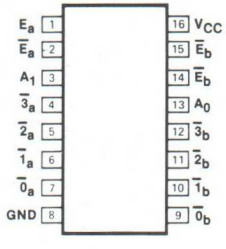
Both decoder sections have a 2-input enable gate. For decoder "a" the enable gate requires one active-HIGH input and one active-LOW input ($E_a \cdot \overline{E}_a$). Decoder "a" can accept either true or complemented data in demultiplexing applications, by using the $\overline{E}_a$ or E_a inputs respectively. The decoder "b" enable gate requires two active-LOW inputs ($\overline{E}_b \cdot \overline{E}_b$). The device can be used as a 1-of-8 decoder/demultiplexer by tying E_a to $\overline{E}_b$ and relabeling the common connection address as (A_2); forming the common enable by connecting the remaining $\overline{E}_b$ and $\overline{E}_a$.

The '156 can be used to generate all four minterms of two variables. The four minterms are useful to replace multiple gate functions in some applications. A further advantage of the '156 is being able to AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown in the formula below:

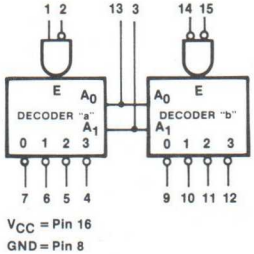
$$f = (E + A_0 + A_1) \cdot (E + \overline{A}_0 + A_1) \cdot (E + A_0 + \overline{A}_1) \cdot (E + A_0 + A_1)$$

where $E = E_a + E_a$; $E = E_b + E_b$.

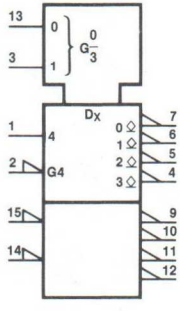
PIN CONFIGURATION



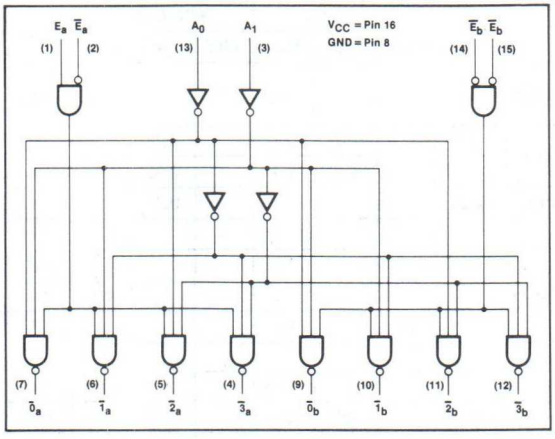
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{E}_b$	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

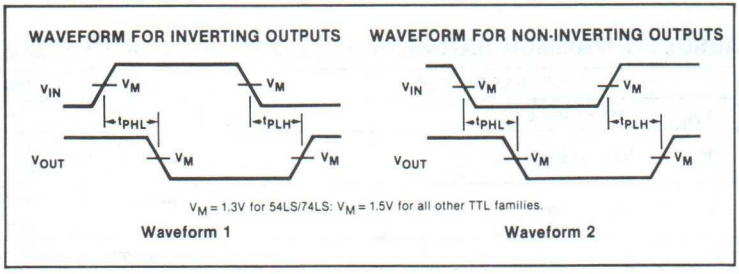
	PARAMETER		54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5	V
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74156			54/74LS156			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					250			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5			− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 1.6			− 0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX		Mil		25	35		6.1	10	mA
				Com'l		25	40		6.1	10	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with A_1, A_0 and E_a inputs at 4.5V, and $\overline{E}_b$, $\overline{E}_a$ inputs grounded, and outputs open.

AC WAVEFORMS

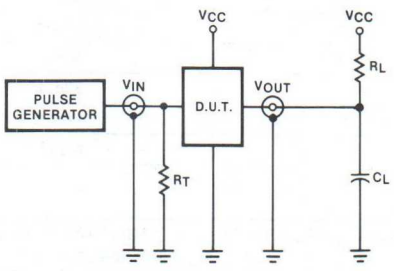


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1		34 34		46 51	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{E}_a$ or $\overline{E}_b$ to output	Waveform 2		23 30		40 51	ns
t_{PLH} t_{PHL}	Propagation delay E_a to output	Waveform 1		27 33		48 48	ns

TEST CIRCUITS AND WAVEFORMS

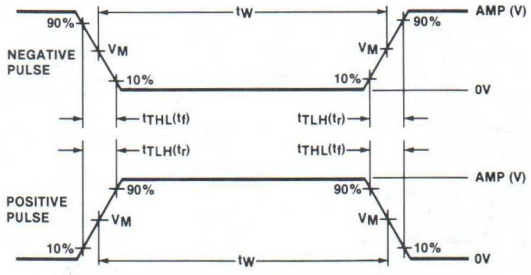
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

'157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
'158 Quad 2-Input Data Selector/Multiplexer (Inverted)

DESCRIPTION

The '157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active LOW. When $\overline{E}$ is HIGH, all of the outputs (Y) are forced LOW regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the '157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The '158 is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74157	13ns	30mA
74LS157	13ns	9.7mA
74S157	7.4ns	50mA
74158	13ns	30mA
74LS158	13ns	4.8mA
74S158	6ns	40mA

ORDERING CODE

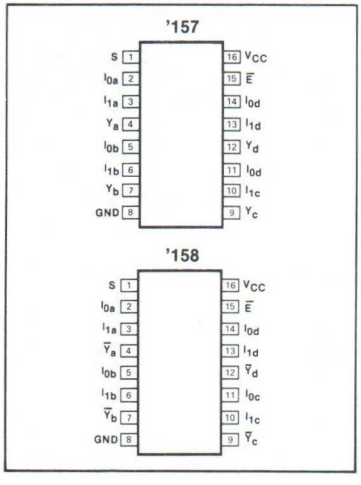
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74157N • N74158N N74S157N • N74LS157N N74S158N • N74LS158N	
Ceramic DIP	N74157F • N74158F N74S157F • N74LS157F N74S158F • N74LS158F	S54157F S54S157F • S54LS157F S54S158F • S54LS158F
Flatpack		S54157W S54S157W • S54LS157W S54S158W • S54LS158W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

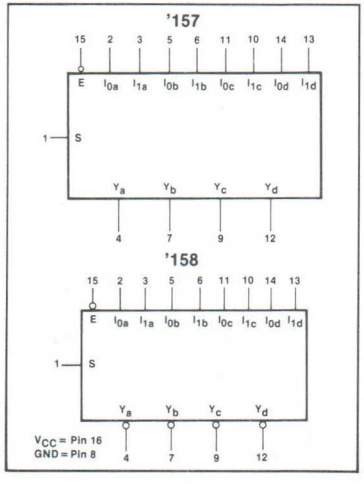
PINS	DESCRIPTION	54/74	54/74S	54/74LS
S, $\overline{E}$	Inputs	1ul	2Sul	2LSul
Data	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

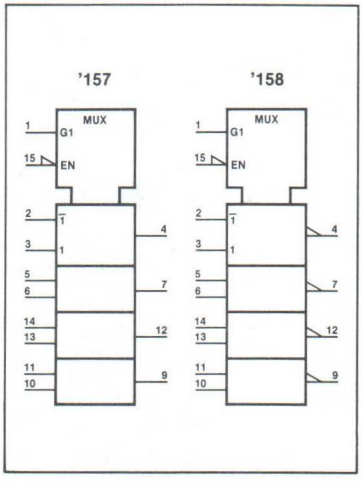
PIN CONFIGURATION



LOGIC SYMBOL

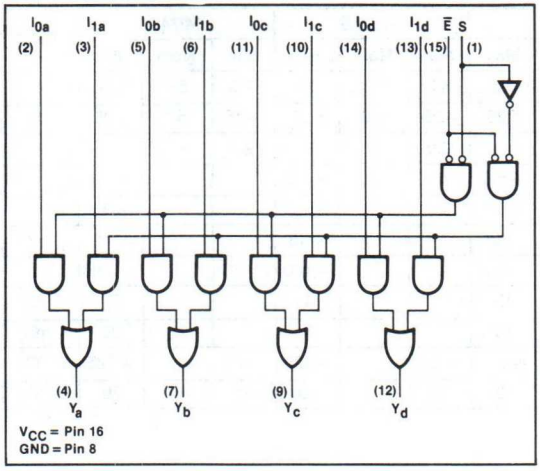


LOGIC SYMBOL (IEEE/IEC)

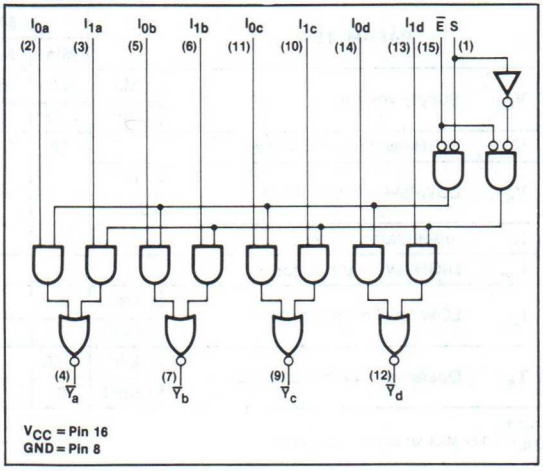


DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

LOGIC DIAGRAM, '157



LOGIC DIAGRAM, '158



FUNCTION TABLE, '157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE, '158

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

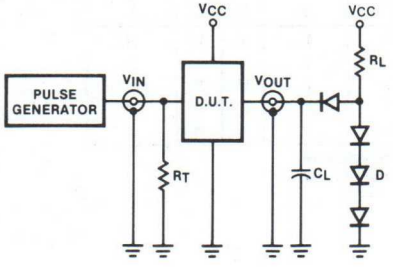
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at +125°C only.

TEST CIRCUITS AND WAVEFORMS

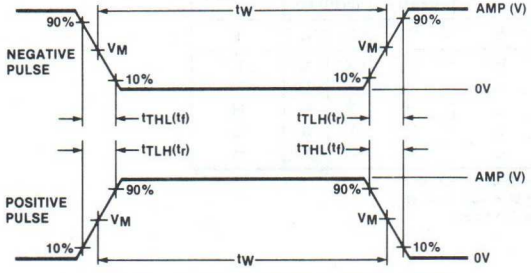
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74157, 158			54/74LS157, 158			54/74S157, 158			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[6]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5			-1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V	S, $\overline{E}$ Inputs						0.2				mA
				Data inputs						0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	S, $\overline{E}$ inputs			40							μA
				Data inputs			40							μA
			V_I = 2.7V	S, $\overline{E}$ inputs						40			100	μA
				Data inputs						20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	S, $\overline{E}$ inputs			-1.6			-0.8				mA
				Data inputs			-1.6			-0.4				mA
			V_I = 0.5V	S, $\overline{E}$ inputs									-4	mA
				Data inputs									-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-55	-20		-100	-40		-100	mA
				Com'l	-18		-55	-20		-100	-40		-100	mA
I_{CC}	Supply current[4,5] (total)	V_{CC} = MAX	Note 4	'157, '158		30	48							mA
			Note 4	'LS157					9.7	16				mA
			Note 4	'LS158					4.8	8				mA
			Note 5	'S157 All inputs = 4.5V								50	78	mA
			Note 5	'S158 All inputs = 4.5V								39	61	mA
			Note 5	'S158 I_{0a}, I_{0b}, I_{0c}, I_{0d} at 4.5V, other inputs at 0V								41	81	mA

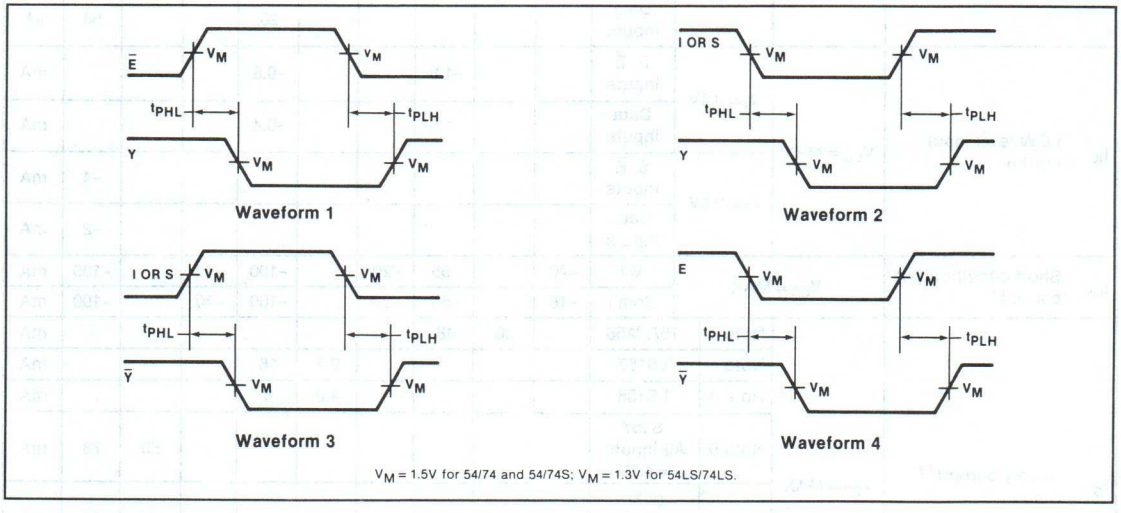
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with 4.5V applied to all inputs and all outputs open.
5. I_{CC} is measured with all outputs open.
6. V_{OL} = +0.45V MAX for 54S at +125°C only.

DATA SELECTORS/MULTIPLEXERS 54/74157, 54/74158, LS157, LS158, S157, S158

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		54S/74S $C_L = 15pF$, $R_L = 280\Omega$		UNIT
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 2, '157		14 14		14 14		7.5 6.5	ns
t_{PLH} Propagation delay t_{PHL} Enable to output	Waveform 1, '157		20 21		20 21		12.5 12	ns
t_{PLH} Propagation delay t_{PHL} Select to output	Waveform 2, '157		23 27		23 27		15 15	ns
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 3, '158		14 14		12 15		6.0 6.0	ns
t_{PLH} Propagation delay t_{PHL} Enable to output	Waveform 4, '158		20 21		17 24		11.5 12	ns
t_{PLH} Propagation delay t_{PHL} Select to output	Waveform 3, '158		23 27		20 24		12 12	ns

AC WAVEFORMS



Waveform 1 Waveform 2 Waveform 3 Waveform 4

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

'160, '162 BCD Decade Counter
'161, '163 4-Bit Binary Counter

- **Synchronous counting and loading**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Asynchronous reset ('160, '161)**
  Synchronous reset ('162, '163)
- **Hysteresis on Clock input (LS only)**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74160-74163	32MHz	61mA
74LS160A-74LS163A	32MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74160N • N74LS160AN N74161N • N74LS161AN N74LS162AN N74163N • N74LS163AN	
Ceramic DIP	N74160F • N74LS160AF N74161F • N74LS161AF N74LS162AF N74163F • N74LS163AF	S54160F • S54LS160AF S54161F • S54LS161AF S54LS162AF S54163F • S54LS163AF
Flatpack		S54160W • S54LS160AW S54161W • S54LS161AW S54LS162AW S54163W • S54LS163AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
CP, CET	Inputs	2ul	2LSul
D, CEP	Inputs	1ul	1LSul
$\overline{PE}$	Input	1ul	2LSul
All	Outputs	10ul	10LSul
$\overline{MR}$	Input ('160, '161)	1ul	1LSul
$\overline{MR}$	Input ('162, '163)	1ul	2LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

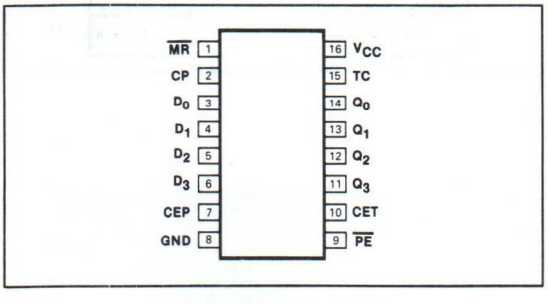
Synchronous presettable decade (54/74160, 54/74LS160A, 54/74LS162A) and 4-bit (54/74161, 54/74LS161A, 54/74163, 54/74LS163A) counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The Clock input is buffered.

The outputs of the counters may be preset to HIGH or LOW level. A LOW level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0–D_3 inputs to be loaded into the counter on the positive-going edge of the clock (providing that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

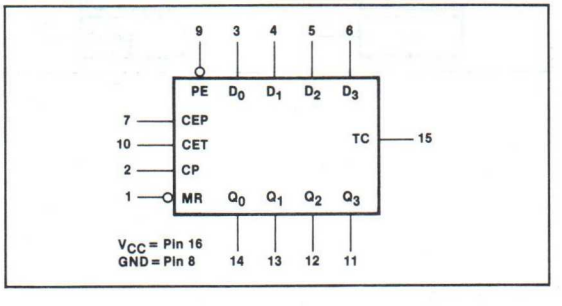
A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0–Q_3) in '160, 'LS160A, '161, and 'LS161A to LOW levels regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function).

For the 'LS162A, '163, and LS163A, the clear function is synchronous. A LOW level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0–Q_3) to LOW levels after the next positive-going transition on the Clock (CP) input (providing that the setup and hold requirements for $\overline{MR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. This synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure A).

PIN CONFIGURATION



LOGIC SYMBOL



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be HIGH to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a HIGH output pulse of a duration approximately equal to the HIGH level output of Q_0. This pulse can be used to enable the next cascaded stage (see Figure B).

For conventional operation of 54/74160, 54/74161 and 54/74163, the following transitions should be avoided.

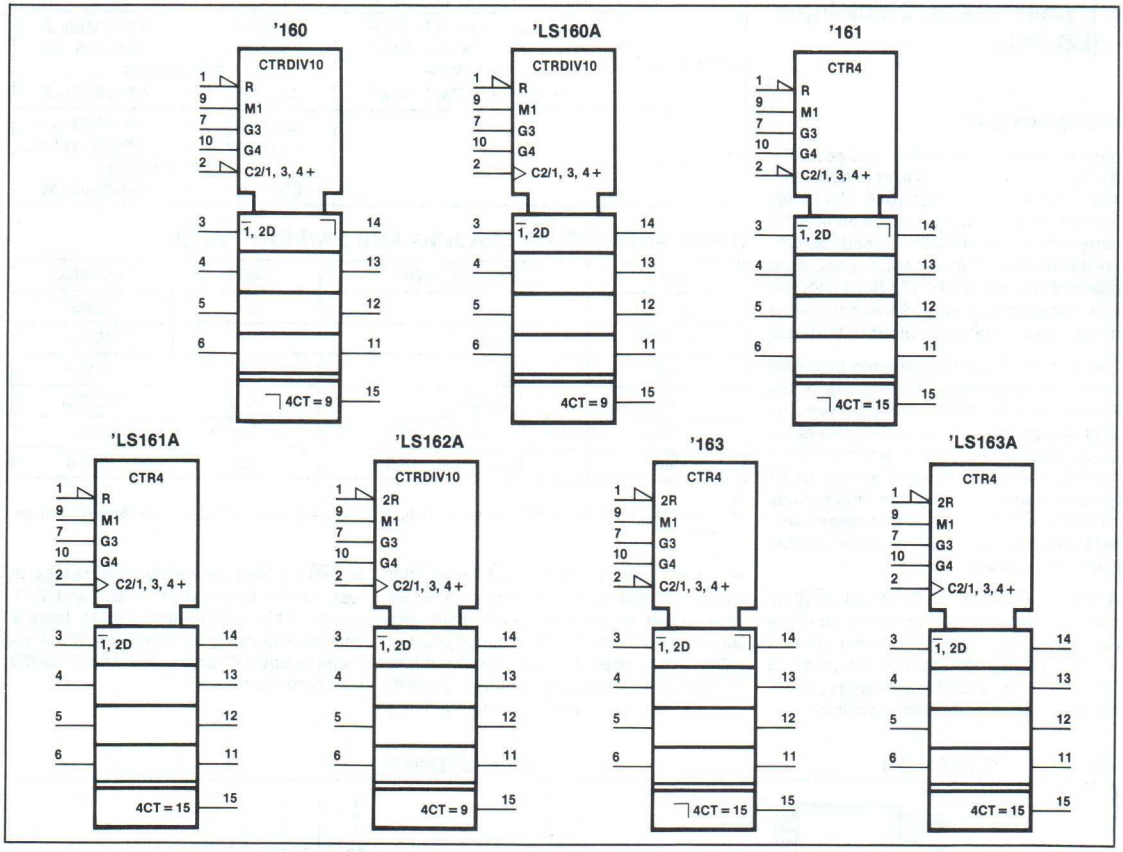
1. HIGH-to-LOW transition on the CEP or CET input if clock is LOW.
2. LOW-to-HIGH transitions on the Parallel Enable input when CP is LOW, if the count enables and $\overline{MR}$ are HIGH at or before the transition.

For 54/74163 there is an additional transition to be avoided.

3. LOW-to-HIGH transition on the $\overline{MR}$ input when clock is LOW, if the Enable and $\overline{PE}$ inputs are HIGH at or before the transition.

These restrictions are not applicable to 54/74LS160A, 54/74LS161A, 54/74LS162A and 54/74LS163A.

LOGIC SYMBOL (IEEE/IEC)



COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

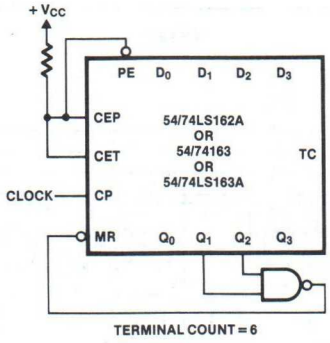


Figure A

SYNCHRONOUS MULTISTAGE COUNTING SCHEME

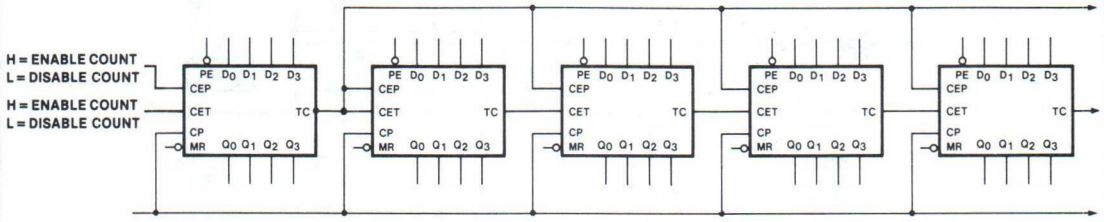
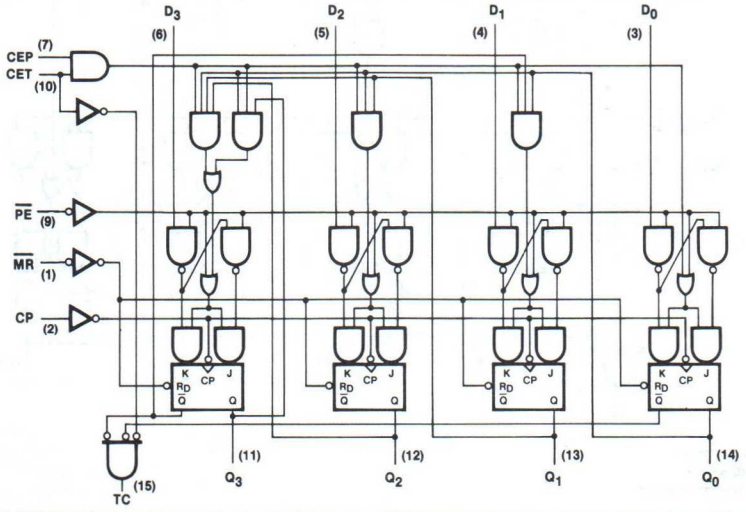


Figure B

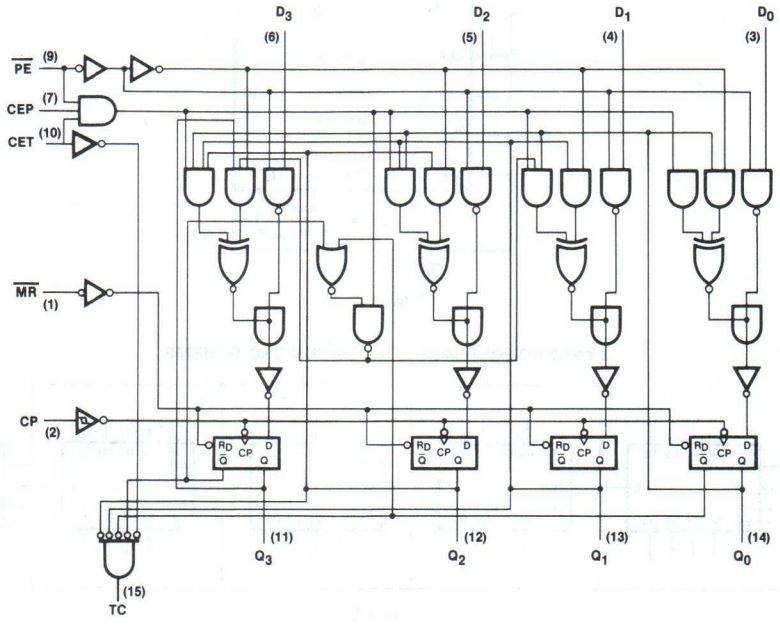
LOGIC DIAGRAM, 54/74160



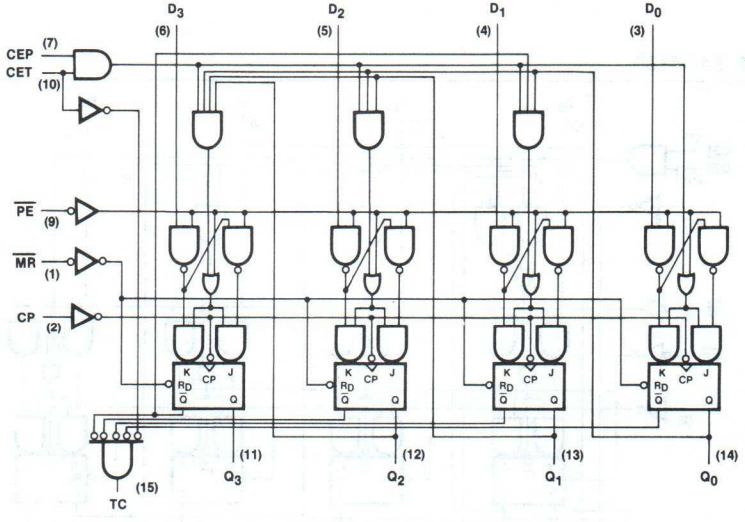
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS

'LS160A



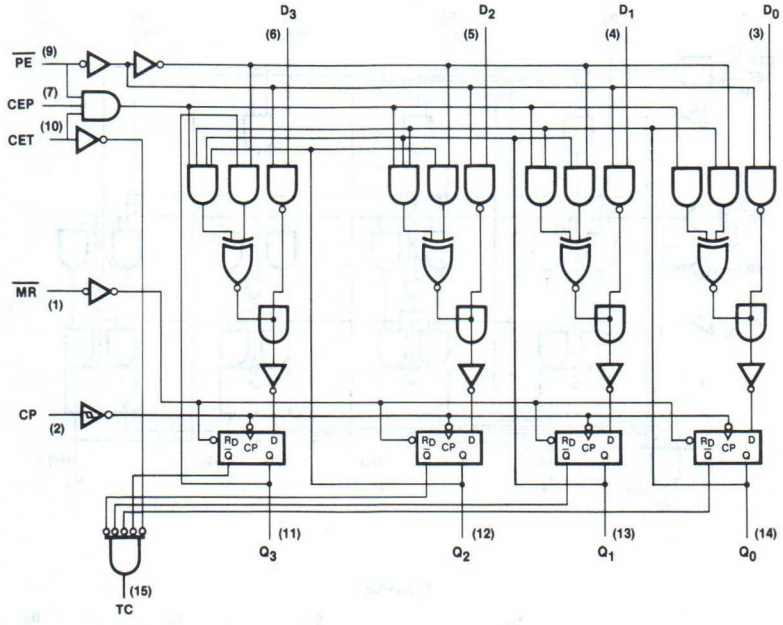
'161



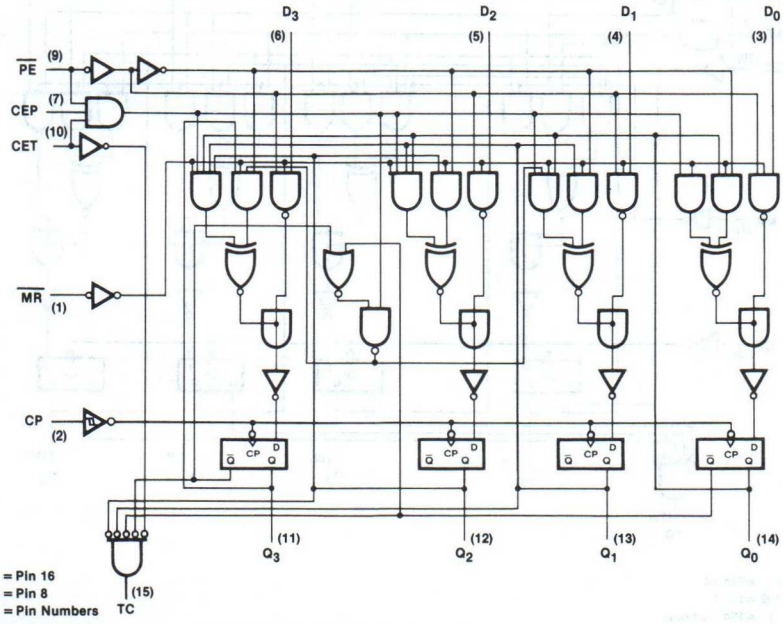
V_{CC} = Pin 16
GND = Pin 8
( ) = Pin numbers

LOGIC DIAGRAMS

'LS161A



'LS162A

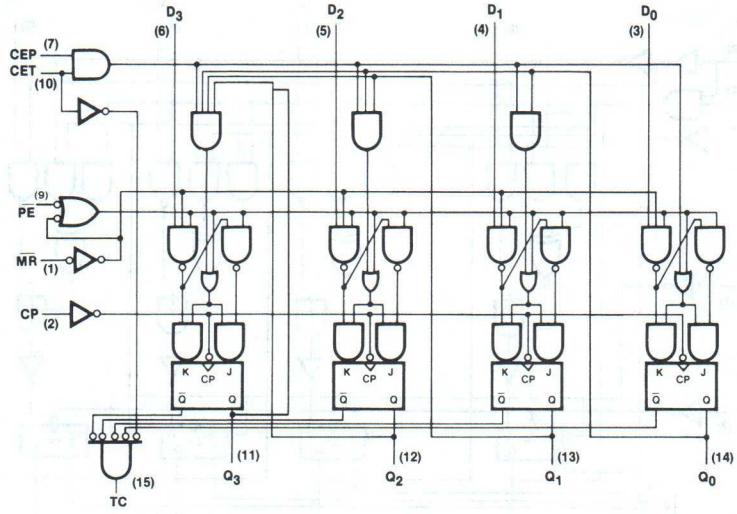


V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

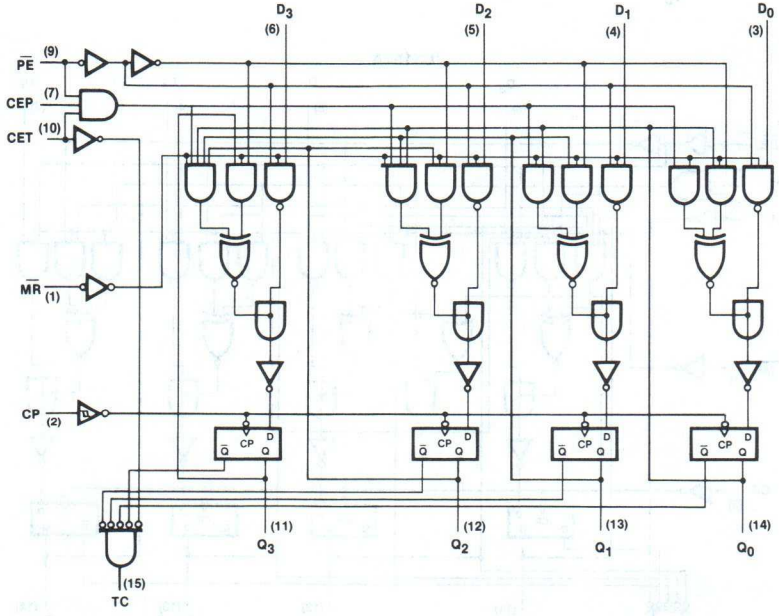
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

LOGIC DIAGRAMS

'163



'LS163A



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

MODE SELECT—FUNCTION TABLE, '160, '161

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	L	X	X	X	X	X	L	L
Parallel Load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(a)
Count	H	↑	h	h	h(c)	X	count	(a)
Hold (do nothing)	H	X	l(b)	X	h(c)	X	q_n	(a)
	H	X	X	l(b)	h(c)	X	q_n	L

MODE SELECT—FUNCTION TABLE, '162, '163

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (Clear)	l	↑	X	X	X	X	L	L
Parallel Load	h(f)	↑	X	X	l	l	L	L
	h(f)	↑	X	X	l	h	H	(d)
Count	h(f)	↑	h	h	h(f)	X	count	(d)
Hold (do nothing)	h(f)	X	l(e)	X	h(f)	X	q_n	(d)
	h(f)	X	X	l(e)	h(f)	X	q_n	L

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTES
(a) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HHHH for '161 and HLLH for '160).
(b) The HIGH-to-LOW transition of CEP or CET on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(c) The LOW-to-HIGH transition of $\overline{PE}$ on the 54/74161 and 54/74160 should only occur while CP is HIGH for conventional operation.
(d) The TC output is HIGH when CET is HIGH and the counter is at Terminal Count (HLLH for '162 and HHHH for '163).
(e) The HIGH-to-LOW transition of CEP or CET on the 54/74163 should only occur while CP is HIGH for conventional operation.
(f) The LOW-to-HIGH transition of $\overline{PE}$ or $\overline{MR}$ on the 54/74163 should only occur while CP is HIGH for conventional operation.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

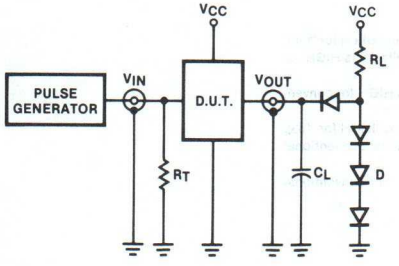
COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7	V
		Com'l			+ 0.8			+ 0.8	V
I_{IK}	Input clamp current				− 12			− 18	mA
I_{OH}	HIGH-level output current				− 800			− 400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	− 55		+ 125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

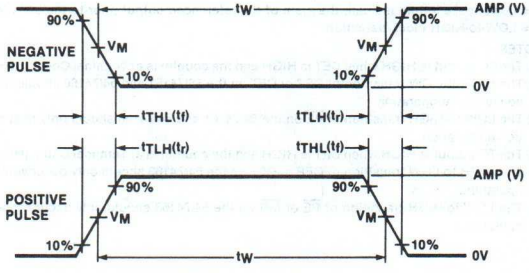
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/74160, '161 '163			54/74LS160A, '161A '162A, '163A			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
		V_I = 7.0V	D, CEP						0.1	mA
			$\overline{PE}$, CP, CET						0.2	mA
			$\overline{MR}$ ('LS160A, 'LS161A)						0.1	mA
			$\overline{MR}$ ('LS162A, 'LS163A)						0.2	mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	CP, CET			80				μA
			Other inputs			40				μA
		V_I = 2.7V	D, CEP						20	μA
			$\overline{PE}$, CP, CET						40	μA
			$\overline{MR}$ ('LS160A, 'LS161A)						20	μA
			$\overline{MR}$ ('LS162A, ('LS163A)						40	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V	CP, CET			-3.2				mA
			Other inputs			-1.6				mA
		V_I = 0.4V	D, CEP						-0.4	mA
			$\overline{PE}$, CP, CET						-0.8	mA
			$\overline{MR}$ ('LS160A, 'LS161A)						-0.4	mA
			$\overline{MR}$ ('LS162A, 'LS163A)						-0.8	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-57	-20		-100	mA
			Com'l	-18		-57	-20		-100	mA
I_{CC} Supply current[4] (total)	V_{CC} = MAX	I_{CCH} All outputs HIGH	Mil		59	85		18	31	mA
			Com'l		59	94		18	31	mA
		I_{CCL} All outputs LOW	Mil		63	91		19	32	mA
			Com'l		63	101		19	32	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CCH} is measured with $\overline{PE}$ input HIGH, again with $\overline{PE}$ input LOW, all other inputs HIGH and outputs open. I_{CCL} is measured with Clock input HIGH, again with Clock input LOW, all other inputs low and outputs open.

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			$C_L = 15pF$, $R_L = 400\Omega$		$C_L = 15pF$, $R_L = 2k\Omega$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Terminal Count	Waveform 1		35 35		35 35	ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = HIGH		20 23		24 27	ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q outputs	Waveform 1, PE = LOW		25 29		24 27	ns
t_{PLH} t_{PHL}	Propagation delay CET input to TC output	Waveform 2		16 16		16 25	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to Q outputs ('160, '161)	Waveform 3		38		28	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

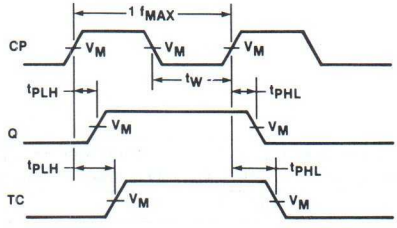
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	25		25		ns
t_W	Master Reset pulse width ('160, '161)	Waveform 3	20		20		ns
t_W	Master Reset pulse width ('162, '163)	Waveform 6	20		20		ns
t_s	Setup time, Data to Clock	Waveform 5	20		20		ns
t_h	Hold time, Data to Clock	Waveform 5	0		0		ns
t_s	Setup time, CEP or CET to Clock	Waveform 4	20		20		ns
t_h	Hold time, CEP or CET to Clock	Waveform 4	0		0		ns
t_s	Setup time, $\overline{PE}$ to Clock	Waveform 5	25		20		ns
t_h	Hold time, $\overline{PE}$ to Clock	Waveform 5	0		0		ns
t_s	Setup time, $\overline{MR}$ to Clock ('162, '163)	Waveform 6	20		20		ns
t_h	Hold time, $\overline{MR}$ to Clock ('162, '163)	Waveform 6	0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		15		ns

COUNTERS 54/74160, 54/74161, 54/74163, LS160A, LS161A, LS162A, LS163A

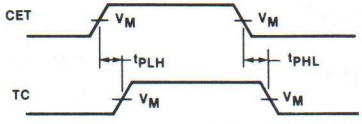
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS, MAXIMUM FREQUENCY, AND CLOCK PULSE WIDTH



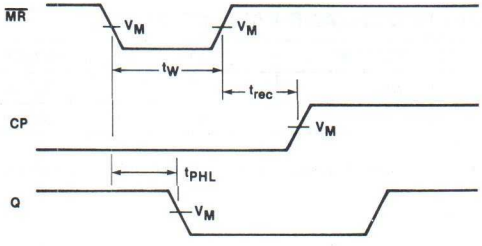
Waveform 1

PROPAGATION DELAYS CET INPUT TO TC OUTPUT



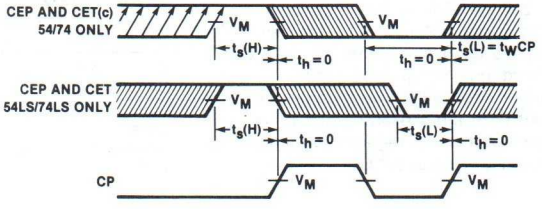
Waveform 2

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME ('160, '161)



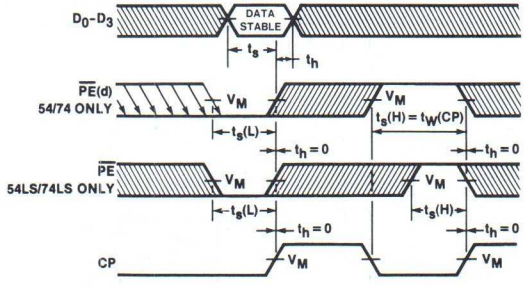
Waveform 3

CEP AND CET SETUP AND HOLD TIMES



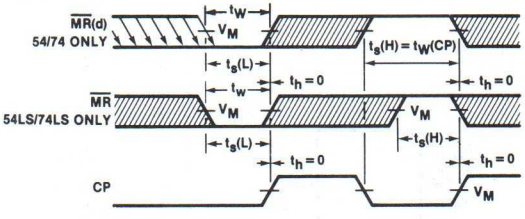
Waveform 4

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



Waveform 5

SYNCHRONOUS RESET SETUP, PULSE WIDTH AND HOLD TIMES ('162, '163)



Waveform 6

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

SHIFT REGISTERS 54/74164, LS164

8-Bit Serial-In Parallel-Out Shift Register

- **Gated serial Data inputs**
- **Typical shift frequency of 36MHz**
- **Asynchronous Master Reset**
- **Fully buffered Clock and Data inputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74164	36MHz	37mA
74LS164	36MHz	16mA

DESCRIPTION

The '164 is an 8-bit edge-triggered shift register with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (D_{sa} or D_{sb}); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the Clock (CP) input, and enters into Q_0 the logical AND of the two Data inputs ($D_{sa} \cdot D_{sb}$) that existed one setup time before the rising clock edge. A LOW level on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

ORDERING CODE

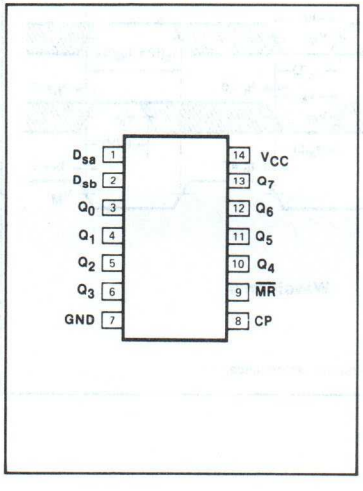
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74164N • N74LS164N	
Ceramic DIP	N74164F • N74LS164F	S54164F • S54LS164F
Flatpack		S54LS164W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

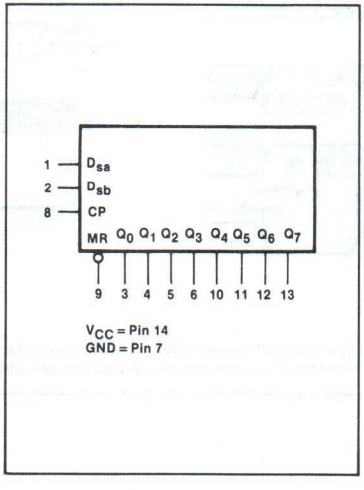
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Ouputs	5ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

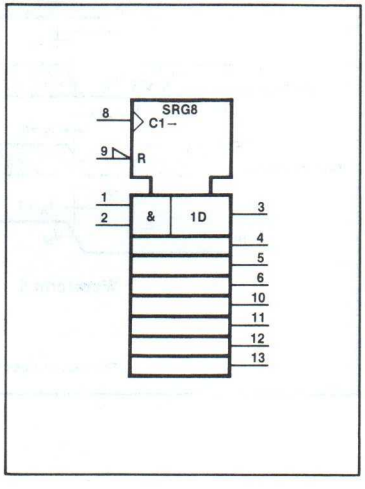
PIN CONFIGURATION



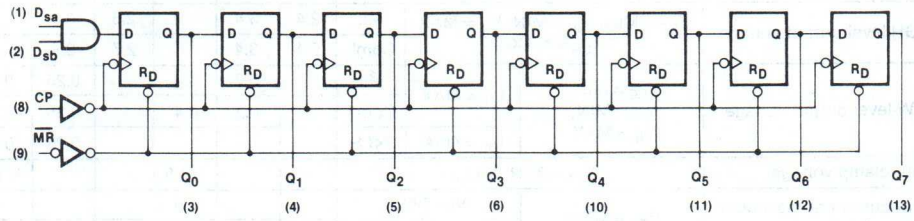
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—TRUTH TABLE

OPERATING MODE	INPUTS				OUTPUTS			
	$\overline{MR}$	CP	D_{sa}	D_{sb}	Q_0	Q_1	—	Q_7
Reset (Clear)	L	X	X	X	L	L	—	L
Shift	H	↑	l	l	L	q_0	—	q_6
	H	↑	l	h	L	q_0	—	q_6
	H	↑	h	l	L	q_0	—	q_6
	H	↑	h	h	H	q_0	—	q_6

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
q = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

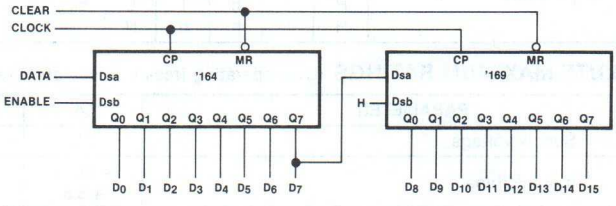
PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−400			−400	μA
I_{OL}	LOW-level output current	Mil			8			4	mA
		Com'l			8			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74164			54/74LS164			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 10		– 27.5	– 20		– 100	mA
				Com'l	– 9		– 27.5	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				37	54		16	27	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the Serial inputs grounded, the Clock input at 2.4V, and a momentary ground, then 4.5V applied to Master Reset, and all outputs open.

APPLICATION



The '164 can be cascaded to form synchronous shift registers of longer length. here, two devices are combined to form a 16-bit shift register

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54/74 C_L = 15pF, R_L = 800Ω		54/74LS C_L = 15pF, R_L = 2kΩ		UNIT
				Min	Max	Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1		25		25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1			27 32		27 32	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2			36		36	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	C_L = 50pF for these parameters	Waveform 1		30 37			ns
t_{PHL}	Propagation delay $\overline{MR}$ to output		Waveform 2		42			ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

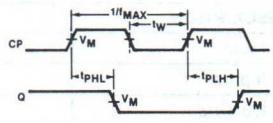
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54/74LS		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		20		ns
t_s	Setup time Data to Clock	Waveform 3	15		15		ns
t_h	Hold time Data to Clock	Waveform 3	5.0		5.0		ns
t_{rec}	$\overline{MR}$ to Clock recovery time	Waveform 2	30		30		ns

3

AC WAVEFORMS

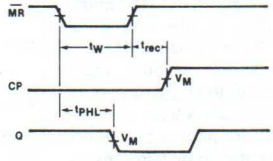
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

Waveform 1

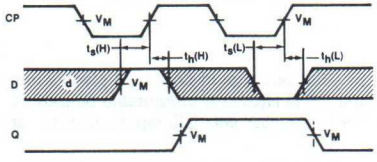
MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

Waveform 2

DATA SETUP AND HOLD TIMES



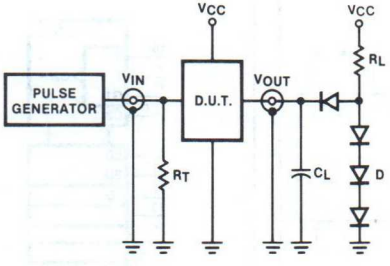
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

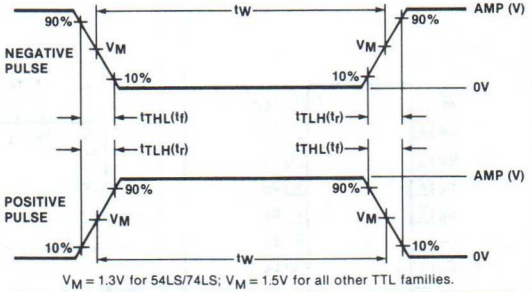
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER 54/74165

8-Bit Serial/Parallel-In, Serial-Out Shift Register

- **Asynchronous 8-bit parallel load**
- **Synchronous Serial input**
- **Clock Enable for "do nothing" mode**
- **See '166 for fully synchronous operation**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74165	26MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74165N	
Ceramic DIP	N74165F	S54165F
Flatpack		S54165W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
$\overline{PL}$	Input	2ul
Other	Inputs	1ul
All	Outputs	10ul

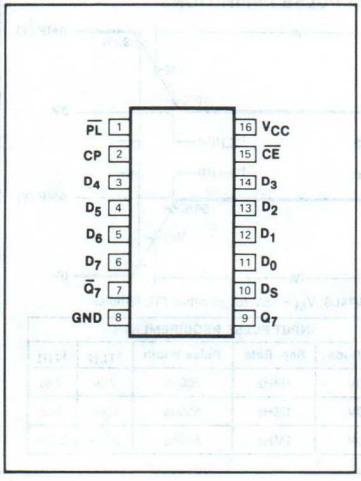
NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

DESCRIPTION

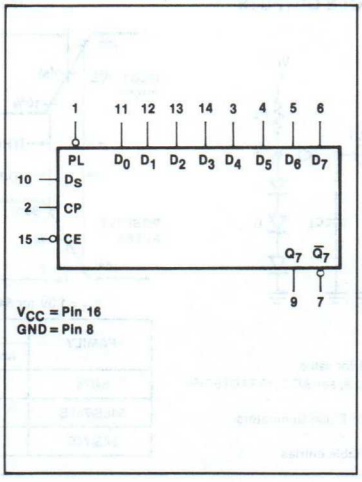
The '165 is an 8-bit parallel load or serial-in shift register with complementary Serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the Parallel Load ($\overline{PL}$) input is LOW, parallel data from the D_0–D_7 inputs are loaded into the register asynchronously. When the $\overline{PL}$ input is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The Clock input is a gated-OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation. Also, the CP and $\overline{CE}$ inputs should be LOW before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is released.

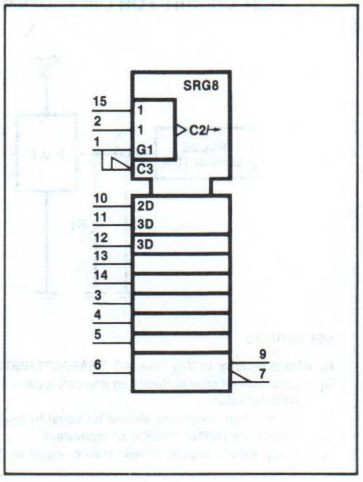
PIN CONFIGURATION



LOGIC SYMBOL

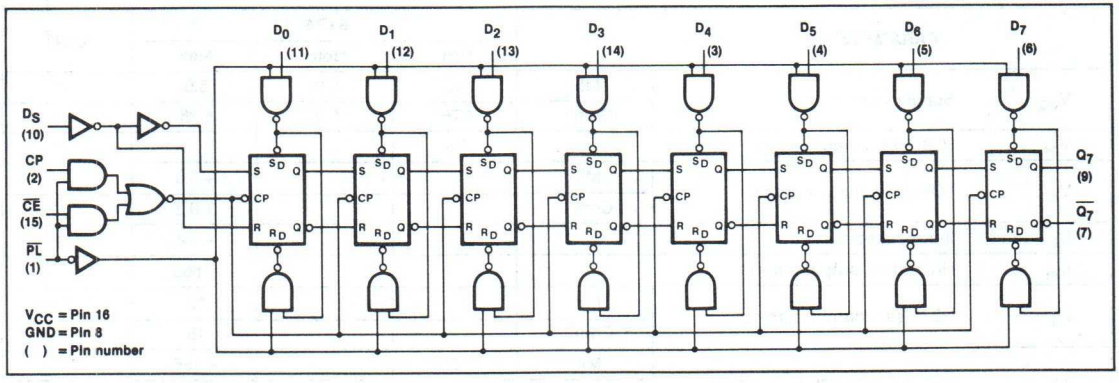


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/74165

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7	$\overline{Q}_7$
Parallel load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial shift	H	L	↑	l	X	L	q_0-q_5	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	q_0-q_5	q_6	$\overline{q}_6$
Hold "do nothing"	H	H	X	X	X	q_0	q_1-q_6	q_7	$\overline{q}_7$

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74165			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OL} = MAX		Mil		0.2	0.4	V
				Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{PL}$ input				80	μA
			Other inputs				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{PL}$ input				−3.2	mA
			Other inputs				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	−20		−55	mA
				Com'l	−18		−55	mA
I_{CC}	Supply Current[4] (total)	V_{CC} = MAX				42	63	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With the outputs open, $\overline{CE}$ and CP at 4.5V, and a clock pulse applied to the $\overline{PL}$ input, I_{CC} is measured first with the Parallel Data inputs at 4.5V, then with the Parallel Data inputs grounded.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		UNIT
			Min	Max	
f_{MAX}	Maximum shift frequency	Waveform 1	20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		24 31	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 2		31 40	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to Q_7	Waveform 3		17 36	ns
t_{PLH} t_{PHL}	Propagation delay D_7 to $\overline{Q}_7$	Waveform 3		27 27	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

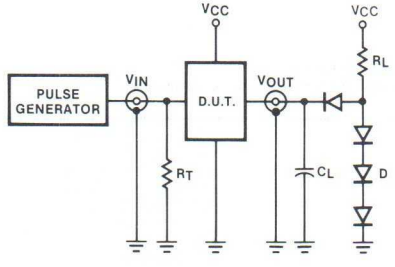
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	25		ns
t_W	$\overline{PL}$ pulse width	Waveform 2	15		ns
t_s	Setup time, D_S to clock	Waveform 4	20		ns
t_h	Hold time, D_S to clock	Waveform 4	0		ns
$t_s(L)$	Setup time, LOW $\overline{CE}$ to clock	Waveform 4	30		ns
t_h	Hold time, $\overline{CE}$ to clock	Waveform 4	0		ns
t_s	$\overline{PL}$ setup time to clock	Waveform 2	45		ns
t_s	Setup time, D_5 and D_7[(a)] to $\overline{PL}$	Waveform 5	10		ns

NOTE
(a) The remaining six Data inputs and D_S are LOW. Prior to test, HIGH level data is loaded into D_7 input.

TEST CIRCUITS AND WAVEFORMS

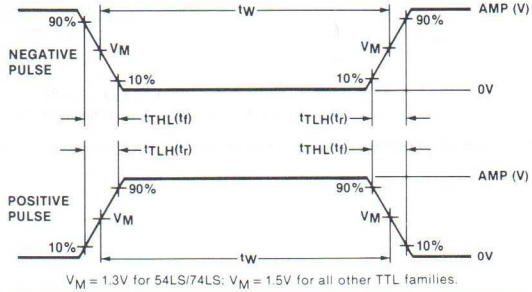
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

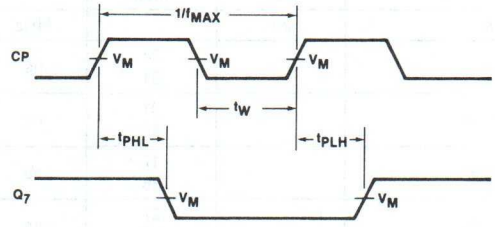


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

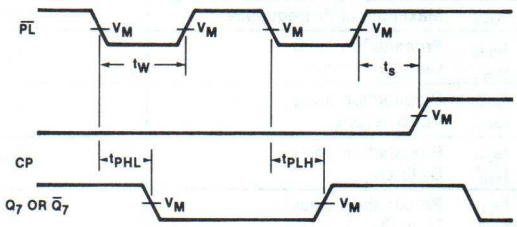
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



PARALLEL LOAD PULSE WIDTH, $\overline{PL}$ TO OUTPUT DELAYS, AND $\overline{PL}$ TO CLOCK SETUP TIME

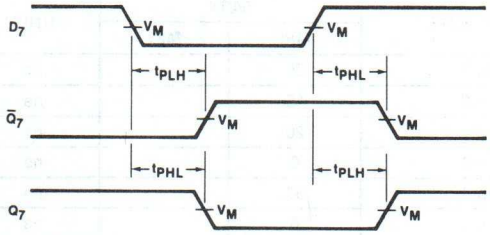


The changing output assumes internal Q_6 opposite state from Q_7.

Waveform 1

Waveform 2

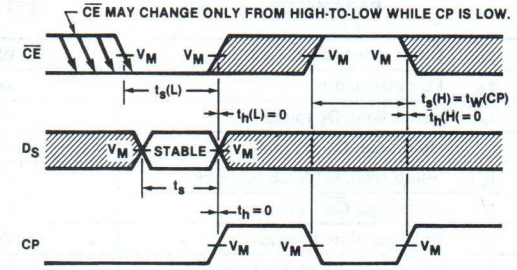
PARALLEL DATA TO OUTPUT DELAYS



CONDITIONS: $\overline{PL}$ = LOW

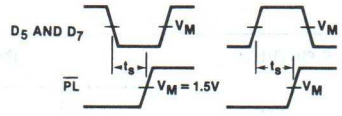
Waveform 3

CLOCK ENABLE AND SERIAL DATA SETUP AND HOLD TIMES



Waveform 4

SETUP TIMES TO ACTIVE LOW PARALLEL LOAD



Waveform 5

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

SHIFT REGISTER 54/74166

8-Bit Serial/Parallel-In, Serial-Out Shift Register

- **Synchronous parallel to serial applications**
- **Synchronous serial data input for easy expansion**
- **Clock enable for "do nothing" mode**
- **Asynchronous Master Reset**
- **See '165 for asynchronous parallel data load**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74166	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74166N	
Ceramic DIP	N74166F	S54166F
Flatpack		S54166W

DESCRIPTION

The '166 is an 8-bit shift register that has fully synchronous serial or parallel data entry selected by an active LOW Parallel Enable ($\overline{PE}$) input. When the $\overline{PE}$ is LOW one setup time before the LOW-to-HIGH clock transition, parallel data is entered into the register. When $\overline{PE}$ is HIGH, data is entered into internal bit position Q_0 from Serial Data input (D_S), and the remaining bits are shifted one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. For expansion of the register in parallel to serial converters, the Q_7 output is connected to the D_S input of the succeeding stage.

The clock input is a gated OR structure which allows one input to be used as an active LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for predictable operation.

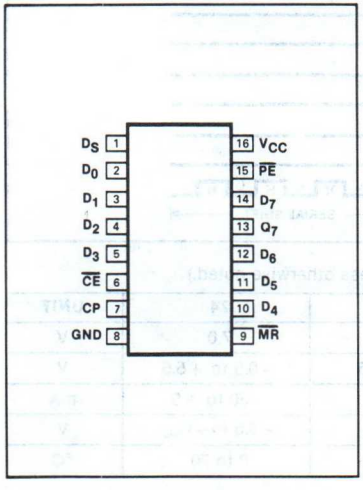
A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

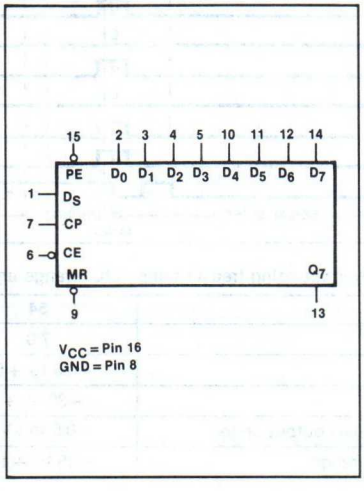
PINS	DESCRIPTION	54/74
All	Inputs	1ul
Q_7	Output	10ul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

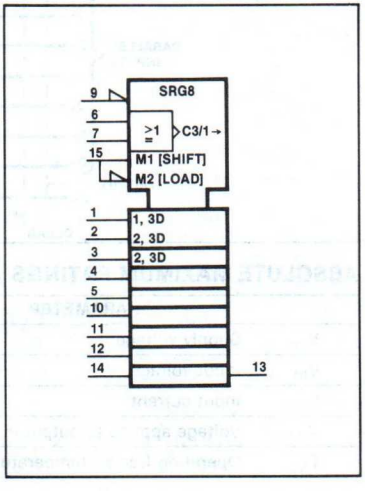
PIN CONFIGURATION



LOGIC SYMBOL

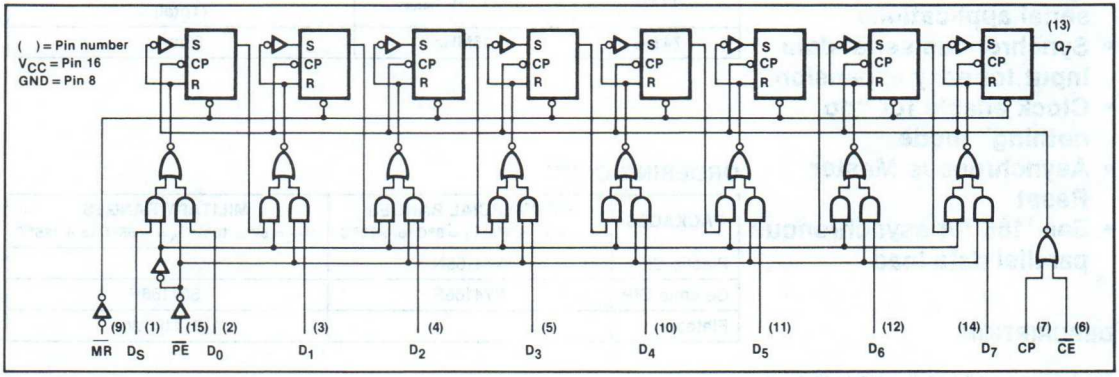


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/74166

LOGIC DIAGRAM

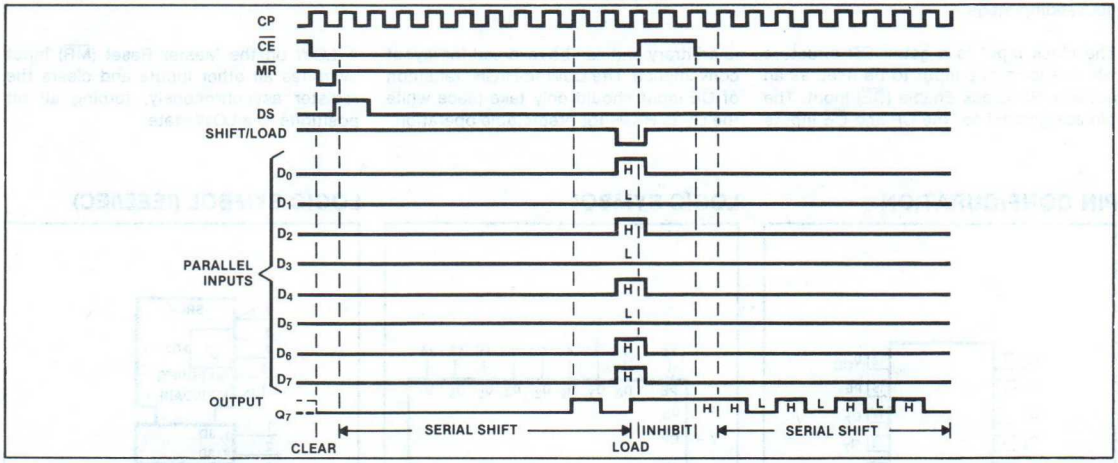


MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS					Q_n REGISTER		OUTPUT
	$\overline{PE}$	$\overline{CE}$	CP	D_S	D_0-D_7	Q_0	Q_1-Q_6	Q_7
Parallel Load	l	l	↑	X	l-l	L	L-L	L
	l	l	↑	X	h-h	H	H-H	H
Serial Shift	h	l	↑	l	X-X	L	q_0-q_5	q_6
	h	l	↑	h	X-X	H	q_0-q_5	q_6
Hold (do nothing)	X	h	X	X	X-X	q_0	q_1-q_6	q_7

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH Clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH Clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH Clock transition.
X = Don't care.
↑ = LOW-to-HIGH Clock transition.

TYPICAL CLEAR, SHIFT, LOAD, INHIBIT, AND SHIFT SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74166			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'L	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	−20		−57	mA
			Com'l	−18		−57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			90	127	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with 4.5V applied to the Serial input, a momentary ground, then 4.5V applied to Clock, all other inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH}	Propagation delay Clock to output	Waveform 1		26	ns
t_{PHL}				30	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		35	ns

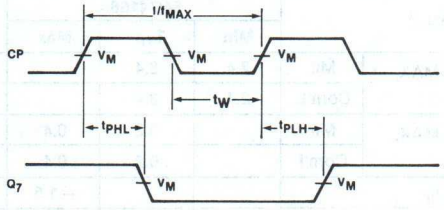
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

	PARAMETER	TEST CONDITIONS	54/74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		ns
t_s	Setup time data to clock	Waveform 3	20		ns
t_h	Hold time data to clock	Waveform 3	0		ns
t_s	Setup time $\overline{CE}$ to clock	Waveform 3	30		ns
t_h	Hold time $\overline{CE}$ to clock	Waveform 3	0		ns
t_s	Setup time $\overline{PE}$ to clock	Waveform 3	30		ns
t_h	Hold time $\overline{PE}$ to clock	Waveform 3	0		ns
t_{rec}	Recovery time $\overline{MR}$ to clock	Waveform 2	30		ns

AC WAVEFORMS

CLOCK TO OUTPUT DELAYS & CLOCK PULSE WIDTH

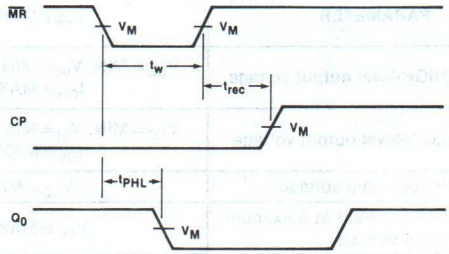


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

The changing output assumes internal Q_6 opposite state from Q_7.

MASTER RESET PULSE WIDTH MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME

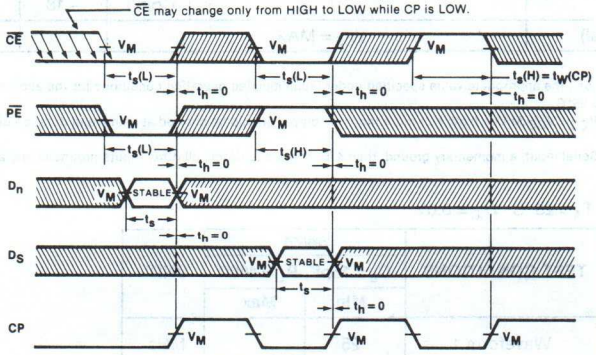


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 1

Waveform 2



CONDITIONS; $\overline{MR}$ = HIGH

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

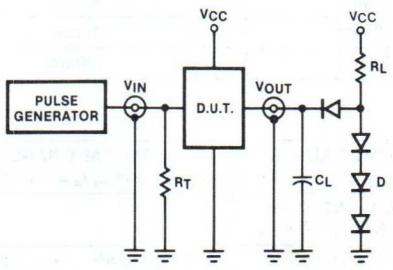
The shaded areas indicate when the input is permitted to change for predictable performance.

The changing output assumes internal Q_6 opposite state from Q_7.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

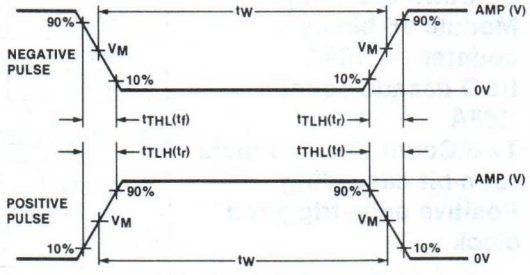
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

COUNTERS 54/74LS168A, 54/74LS169A, S168, S169

4-Bit Up/Down Synchronous Counter

- Synchronous counting and loading
- Up/down counting
- Modulo 16 binary counter — '169A
- BCD decade counter — '168A
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS168A	32MHz	20mA
74S168	70MHz	100mA
74LS169A	32MHz	20mA
74S169	70MHz	100mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS168AN • N74S168N N74LS169AN • N74S169N	
Ceramic DIP	N74LS168AF • N74S168F N74LS169AF • N74S169F	S54LS168AF • S54S168F S54LS169AF • S54S169F
Flatpack		S54LS168AW S54LS169AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
$\overline{PE}$	Input	1Sul	2LSul
$\overline{CET}$	Input	2Sul	1LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

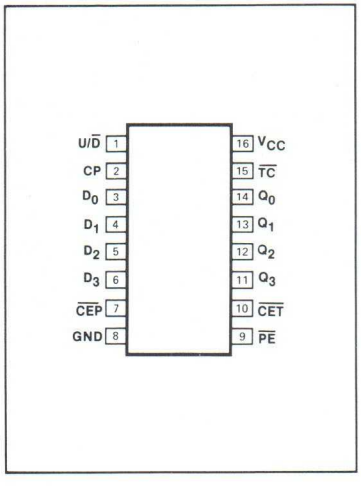
The '168 is a synchronous, presettable BCD decade up/down counter featuring an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n input to be loaded into the counter on the next LOW-to-HIGH transition of the clock.

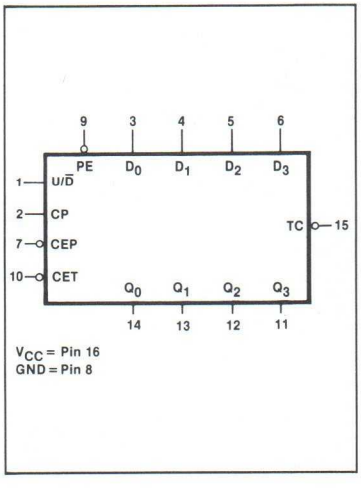
The direction of counting is controlled by the Up/Down ($U/\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. In-

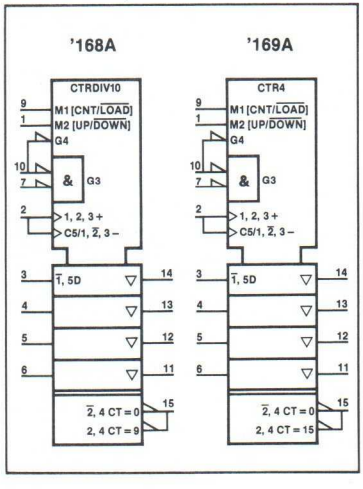
PIN CONFIGURATION



LOGIC SYMBOL



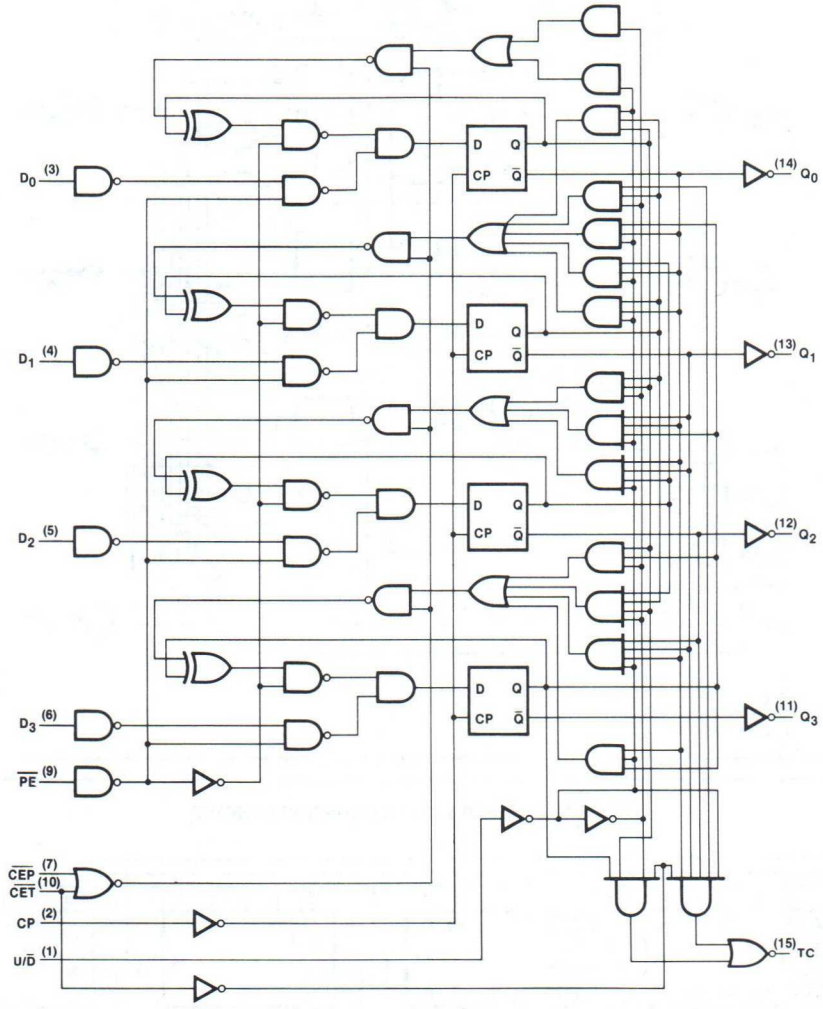
LOGIC SYMBOL (IEEE/IEC)



strumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A for the fast synchronous multistage counting connections.

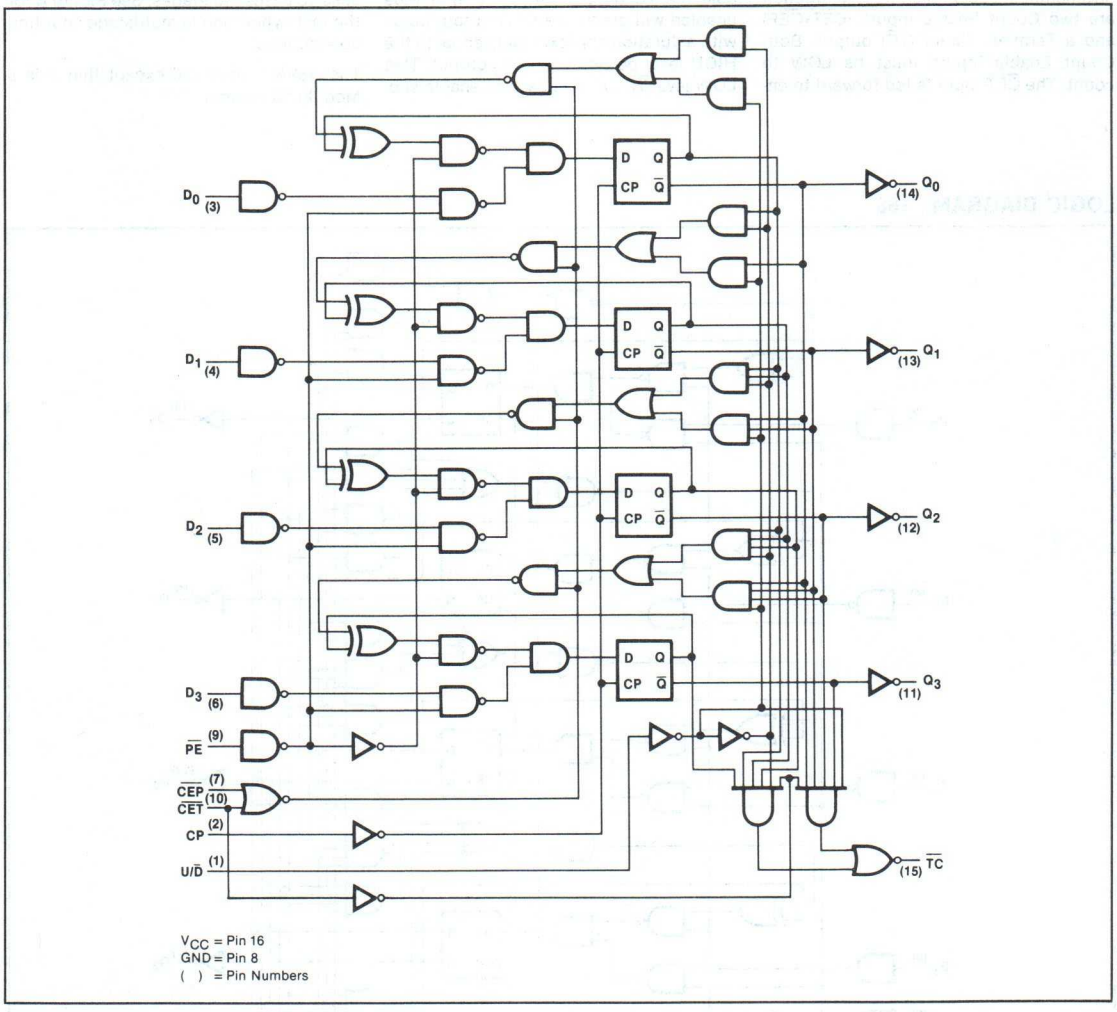
The '169A is identical except that it is a Modulo 16 counter.

LOGIC DIAGRAM, '168



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

LOGIC DIAGRAM, '169



SYNCHRONOUS MULTISTAGE COUNTING SCHEME

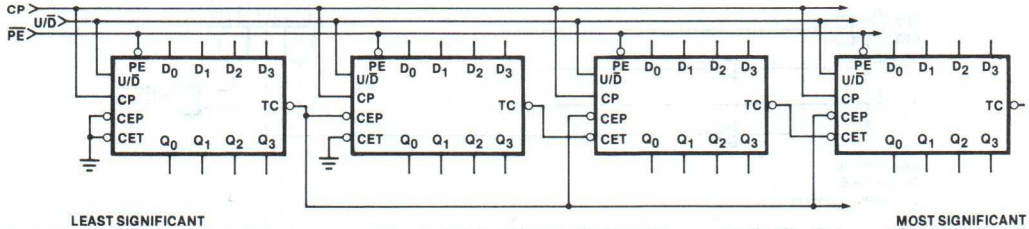


Figure A

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$
Parallel Load	↑	X	X	X	l	l	L	(a)
	↑	X	X	X	l	h	H	(a)
Count Up	↑	h	l	l	h	X	Count Up	(a)
Count Down	↑	l	l	l	h	X	Count Down	(a)
Hold (do nothing)	↑	X	h	X	h	X	q_n	(a)
	↑	X	X	h	h	X	q_n	H

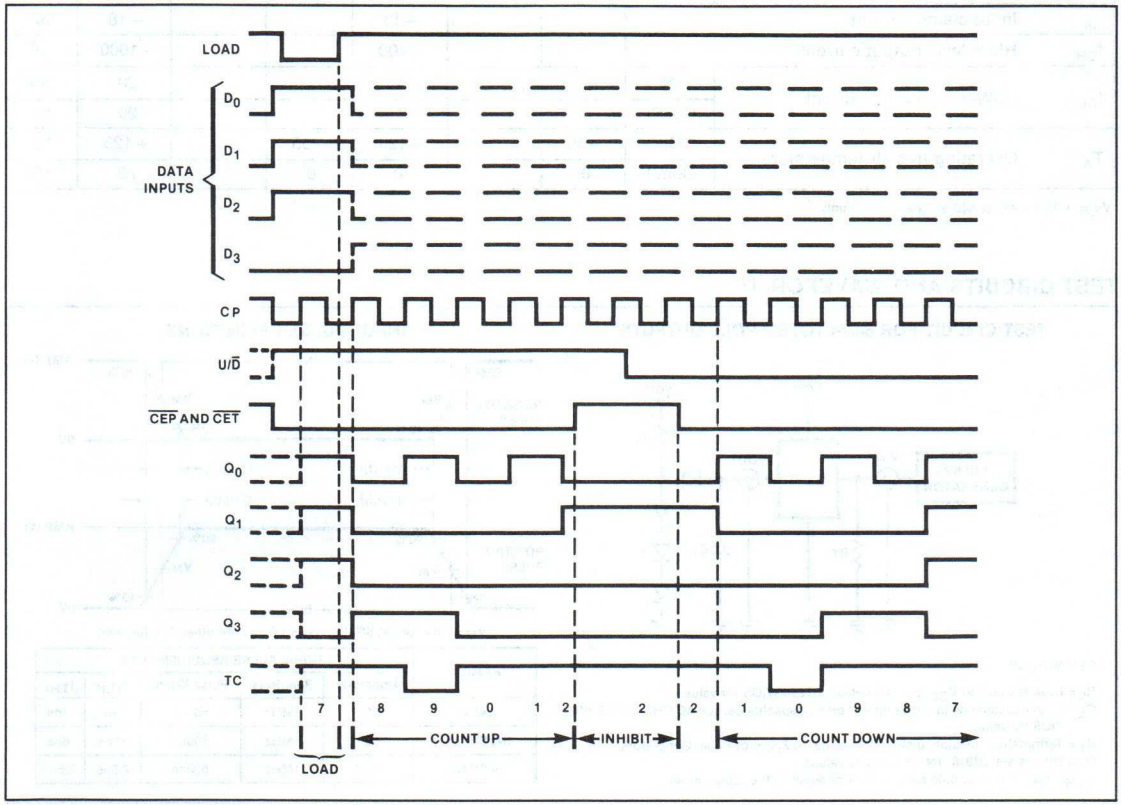
H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level steady state
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
q = Lower case letters indicate the state of the referenced output prior to the LOW-to-HIGH clock transition
↑ = LOW-to-HIGH clock transition

NOTE
a. The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for '169.
The $\overline{TC}$ is LOW when $\overline{CET}$ is LOW and the counter is at Terminal Count. Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for '168.

WAVEFORM (Typical Load, Count, and Inhibit Sequences)

Illustrated below is the following sequence for the '168A. The operation of the '169A is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum), zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine, eight, and seven



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

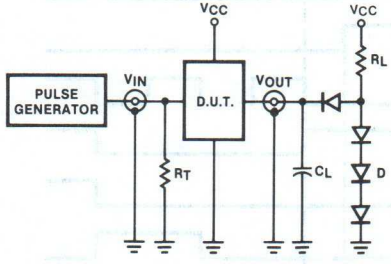
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

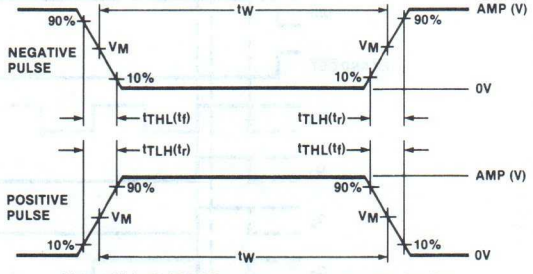
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/74LS168A, 169A			54/74S168, 169			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5	3.4		V
			Com'l	2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
			Com'l		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
		V_I = 7.0V	$\overline{PE}$ input			0.2				mA
			Other inputs			0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	$\overline{PE}$ input			40			-200	μA
			$\overline{CET}$ input			20			100	μA
			Other inputs			20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V	$\overline{PE}$ input			-0.8				mA
			Other inputs			-0.4				mA
		V_I = 0.5V	$\overline{CET}$ input						-4.0	mA
			Other inputs						-2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX			-20		-100	-40		-100	mA
I_{CC} Supply current[4] (total)	V_{CC} = MAX				20	34		100	160	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, then ground to the Clock input with all other inputs grounded and outputs open.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54LS/74LS		54S/74S				UNIT
		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω, U/$\overline{D}$ = HIGH		C_L = 15pF, R_L = 280Ω, U/$\overline{D}$ = LOW		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		40		40		MHz
t_{PLH} Propagation delay	Waveform 1		20		15		15	ns
t_{PHL} Clock to Q output			23		15		15	
t_{PLH} Propagation delay	Waveform 1		35		21		21	ns
t_{PHL} Clock to $\overline{TC}$			35		28		28	
t_{PLH} Propagation delay	Waveform 2		14		11		12	ns
t_{PHL} $\overline{CET}$ to $\overline{TC}$			14		22		25	
t_{PLH} Propagation delay	Waveform 3		25		15		15	ns
t_{PHL} U/$\overline{D}$ control to $\overline{TC}$[(b)]			29		15		22	

NOTE

b. Propagation delay time from up/down to terminal count must be measured with the counter at either a minimum or a maximum count. As the logic level of the Up/Down input is changed, the Terminal Count output will follow. If the count is minimum (0), the Terminal Count output transition will be in phase. If the count is maximum (9 for '168 or 15 for '169), the Terminal Count output will be out of phase.

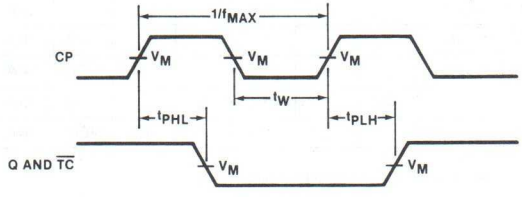
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	25		10		ns
t_s	Setup time, data to clock	Waveform 4	20		4		ns
t_h	Hold time, data to clock	Waveform 4	0		1		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 4	25		6		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 4	0		1		ns
t_s	Setup time, $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 5	20		14		ns
t_h	Hold time, $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 5	0		1		ns
t_s	Setup time, U/$\overline{D}$ to clock	Waveform 6	30		20		ns
t_h	Hold time, U/$\overline{D}$ to clock	Waveform 6	0		1		ns

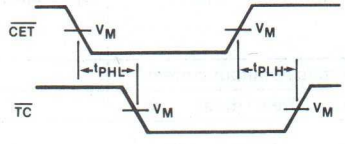
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



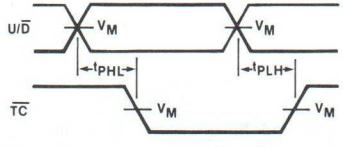
Waveform 1

PROPAGATION DELAYS CET INPUT TO TERMINAL COUNT OUTPUT



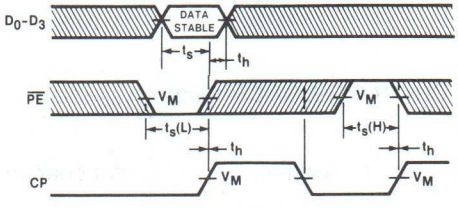
Waveform 2

PROPAGATION DELAYS U/D CONTROL TO TERMINAL COUNT OUTPUT



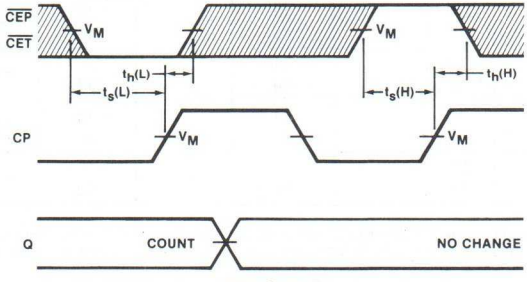
Waveform 3

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES



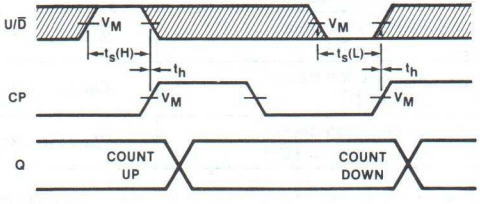
Waveform 4

COUNT ENABLE SETUP AND HOLD TIMES



Waveform 5

UP/DOWN CONTROL SETUP AND HOLD TIMES



Waveform 6

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

REGISTER FILES 54/74170, LS170

4 x 4 Register File (Open Collector)

- **Simultaneous and independent Read and Write operations**
- **Expandable to 1024 words by n-bits**
- **Open Collector outputs for wired-AND expansion**
- **See '670 for 3-State output version**

TYPE	TYPICAL PROPAGATION DELAY (RE to Q)	TYPICAL SUPPLY CURRENT (Total)
74170	10ns (t_{PLH}) 20ns (t_{PHL})	127mA
74LS170	20ns (t_{PLH}) 20ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74170N • N74LS170N	
Ceramic DIP	N74170F • N74LS170F	

3

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
D, W_A, W_B, R_A, R_B	Inputs	1ul	1LSul
$\overline{WE}$, $\overline{RE}$	Inputs	1ul	2LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

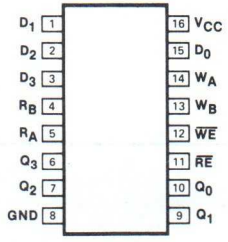
DESCRIPTION

The '170 is a 16-bit register file organized as 4 words of 4 bits each, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

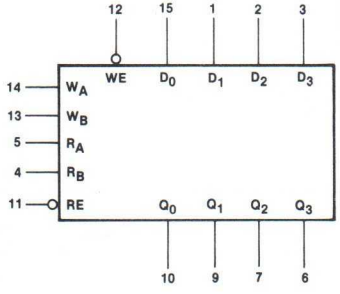
Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is LOW. Data outputs are inhibited and remain HIGH when the Read Enable input is HIGH. This permits simultaneous reading and writing, eliminates recovery times, and is limited in speed only by the read time and the write time.

Up to 256 devices can be stacked to increase the word size to 1024 locations by tying the Open Collector outputs together. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

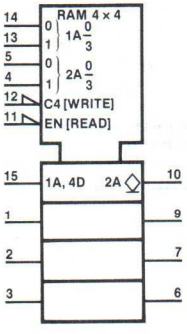
PIN CONFIGURATION



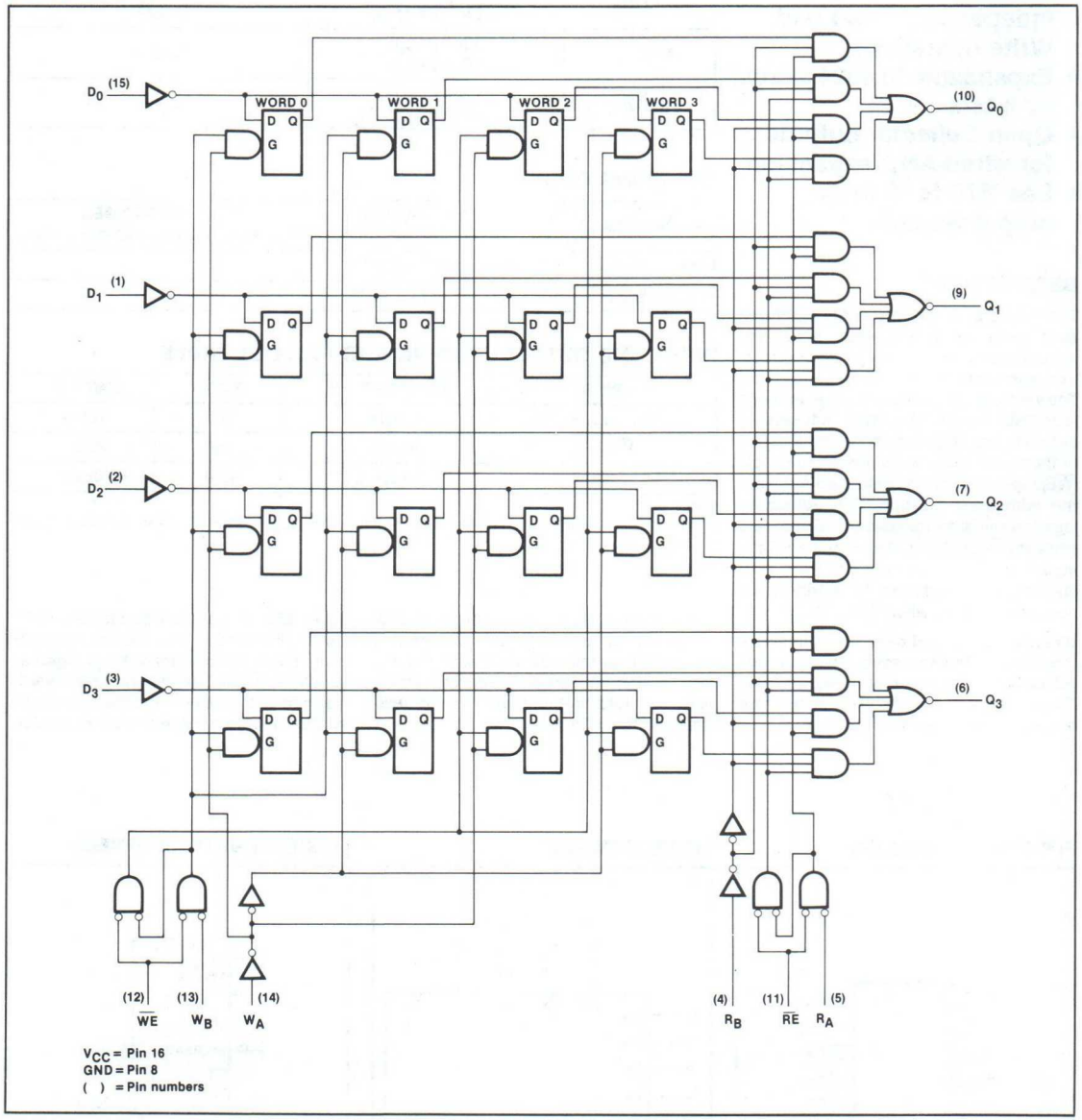
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{WE}$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	INTERNAL LATCHES[b]	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

NOTES
a. The Write Address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.
b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
V_{OH}	HIGH-level output voltage				5.5			5.5	V
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/74170			54/74LS170			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
I_{OH} HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					30			100	μA
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
			Com'l		0.2	0.4		0.35	0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
		V_I = 7.0V	D, W_A, W_B, R_A, R_B inputs						0.1	mA
			$\overline{WE}$, $\overline{RE}$ inputs						0.2	mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
		V_I = 2.7V	D, W_A, W_B, R_A, R_B inputs						20	μA
			$\overline{WE}$, $\overline{RE}$ inputs						40	μA
I_{IL} LOW-level input current	V_{CC} = MAX, V_I = 0.4V		D, W_A, W_B, R_A, R_B inputs			-1.6			-0.4	mA
			$\overline{WE}$, $\overline{RE}$ inputs			-1.6			-0.8	mA
I_{CC} Supply current[3] (total)	V_{CC} = MAX		Mil		127	140		25	40	mA
			Com'l		127	150		25	40	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with 4.5V applied to all Data and both Enable inputs, the Address inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
		Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} Read Enable to output	Waveform 1		15 30		30 30	ns
t_{PLH} Propagation delay t_{PHL} Read Address to output	Waveform 2		35 40		40 40	ns
t_{PLH} Propagation delay t_{PHL} Write Enable to output	Waveform 1		40 45		45 40	ns
t_{PLH} Propagation delay t_{PHL} Data to output	Waveform 1		30 45		45 35	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	Write Enable pulse width	Waveform 3	25		25		ns
t_s	Setup time, Data to positive-going $\overline{WE}$[c]	Waveform 3	10		10		ns
t_h	Hold time, Data to positive-going $\overline{WE}$[c]	Waveform 3	15		15		ns
t_s	Setup time, Read Address to negative-going $\overline{WE}$[c]	Waveform 3	15		15		ns
t_h	Hold time, Read Address to positive-going $\overline{WE}$[c]	Waveform 3	5.0		5.0		ns
t_W	Read Enable pulse width	Waveform 4	25		25		ns
t_{latch}	Latch time for new data[d]	Waveform 5	25		25		ns

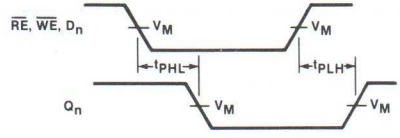
NOTES

c. Write Address setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (Write Address to $\overline{WE}$) can be ignored, as any address selection sustained for the final 30ns of the $\overline{WE}$ pulse and during t_h (Write Address to $\overline{WE}$) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B. $\overline{RE}$ must be LOW.

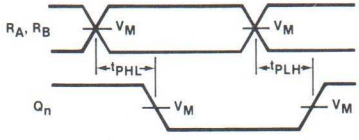
AC WAVEFORMS

PROPAGATION DELAY READ ENABLE, WRITE ENABLE AND DATA TO OUTPUTS



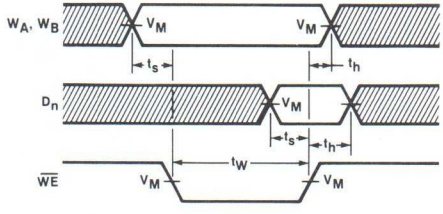
Waveform 1

PROPAGATION DELAY READ ADDRESS TO OUTPUTS



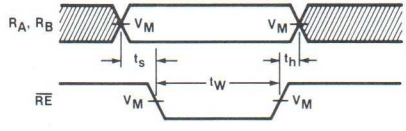
Waveform 2

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



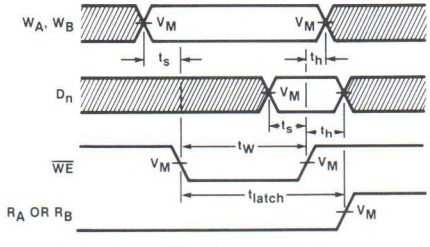
Waveform 3

SETUP AND HOLD TIMES READ ADDRESS TO READ ENABLE



Waveform 4

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



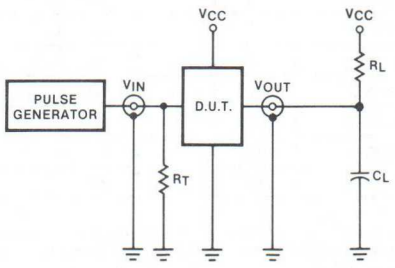
Waveform 5

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

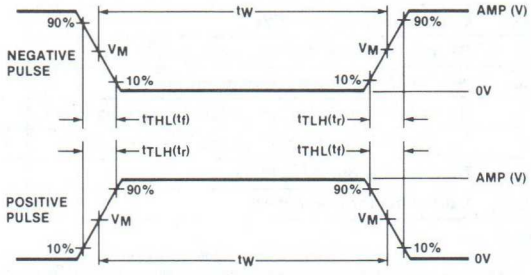
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

REGISTER FILE 74S172

16-Bit Multiple Port Register File (3-State)

- **Simultaneous and independent Read and Write operations**
- **Expandable to 1024 words on n-bits**
- **3-State outputs**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74S172	40MHz	160mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S172N	
Ceramic DIP	N74S172F	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74S
All	Inputs	1Sul
All	Outputs	8Sul

NOTE
A 54/74S unit load (Sul) is 50μA and I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

The '172 is a high-performance, 16-bit multiport register file with 3-State outputs organized as eight words of two bits each. Multiple address decoding circuitry is used so that the read and write operation can be performed independently on up to three word locations. Data can be written into two word locations through input Port "A" or input Port "C" while data is simultaneously read from both output Port "B" and output Port "C".

Port "A" is an input port which can be used to write two bits of data (D_{A0}, D_{A1}) into one of eight register locations selected by the Address inputs (A_{A0}, A_{A1}, A_{A2}). When the Write Enable ($\overline{WE}_A$) input is LOW one setup time prior to the LOW-to-HIGH transition of the Clock (CP) input, the data is written into the selected location.

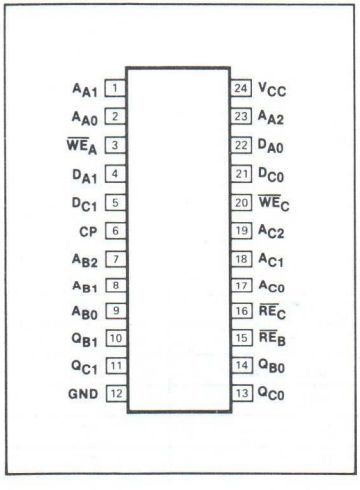
Port "B" is an output port which can be used to read two bits of data from one of eight register locations selected by the Address inputs (A_{B0}, A_{B1}, A_{B2}). When the Read Enable ($\overline{RE}_B$) is LOW, the selected 2-bit word appears on outputs Q_{B0} and Q_{B1}. When $\overline{RE}_B$ is HIGH, the Q_{B0} and Q_{B1} outputs are in the HIGH impedance "off" state. The read operation is independent of the clock.

Port "C" is a read/write port that has separate Data input and Data output sections, but common Address inputs (A_{C0}, A_{C1}, A_{C2}). Data can be simultaneously written into and read from the same register location. Port "C" can be used to write data into one location while Port "A" is writing into a different location, but data cannot be written reliably into the same location simultaneously.

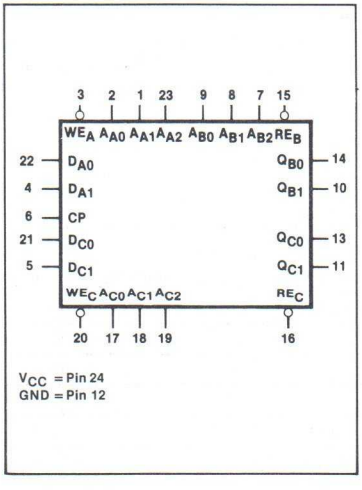
If both Ports "A" and "C" are enabled for writing into the same location during the same clock cycle, the LOW data will predominate if there is a conflict.

The register operation is essentially a master-slave flip-flop. Each master acts as a transparent D latch when selected by the "A" or "C" address and the clock and applicable write enable are LOW. The data in the master is transferred to the slave (or output section) following the LOW-to-HIGH transition of the Clock (CP). The Address inputs must be stable while the

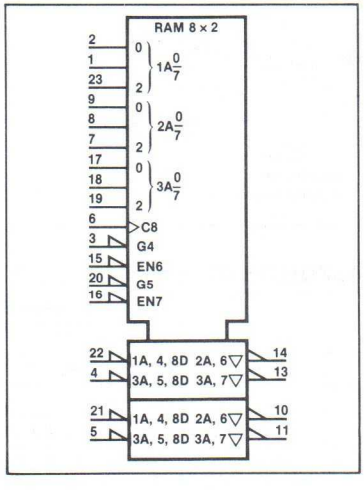
PIN CONFIGURATION



LOGIC SYMBOL



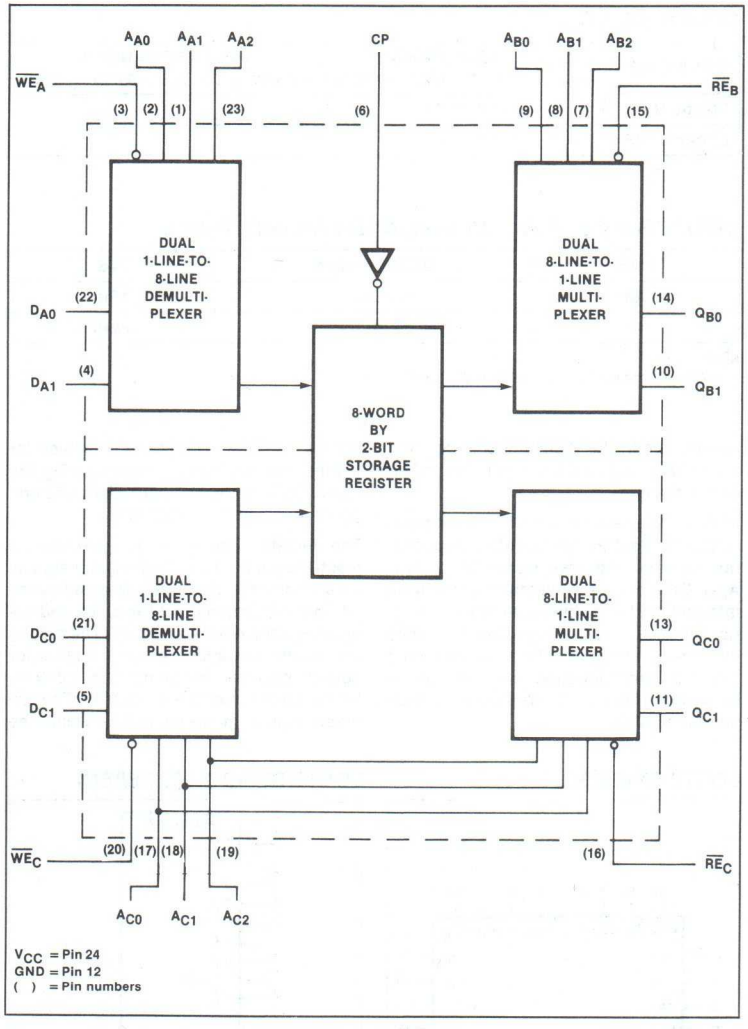
LOGIC SYMBOL (IEEE/IEC)



REGISTER FILE 74S172

Clock and Write Enable inputs are LOW to ensure retention of data previously written into the other locations. Any number of masters can be altered while the clock and write enable are LOW, but the new data will not be loaded into the slaves, or be available at the outputs, until the clock goes HIGH.

BLOCK DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS			ADDRESSED REGISTER
	CP	$\overline{WE}$	D_n	
Write Data[a]	↑	l	l	L
	↑	l	h	H
Hold[b]	↓	h	X	no change

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUTS
	$\overline{RE}$	ADDRESSED REGISTER	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH or HIGH-to-LOW clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = HIGH impedance (off) state.
↑ = LOW-to-HIGH clock transition.
↓ = HIGH-to-LOW clock transition.

NOTES
a. The Write Address (A_A and A_C) to the "internal register" must be stable while $\overline{WE}$ and CP are LOW for conventional operation.
b. The Write Enable must be HIGH before the HIGH-to-LOW clock transition to ensure that the data in the register is not changed.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74S	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−5.2	mA
I_{OL}	LOW-level output current	Com'l			20	mA
T_A	Operating free-air temperature	Com'l	0		70	°C

3

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		74S172			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX				0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V				40	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V				−40	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	CP, $\overline{WE}_A$, $\overline{WE}_C$, A_{C0}-A_{C2}			−1.6	mA
			Other inputs			−0.8	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			160	190	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs at 4.5V and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	74S		UNIT
			C_L = 50pF, R_L = 400Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Address (B or C) to output	Waveform 2		30 30	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		38 38	ns
t_{PZH}	Read enable time to HIGH	Waveform 3		30	ns
t_{PZL}	Read enable time to LOW	Waveform 4		30	ns
t_{PHZ}	Disable time from HIGH	Waveform 3, C_L = 5pF		20	ns
t_{PLZ}	Disable time from LOW	Waveform 4, C_L = 5pF		20	ns

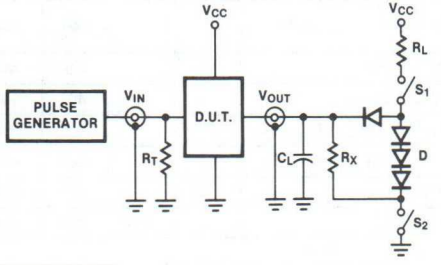
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	74S		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	25		ns
t_s	Setup time, Write Address (A or C) to negative-going Clock and $\overline{WE}$	Waveform 5	15		ns
t_h	Hold time, Write Address (A or C) to positive-going Clock and $\overline{WE}$	Waveform 5	0		ns
$t_s(H)$	Setup time, HIGH Data to Clock	Waveform 5	30		ns
$t_h(H)$	Hold time, HIGH Data to Clock	Waveform 5	0		ns
$t_s(L)$	Setup time, LOW Data to Clock	Waveform 5	20		ns
$t_h(L)$	Hold time, LOW Data to Clock	Waveform 5	0		ns
t_s	Setup time, LOW $\overline{WE}$ to positive-going Clock	Waveform 6	35		ns
t_h	Hold time, LOW $\overline{WE}$ to positive-going Clock	Waveform 6	0		ns
t_s	Setup time, HIGH $\overline{WE}$ to negative-going Clock	Waveform 6	10		ns
t_h	Hold time, HIGH $\overline{WE}$ to positive-going Clock	Waveform 6	0		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



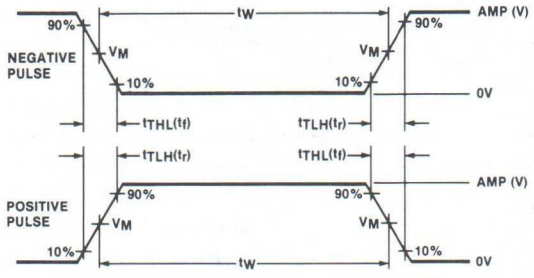
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

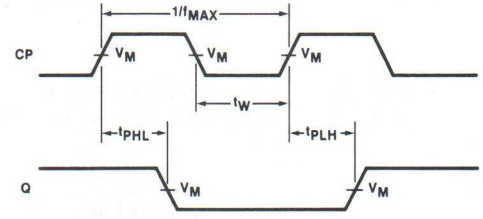


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

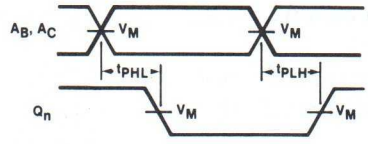
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



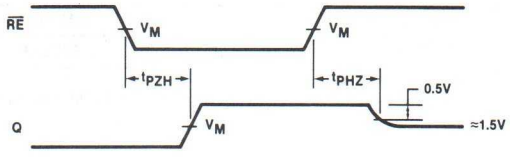
Waveform 1

PROPAGATION DELAY READ ADDRESS TO OUTPUTS



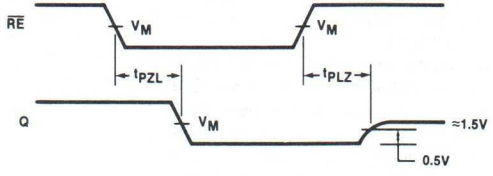
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



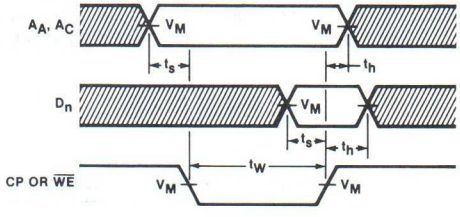
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



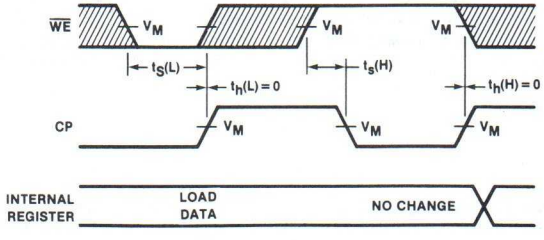
Waveform 4

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



Waveform 5

WRITE ENABLE SETUP AND HOLD TIMES



Waveform 6

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Quad D-Type Flip-Flop With 3-State Outputs

- **Edge-triggered D-type register**
- **Gated input enable for hold "do nothing" mode**
- **3-State output buffers**
- **Gated output enable control**
- **Pin compatible with the 8T10 and DM8551**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74173	35MHz	50mA
74LS173	50MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74173N • N74LS173N	
Ceramic DIP	N74173F • N74LS173F	S54LS173F
Flatpack		S54LS173W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

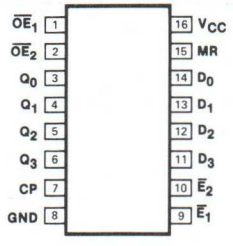
DESCRIPTION

The '173 is a 4-bit parallel load register with clock enable control, 3-State buffered outputs and master reset. When the two Clock Enable ($\overline{E}_1$ and $\overline{E}_2$) inputs are LOW, the data on the D inputs is loaded into the register synchronously with the LOW-to-HIGH Clock (CP) transition. When one or both $\overline{E}$ inputs are HIGH one setup time before the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and Clock Enable inputs are fully edge triggered and must be stable only one setup time before the LOW-to-HIGH clock transition.

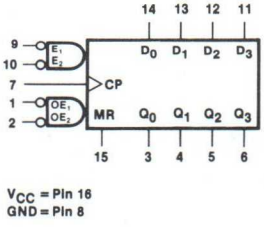
The Master Reset (MR) is an active HIGH asynchronous input. When the MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-State output buffers are controlled by a 2-input NOR gate. When both Output Enable ($\overline{OE}_1$ and $\overline{OE}_2$) inputs are LOW, the data in the register is presented at the Q outputs. When one or both $\overline{OE}$ inputs is HIGH, the outputs are forced to a HIGH impedance "off" state. The 3-State output buffers are completely independent of the register operation; the $\overline{OE}$ transition does not affect the clock and reset operations.

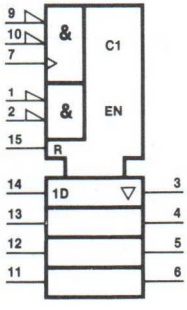
PIN CONFIGURATION



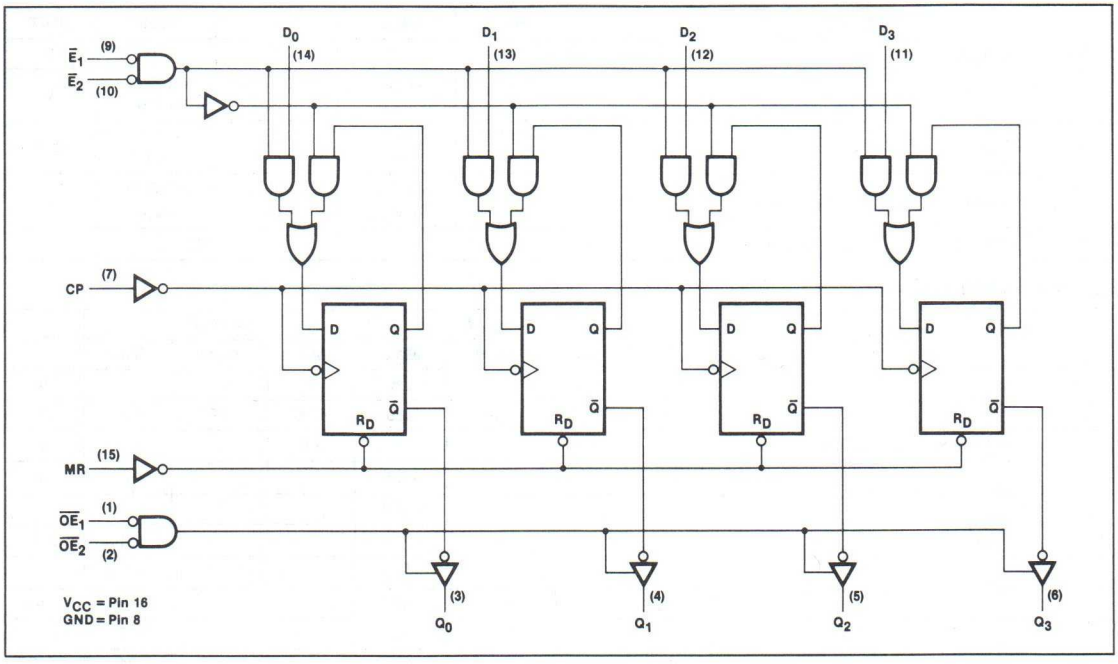
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\overline{E}_1$	$\overline{E}_2$	D_n	Q_n (Register)
Reset (clear)	H	X	X	X	X	L
Parallel load	L	↑	l	l	l	L
	L	↑	l	l	h	H
Hold (no change)	L	X	h	X	X	q_n
	L	X	X	h	X	q_n

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS
	Q_n (Register)	$\overline{OE}_1$	$\overline{OE}_2$	Q_0, Q_1, Q_2, Q_3
Read	L	L	L	L
	H	L	L	H
Disabled	X	H	X	(Z)
	X	X	H	(Z)

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
q_n = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
(Z) = HIGH impedance "off" state.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

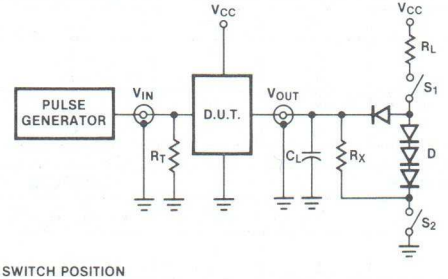
PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0			−1.0	mA
		Com'l			−5.2			−2.6	mA
I_{OL}	LOW-level output current	Mil			16			12	mA
		Com'l			16			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



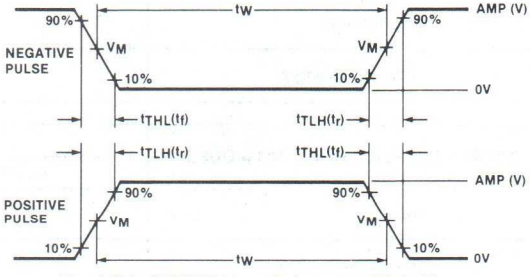
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load, capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74173			54/74LS173			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4			2.4	3.4		V
				Com'l	2.4			2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN		V_O = 2.4V			40				μA
				V_O = 2.7V						20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					-40			-20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX		V_I = 5.5V			1.0				mA
				V_I = 7.0V						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX		V_I = 2.4V			40				μA
				V_I = 2.7V						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-30		-70	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				50	72		20	30	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V, and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with MR grounded following momentary connection to 4.5V, $\overline{OE}_2$, $\overline{E}_1$, $\overline{E}_2$ and all Data inputs grounded, CP and $\overline{OE}_1$ at 4.5V, and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 50pF, R_L = 400Ω		54LS/74LS C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		43 31		25 30	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		27		35	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		30		23	ns
t_{PZL}	Output enable to LOW level	Waveform 3		30		27	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		14		17	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		20		17	ns

NOTE

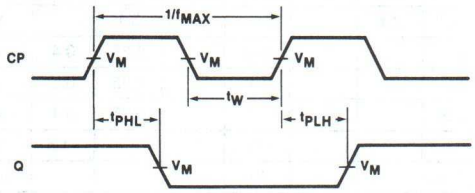
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W(CP)	Clock pulse width	Waveform 1	20		20		ns
t_W(MR)	MR pulse width	Waveform 4	20		20		ns
t_s(D)	Setup time, Data to Clock	Waveform 5	10		17		ns
t_h(D)	Hold time, Data to Clock	Waveform 5	10		0		ns
$t_s(\overline{E})$	Setup time, Enable to Clock	Waveform 5	17		35		ns
$t_h(\overline{E})$	Hold time, Enable to Clock	Waveform 5	2		0		ns
t_{rec}(MR)	Recovery time, Master Reset to Clock	Waveform 4	10		17		ns

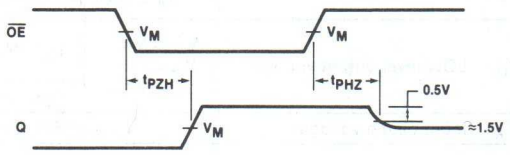
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



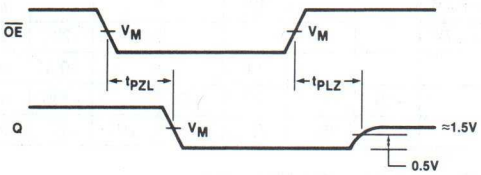
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



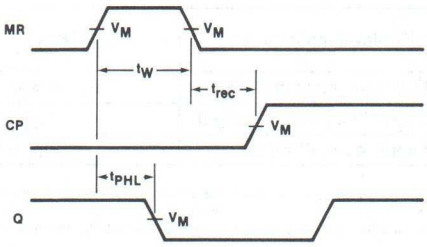
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



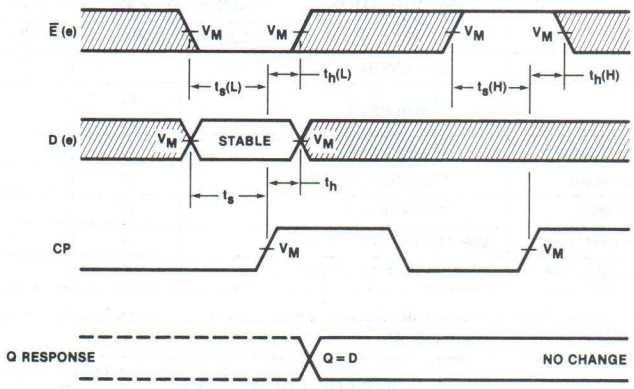
Waveform 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 4

SETUP (t_s) AND HOLD (t_h) TIMES FOR DATA (D) AND ENABLE (E) INPUTS



Waveform 5

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Hex D Flip-Flops

- **Six edge-triggered D-type flip-flops**
- **Three speed-power ranges available**
- **Buffered common clock**
- **Buffered, asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74174	35MHz	45mA
74LS174	40MHz	16mA
74S174	110MHz	90mA

DESCRIPTION

The '174 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING CODE

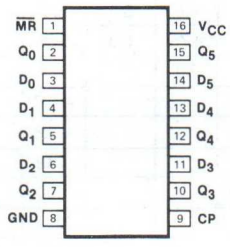
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74174N • N74LS174N N74S174N	
Ceramic DIP	N74174F • N74LS174F N74S174F	S54174F • S54LS174F S54S174F
Flatpack		S54174W • S54LS174W S54S174W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

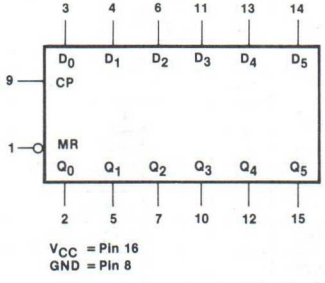
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
Q_0-Q_5	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

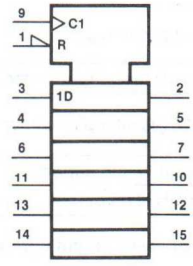
PIN CONFIGURATION



LOGIC SYMBOL

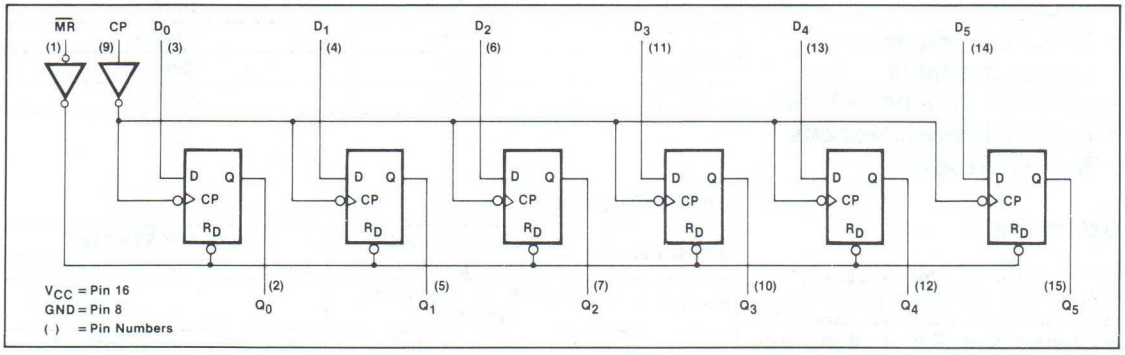


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOPS 54/74174, LS174, S174

LOGIC DIAGRAM



FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS[1]			54/74174			54/74LS174			54/74S174			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH} HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
			Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
			Com'l		0.2	0.4		0.35	0.5			0.5	V
		I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK} Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
		V_I = 7.0V							0.1				mA
I_{IH} HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
		V_I = 2.7V							20			50	μA
I_{IL} LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
		V_I = 0.5V										– 2.0	mA
I_{OS} Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	– 40		– 100	mA
			Com'l	– 18		– 57	– 20		– 100	– 40		– 100	mA
I_{CC} Supply current[4] (total)	V_{CC} = MAX				45	65		16	26		90	144	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after a momentary ground, then 4.5V is applied to Clock, with 4.5V applied to all Data and $\overline{MR}$ inputs and all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t_{PLH} Propagation delay	Waveform 1		30		30		13	ns
t_{PHL} Clock to output			35		30		17	
t_{PHL} Propagation delay $\overline{MR}$ to output	Waveform 3		35		35		22	ns

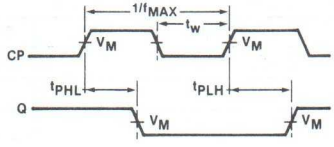
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
		Min	Max	Min	Max	Min	Max	
t_W(L) Clock pulse width (LOW)	Waveform 1	20		20		7.0		ns
t_W Master Reset pulse width	Waveform 3	20		20		10		ns
t_s Setup time, data to CP	Waveform 2	20		20		5.0		ns
t_h Hold time, data to CP	Waveform 2	5		5		3.0		ns
t_{rec} Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		5.0		ns

AC WAVEFORMS

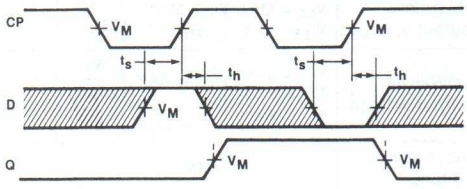
CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 1

DATA SET-UP AND HOLD TIMES

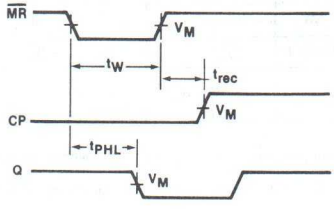


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance

Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

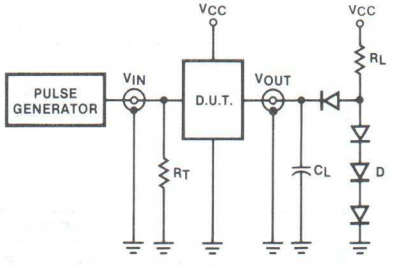


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

Waveform 3

TEST CIRCUITS AND WAVEFORMS

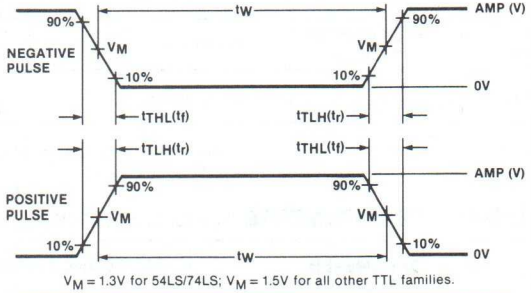
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Quad D Flip-Flop

- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74175	35MHz	30mA
74LS175	40MHz	11mA
74S175	110MHz	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74175N • N74LS175N N74S175N	
Ceramic DIP	N74175F • N74LS175F N74S175F	S54175F • S54LS175F
Flatpack		S54175W • S54LS175W

DESCRIPTION

The '175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and $\overline{Q}$ outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

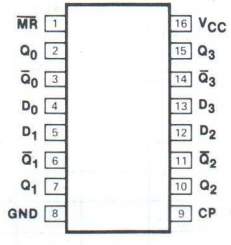
All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

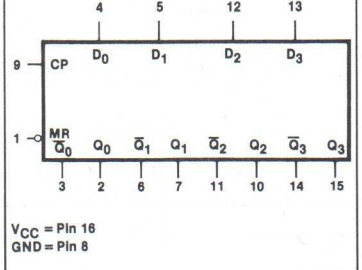
PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

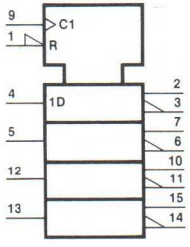
PIN CONFIGURATION



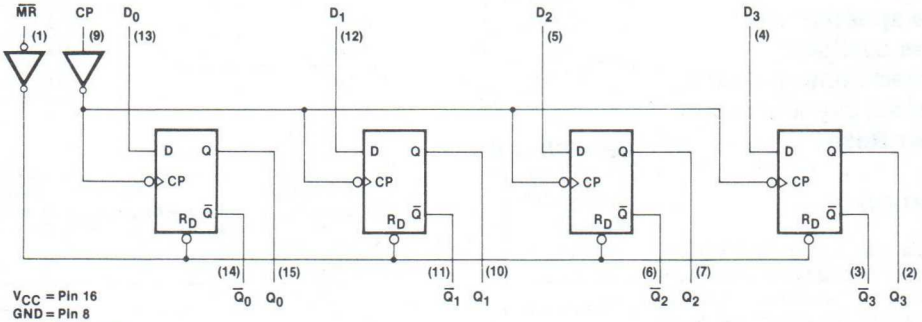
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74175			54/74LS175			54/74S175			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				30	45		11	18		60	96	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open and 4.5V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		30		75		MHz
t_{PLH}	Propagation delay Clock to outputs	Waveform 1		30		25		12	ns
t_{PHL}				35		25		17	
t_{PLH}	Propagation delay $\overline{MR}$ to outputs	Waveform 3		25		30		15	ns
t_{PHL}				35		30		22	

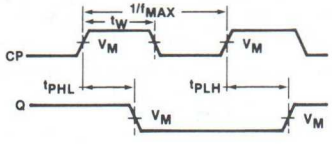
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_f, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		7		ns
t_W	Master Reset pulse width	Waveform 3	20		20		10		ns
t_s(H)	Setup time, HIGH data to CP	Waveform 2	20		20		5		ns
t_h(H)	Hold time, HIGH data to CP	Waveform 2	5		5		3		ns
t_s(L)	Setup time, LOW data to CP	Waveform 2	20		20		5		ns
t_h(L)	Hold time, LOW data to CP	Waveform 2	5		5		3		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 3	25		25		5		ns

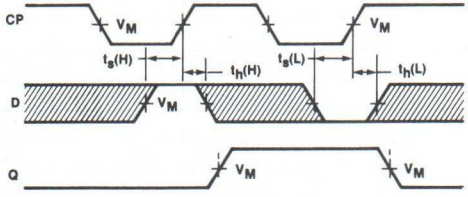
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



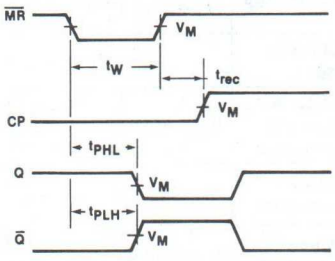
Waveform 1

DATA SET-UP AND HOLD TIMES



Waveform 2

MASTER RESET TO OUTPUT DELAY, MASTER RESET PULSE WIDTH, AND MASTER RESET RECOVERY TIME

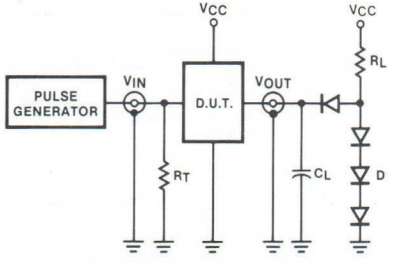


Waveform 3

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

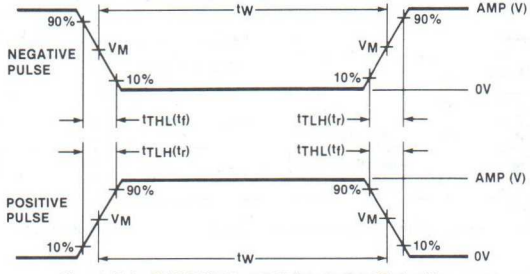
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

PARITY GENERATOR/CHECKER 54/74180

9-Bit Odd/Even Parity Generator/Checker

- **Word length easily expanded by cascading**
- **Generate even or odd parity**
- **Checks for parity errors**
- **See '280 for faster parity checker**

TYPE	TYPICAL PROPAGATION DELAY, $P_O = 0V$	TYPICAL SUPPLY CURRENT
74180	36ns	34mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%; T_A = 0°C$ to $+70°C$	MILITARY RANGES $V_{CC} = 5V \pm 10\%; T_A = -55°C$ to $+125°C$
Plastic DIP	N74180N	
Ceramic DIP	N74180F	S54180F
Flatpack		S54180W

3

DESCRIPTION

The '180 is a 9-bit parity generator or checker commonly used to detect errors in high speed data transmission or data retrieval systems. Both Even and Odd parity enable inputs and parity outputs are available for generating or checking parity on 8-bits.

True active-HIGH or true active-LOW parity can be generated at both the Even and Odd outputs. True active-HIGH parity is established with Even Parity enable input (P_E) set HIGH and the Odd Parity enable input (P_O) set LOW. True active-LOW parity is established when P_E is LOW and P_O is HIGH. When both enable inputs are at the same logic level, both outputs will be forced to the opposite logic level.

Parity checking of a 9-bit word (8 bits plus parity) is possible by using the two enable inputs plus an inverter as the ninth data input. To check for true active-HIGH parity, the ninth data input is tied to the P_O input and an inverter is connected between the P_O and P_E inputs. To check for true active-LOW parity, the ninth data input is tied to the P_E input and an inverter is connected between the P_E and P_O inputs.

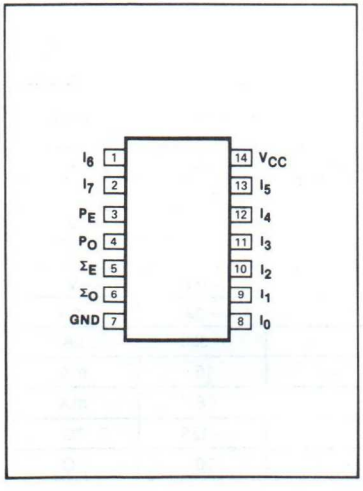
Expansion to larger word sizes is accomplished by serially cascading the '180 in 8-bit increments. The Even and Odd parity outputs of the first stage are connected to the corresponding P_E and P_O inputs, respectively, of the succeeding stage.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

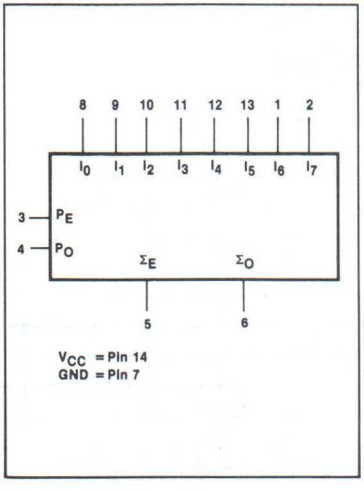
PINS	DESCRIPTION	54/74
I_0-I_7	Data inputs	1ul
P_E, P_O	Parity inputs	2ul
Σ_E, Σ_O	Parity outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

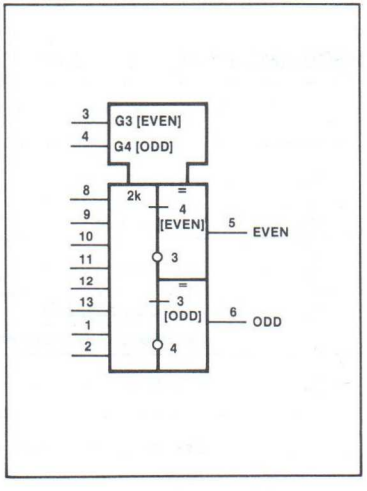
PIN CONFIGURATION



LOGIC SYMBOL

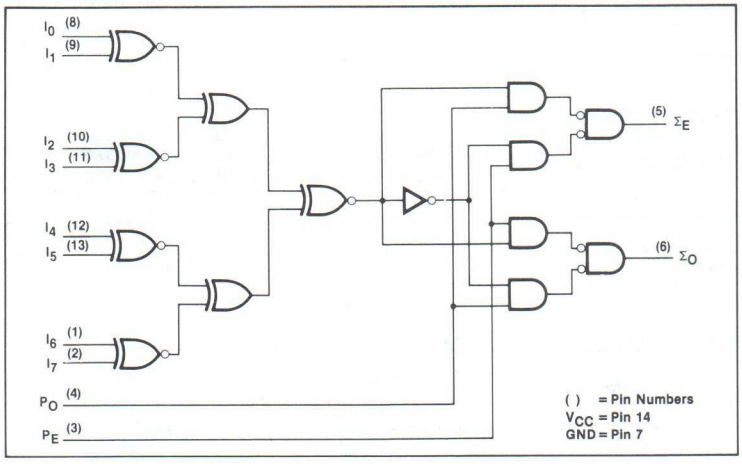


LOGIC SYMBOL (IEEE/IEC)



PARITY GENERATOR/CHECKER 54/74180

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	
Number of HIGH Data Inputs (I_0-I_7)	P_E	P_O	Σ_E	Σ_O
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5V to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

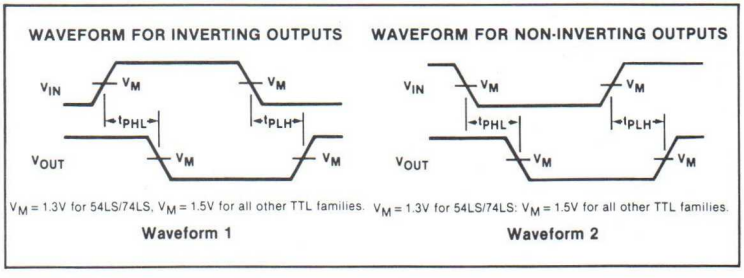
PARITY GENERATOR/CHECKER 54/74180

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74180 Min	54/74180 Typ[2]	54/74180 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.3		V
			Com'l	2.4	3.3		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	I_0-I_7 inputs			40	μA
			P_E, P_O inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	I_0-I_7 inputs			−1.6	mA
			P_{0E}, P_O inputs			−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	−20		−55	mA
			Com'l	−18		−55	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Mil		34	49	mA
			Com'l		34	56	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with P_E and P_O inputs at 4.5V, all other inputs and outputs open.

AC WAVEFORMS

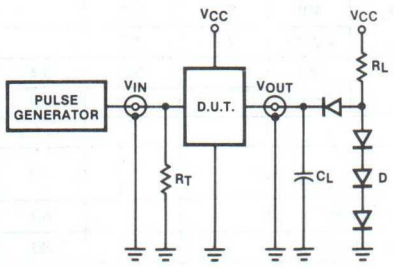


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Data to Even output	Waveforms 1 & 2, P_O = 0V		60 68	ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output	Waveforms 1 & 2, P_O = 0V		48 38	ns
t_{PLH} t_{PHL}	Propagation delay Data to Even output	Waveforms 1 & 2, P_E = 0V		48 38	ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output	Waveforms 1 & 2, P_E = 0V		60 68	ns
t_{PLH} t_{PHL}	Propagation delay P_E or P_O to output	Waveform 1		20 10	ns

TEST CIRCUITS AND WAVEFORMS

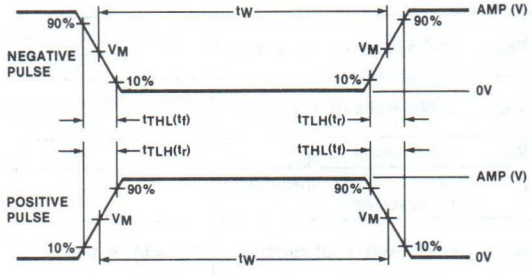
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

ARITHMETIC LOGIC UNITS

54/74181, LS181, S181

4-Bit Arithmetic Logic Unit

- **Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations**
- **Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations**
- **Full lookahead carry for high-speed arithmetic operation on long words**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74181	22ns	91mA
74LS181	22ns	21mA
74S181	11ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74181N • N74LS181N N74S181N	
Ceramic DIP	N74181F • N74LS181F N74S181F	S54181F • S54LS181F S54S181F
Flatpack		S54LS181W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
Mode	Input	1ul	1Sul	1LSul
$\overline{A}$ or $\overline{B}$	Inputs	3ul	3Sul	3LSul
S	Inputs	4ul	4Sul	4LSul
Carry	Input	5ul	5Sul	5LSul
F_0-F_3, A = B, C_{n+4}	Outputs	10ul	10Sul	10LSul
$\overline{G}$	Output	10ul	10Sul	40LSul
$\overline{P}$	Output	10ul	10Sul	20LSul

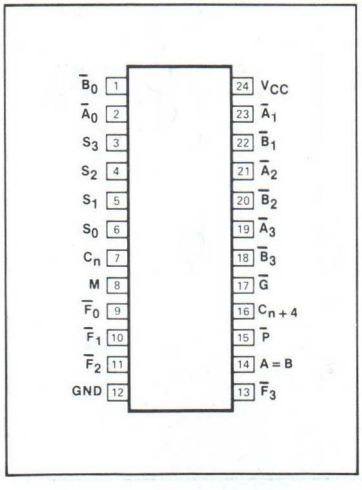
NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

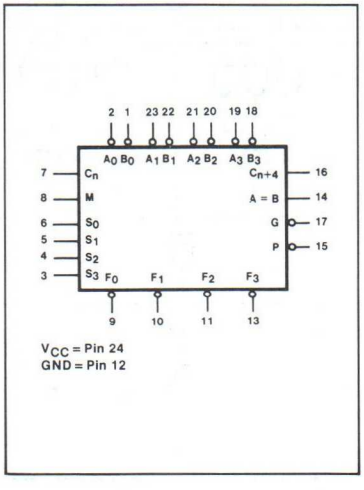
The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S_0-S_3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals $\overline{P}$ (Carry Propagate) and $\overline{G}$ (Carry Generate). $\overline{P}$ and $\overline{G}$ are not affected by carry in. When speed require-

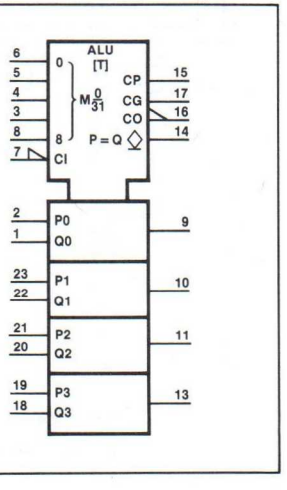
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



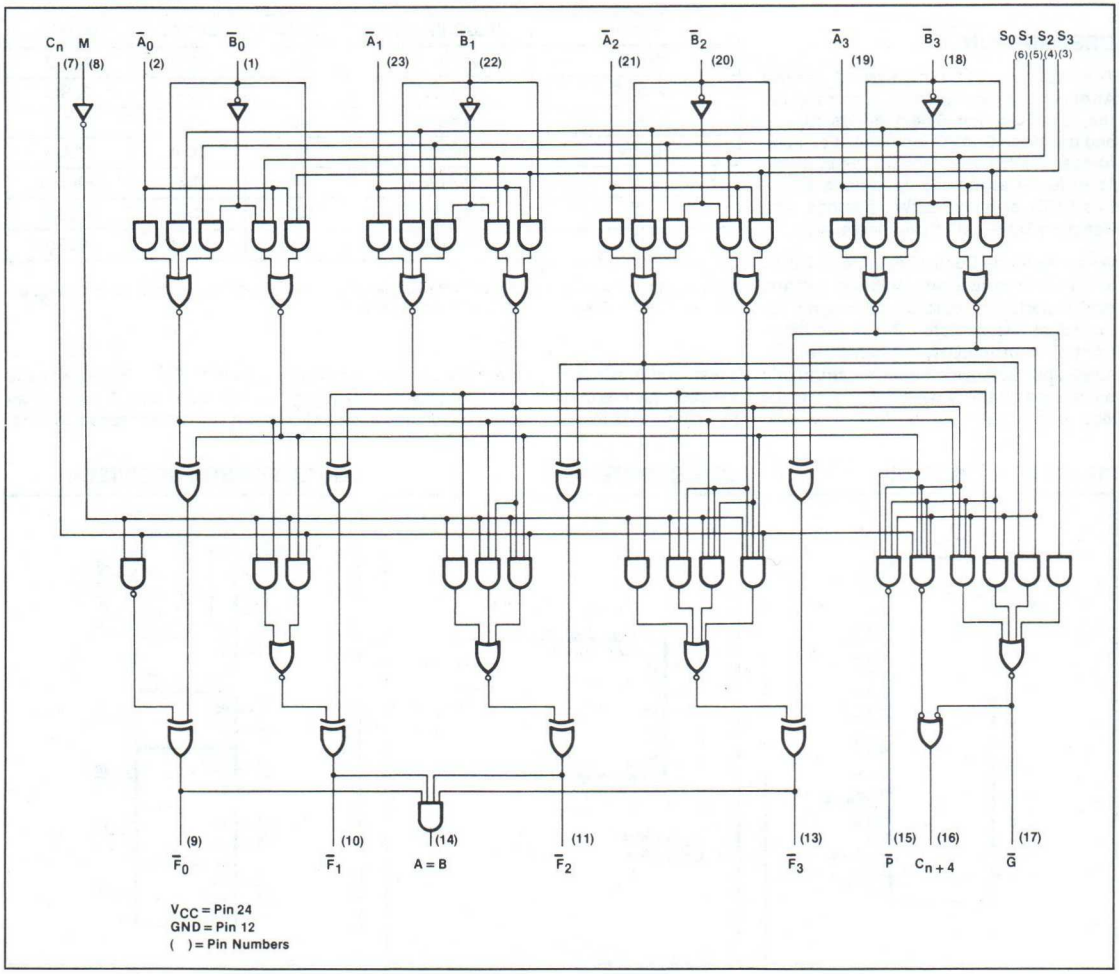
ments are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the '182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The A = B output from the device goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more than 4 bits. The A = B signal can also be used with the C_{n+4} signal to indicate A > B and A < B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM

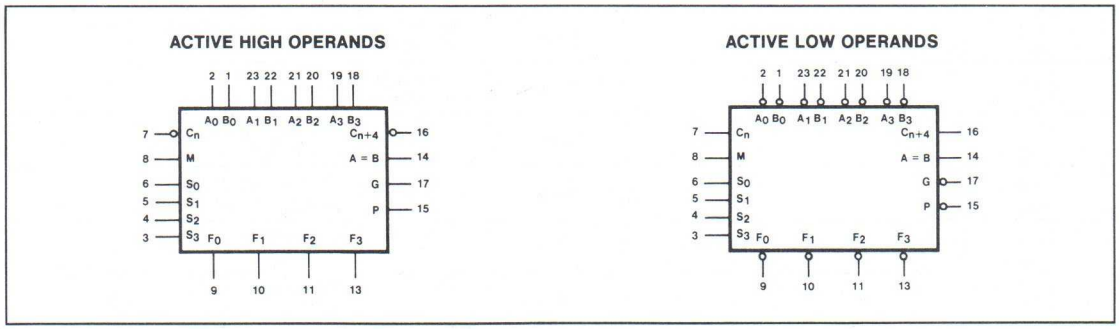


MODE SELECT—FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A
L	L	L	H	$\overline{A+B}$	A + B
L	L	H	L	$A\overline{B}$	A + $\overline{B}$
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\overline{AB}$	A plus A$\overline{B}$
L	H	L	H	$\overline{B}$	(A + B) plus A$\overline{B}$
L	H	H	L	$A \oplus B$	A minus B minus 1
L	H	H	H	$A\overline{B}$	AB minus 1
H	L	L	L	$\overline{A}+B$	A plus AB
H	L	L	H	$\overline{A \oplus B}$	A plus B
H	L	H	L	B	(A + $\overline{B}$) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	A + $\overline{B}$	(A + B) plus A
H	H	H	L	A + B	(A + $\overline{B}$) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S_3	S_2	S_1	S_0	LOGIC (M = H)	ARITHMETIC** (M = L) (C_n = L)
L	L	L	L	$\overline{A}$	A minus 1
L	L	L	H	$\overline{AB}$	AB minus 1
L	L	H	L	$\overline{A}$ + B	A$\overline{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\overline{A+B}$	A plus (A + $\overline{B}$)
L	H	L	H	$\overline{B}$	AB plus (A + $\overline{B}$)
L	H	H	L	$\overline{A \oplus B}$	A minus B minus 1
L	H	H	H	A + $\overline{B}$	A + $\overline{B}$
H	L	L	L	$\overline{A}B$	A plus (A + B)
H	L	L	H	$A \oplus B$	A plus B
H	L	H	L	B	A$\overline{B}$ plus (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	A$\overline{B}$	AB plus A
H	H	H	L	AB	A$\overline{B}$ plus A
H	H	H	H	A	A

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7			+ 0.8	V
		Com'l			+ 0.8			+ 0.8			+ 0.8	V
I_{IK}	Input clamp current				− 12			− 18			− 18	mA
I_{OH}	HIGH-level output current				− 800			− 400			− 1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	− 55		+ 125	− 55		+ 125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = + 0.7V MAX for 54S at T_A = + 125°C only.

SUM MODE TEST TABLE I

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$	C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	Remaining $\overline{B}$	Remaining $\overline{A}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$	All $\overline{B}$	Any $\overline{F}$ or C_{n+4}

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND	
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$\overline{F}_i$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{P}$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{G}$
t_{PLH} t_{PHL}	$\overline{A}_i$	None	$\overline{B}_i$	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	Remaining $\overline{A}$	Remaining $\overline{B}$, C_n	$A = B$
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	$\overline{B}_i$	None	$\overline{A}_i$	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	C_{n+4}
t_{PLH} t_{PHL}	C_n	None	None	All $\overline{A}$ and $\overline{B}$	None	Any $\overline{F}$ or C_{n+4}

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		APPLY 4.5V	APPLY GND	APPLY 4.5V	APPLY GND		
t_{PLH} t_{PHL}	$\overline{A}_i$	$\overline{B}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	$\overline{B}_i$	$\overline{A}_i$	None	None	Remaining $\overline{A}$ and $\overline{B}$, C_n	$\overline{F}_i$	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74181			54/74LS181			54/74S181			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Any output except A = B	Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX All outputs	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
			I_{OL} = 16mA $\overline{G}$ output	Mil					0.47	0.7				V
				Com'l					0.47	0.7				V
			I_{OL} = 8mA $\overline{P}$ output	Mil					0.35	0.6				V
				Com'l					0.35	0.5				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V	Mode input				1.0			0.1			1.0	mA
			$\overline{A}$ or $\overline{B}$ inputs				1.0			0.3			1.0	mA
			S inputs				1.0			0.4			1.0	mA
			Carry input				1.0			0.5			1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	Mode input			40							μA
				$\overline{A}$ or $\overline{B}$ inputs			120							μA
				S inputs			160							μA
				Carry input			200							μA
			V_I = 2.7V	Mode input						20			50	μA
				$\overline{A}$ or $\overline{B}$ inputs						60			150	μA
				S inputs						80			200	μA
				Carry input						100			250	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	Mode input			– 1.6			– 0.4				mA
				$\overline{A}$ or $\overline{B}$ inputs			– 4.8			– 1.2				mA
				S inputs			– 6.4			– 1.6				mA
				Carry input			– 8			– 2				mA
			V_I = 0.5V	Mode input									– 2	mA
				$\overline{A}$ or $\overline{B}$ inputs									– 6	mA
				S inputs									– 8	mA
				Carry input									– 10	mA
I_{OH}	HIGH-level output current	V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V A = B only					250			100			250	μA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX Any output except A = B		Mil	– 20		– 55	– 15		– 100	– 40		– 100	mA
				Com'l	– 18		– 57	– 15		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Note 4a	Mil		88	127		20	32		120	220	mA
				Com'l		88	140		20	34		120	220	mA
			Note 4b	Mil		94	135		21	35		120	220	mA
				Com'l		94	150		21	37		120	220	mA

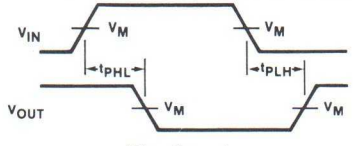
NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with the following conditions: a. S_0 through S_3, M, and A inputs are at 4.5V, other inputs grounded, all outputs open. b. S_0 through S_3 and M inputs are at 4.5V, other inputs grounded, all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

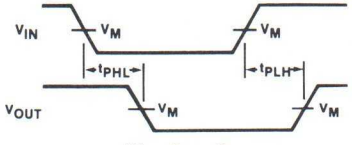
AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74 $C_L = 15pF$ $R_L = 400\Omega$		54/74LS $C_L = 15pF$ $R_L = 2k\Omega$		54/74S $C_L = 15pF$ $R_L = 280\Omega$		UNIT
		Min	Max	Min	Max	Min	Max	
t_{PLH} Propagation delay t_{PHL} C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		18 19		27 20		10.5 10.5	ns
t_{PLH} Propagation delay t_{PHL} C_n to $\overline{F}$ outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		19 18		26 20		12 12	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		19 19		29 23		12 12	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{G}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		25 25		32 32		15 15	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		19 25		30 30		12 12	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to $\overline{P}$ output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		25 25		30 33		15 15	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_1 = S_2 = 0V, S_0 = S_3 = 4.5V Sum Mode, see Waveform 2 and Table I		42 32		32 20		16.5 16.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		48 34		32 32		20 22	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}_i$ or $\overline{B}_i$ inputs to $\overline{F}_i$ outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		48 34		33 38		20 22	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	M = 0V, S_0 = S_3 = 4.5V, S_1 = S_2 = 0V Sum Mode, see Waveform 1 and Table I		43 41		38 38		18.5 18.5	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to C_{n+4} output	M = 0V, S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 4 and Table II		50 50		41 41		23 23	ns
t_{PLH} Propagation delay t_{PHL} $\overline{A}$ or $\overline{B}$ inputs to A = B output	M = S_0 = S_3 = 0V, S_1 = S_2 = 4.5V Diff Mode, see Waveform 3 and Table II		50 48		50 62		23 30	ns

AC WAVEFORMS

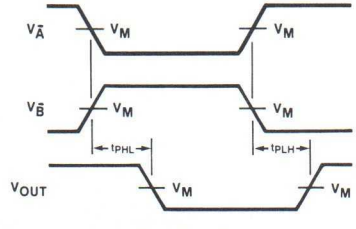


Waveform 1

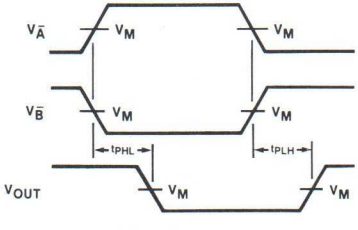


Waveform 2

V_M = 1.5V for 54/74 & 54S/74S; V_M = 1.3V for 54LS/74LS



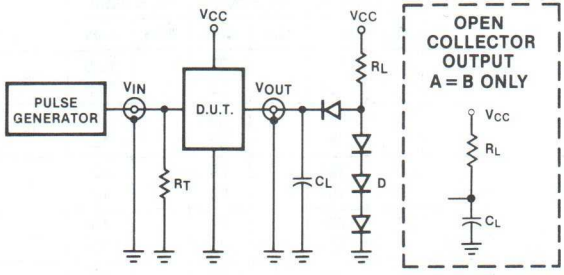
Waveform 3



Waveform 4

TEST CIRCUITS AND WAVEFORMS

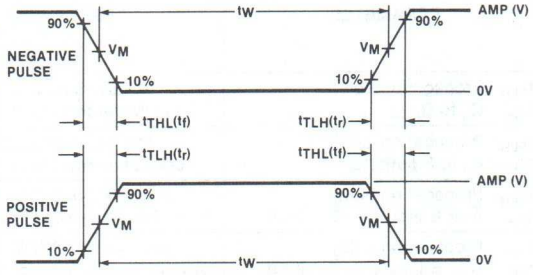
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

CARRY GENERATOR 54/74S182

Lookahead Carry Generator

- **Provides carry lookahead across a group of four ALU's**
- **Multi-level lookahead for high-speed arithmetic operation over long word lengths**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S182	5.8ns	69mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S182N	
Ceramic DIP	N74S182F	S54S182F
Flatpack		S54S182W

DESCRIPTION

The '182 carry lookahead generator accepts up to four pairs of active LOW Carry Propagate ($\overline{P}_0$, $\overline{P}_1$, $\overline{P}_2$, $\overline{P}_3$) and Carry Generate ($\overline{G}_0$, $\overline{G}_1$, $\overline{G}_2$, $\overline{G}_3$) signals and an active HIGH Carry input (C_n) and provides anticipated active HIGH carries (C_{n+x}, C_{n+y}, C_{n+z}) across four groups of binary adders. The '182 also has active LOW Carry Propagate ($\overline{P}$) and Carry Generate ($\overline{G}$) outputs which may be used for further levels of lookahead.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0 C_n$$

$$C_{n+y} = G_1 + P_1 G_0 = P_1 P_0 C_n$$

$$C_{n+z} = G_2 + P_2 G_1 + P_2 P_2 G_0 + P_2 P_1 P_0 C_n$$

$$\overline{G} = \overline{G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0}$$

$$\overline{P} = \overline{P_3 P_2 P_1 P_0}$$

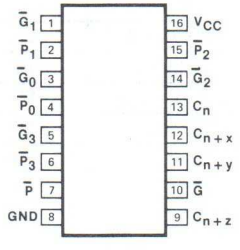
The '182 can also be used with binary ALU's in an active LOW or active HIGH input operand mode. The connections to and from the ALU to the carry lookahead generator are identical in both cases.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

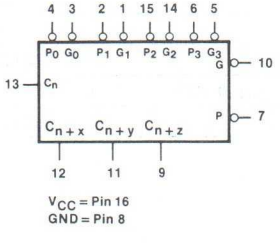
PINS	DESCRIPTION	54/74S
C_n	Input	1Sul
$\overline{P}_3$	Input	2Sul
$\overline{P}_2$	Input	3Sul
$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$	Inputs	4Sul
$\overline{G}_0$, $\overline{G}_2$	Inputs	7Sul
$\overline{G}_1$	Input	8Sul
All	Outputs	10Sul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

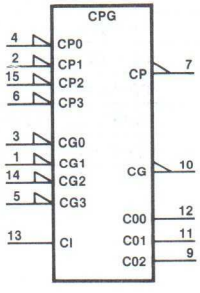
PIN CONFIGURATION



LOGIC SYMBOL

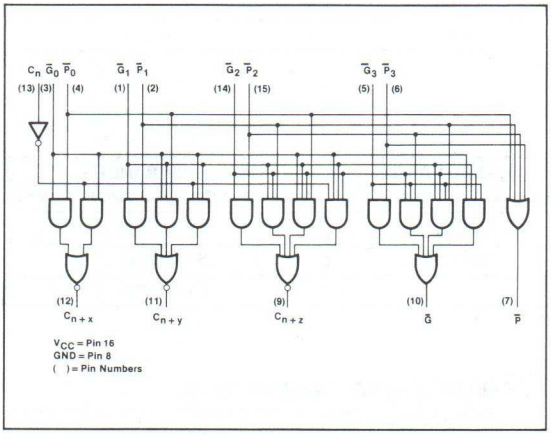


LOGIC SYMBOL (IEEE/IEC)



CARRY GENERATOR 54/74S182

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS									OUTPUTS				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	X	H	H	H	H	X					L		
X	H	H	X	H	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	L	H	L					H		
X	X	X	X	L	X	L					H		
X	L	X	X	L	L	L					H		
H	X	L	X	L	L	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		X	H	H	H	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	H	X	L	X				L	
	X		X	X	X	X	X	L				L	
	X		X	L	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		X		X					H
		X		X		H		X					H
		L		X		L		L					L

H = HIGH voltage level
L = LOW voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

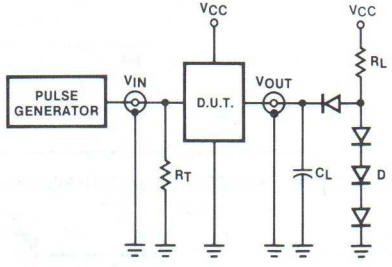
PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = + 0.7V MAX for 54S at T_A = + 125°C only.

3

TEST CIRCUITS AND WAVEFORMS

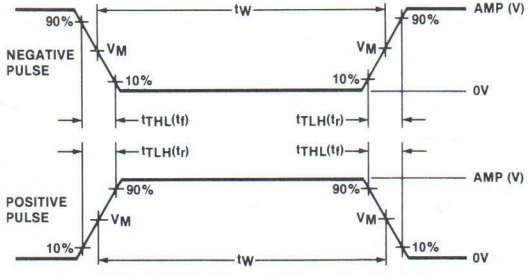
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

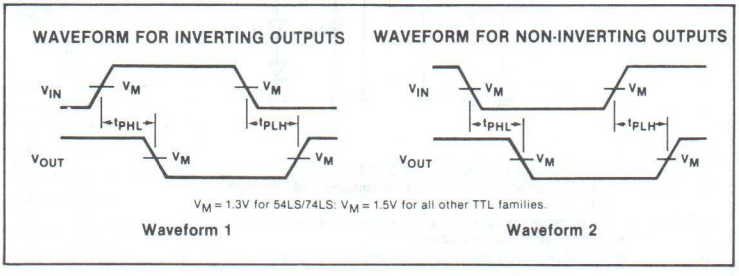
CARRY GENERATOR 54/74S182

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S182 Min	54/74S182 Typ[2]	54/74S182 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil			0.5[5]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	C_n input			50	μA
			$\overline{P}_3$ input			100	μA
			$\overline{P}_2$ input			150	μA
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$ inputs			200	μA
			$\overline{G}_0$, $\overline{G}_2$ inputs			350	μA
			$\overline{G}_1$ input			400	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	C_n input			− 2	mA
			$\overline{P}_3$ input			− 4	mA
			$\overline{P}_2$ input			− 6	mA
			$\overline{P}_0$, $\overline{P}_1$, $\overline{G}_3$ inputs			− 8	mA
			$\overline{G}_0$, $\overline{G}_2$ inputs			− 14	mA
			$\overline{G}_1$ input			− 16	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 40		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Mil		69	99	mA
			Com'l		69	109	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with $\overline{G}_0$, $\overline{G}_1$ and $\overline{G}_2$ inputs at 4.5V, all other inputs grounded and all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74S C_L = 15pF, R_L = 280Ω Min	54/74S C_L = 15pF, R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_n$ or $\overline{P}_n$ to any C output	Waveform 1		7.0 7.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{G}_n$ or $\overline{P}_n$ to $\overline{G}$ output	Waveform 2		7.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{P}_n$ to $\overline{P}$ output	Waveform 2		6.5 10	ns
t_{PLH} t_{PHL}	Propagation delay C_n to any C output	Waveform 2		10 10.5	ns

'190 Presettable BCD/Decade Up/Down Counter
'191 Presettable 4-Bit Binary Up/Down Counter

- **Synchronous, reversible counting**
- **BCD/decade — '190**
  4-bit binary — '191
- **Synchronous, reversible counting**
- **Asynchronous parallel load capability**
- **Count enable control for synchronous expansion**
- **Single Up/Down control input**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74190	25MHz	65mA
74191	25MHz	65mA
74LS191	25MHz	20mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74190N N74191N • N74LS191N	
Ceramic DIP	N74190F N74191F • N74LS191F	S54190F S54191F • S54LS191F
Flatpack		S54190W S54191W • S54LS191W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
$\overline{CE}$	Input	3ul	3LSul
Other	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

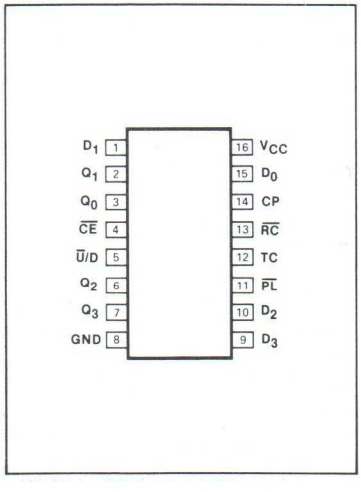
DESCRIPTION

The '190 is an asynchronously presettable up/down BCD decade counter. It contains four master/slave flip-flops with internal gating and steering logic to provide asynchronous preset and synchronous count-up and count-down operation. The '191 is similar, but is a 4-bit binary counter.

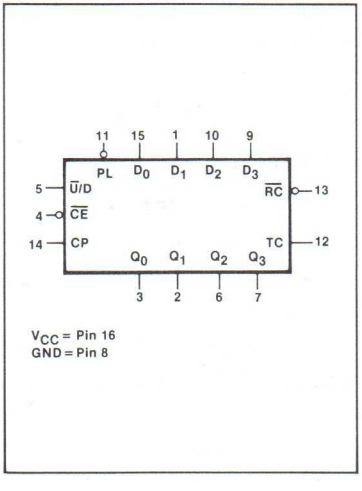
Asynchronous parallel load capability permits the counter to be preset to any desired number. Information present on the parallel Data inputs (D_0-D_3) is loaded into the counter and appears on the outputs when the Parallel Load ($\overline{PL}$) input is LOW. As indicated in the Mode Select Table, this operation overrides the counting function.

Counting is inhibited by a HIGH level on the Count Enable ($\overline{CE}$) input. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the Clock input. The Up/Down ($\overline{U}$/D) input signal determines the direction of counting as indicated in the Mode Select Table. The $\overline{CE}$ input may go LOW when the clock is in either state, however, the LOW-to-HIGH $\overline{CE}$ transition must occur only when the clock is HIGH. Also, the $\overline{U}$/D input should be changed only when either $\overline{CE}$ or CP is HIGH.

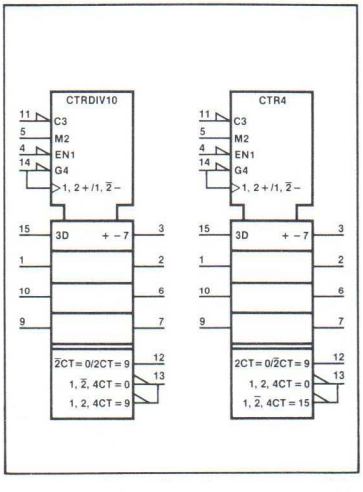
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Overflow/underflow indications are provided by two types of outputs, the Terminal Count (TC) and Ripple Clock ($\overline{RC}$). The TC output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches "9" in the count-up mode. The TC output will remain HIGH until a state change occurs, either by counting or presetting, or until $\overline{U}$/D is changed. Do not use the TC output as a clock signal because it is subject to decoding spikes.

The TC signal is used internally to enable the $\overline{RC}$ output. When TC is HIGH and $\overline{CE}$ is LOW, the RC follows the Clock Pulse (CP) delayed by two gate delays. The $\overline{RC}$ output essentially duplicates the LOW clock pulse width, although delayed in time by two gate delays. This feature simplifies the design of multistage counters, as indicated in Figures A and B. In Figure A, each $\overline{RC}$ output is used as the Clock input for the next higher stage. When the clock source has a limited drive capability this configuration is particularly advantageous, since the clock source drives only the first stage. It is only necessary to inhibit the first stage to prevent counting in all stages, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse as indicated in the Mode Select Table. The timing skew between state changes in the first and last stages is represented by the cumulative delay of the clock as it ripples through the preceding stages. This is a disadvantage of the configuration in some applications.

Figure B shows a method of causing state changes to occur simultaneously in all stages. The $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion and all Clock inputs are driven in parallel. The LOW state duration of the clock in this configuration must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. Since the $\overline{RC}$ output of any package goes HIGH shortly after its CP input goes HIGH, there is no such restriction on the HIGH state duration of the clock.

In Figure C, the configuration shown avoids ripple delays and their associated restrictions. Combining the TC signals from all the preceding stages forms the $\overline{CE}$ input signal for a given stage. An enable signal must be included in each carry gate in order to inhibit counting. The TC output of a given stage is not affected by its own $\overline{CE}$, therefore, the simple inhibit scheme of Figure A and B does not apply.

N-STAGE COUNTER USING RIPPLE CLOCK

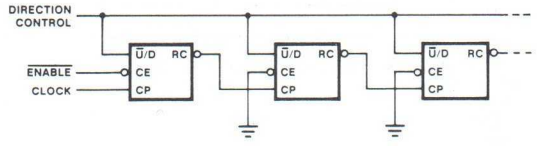


Figure A

SYNCHRONOUS N-STAGE COUNTER USING RIPPLE CARRY/BORROW

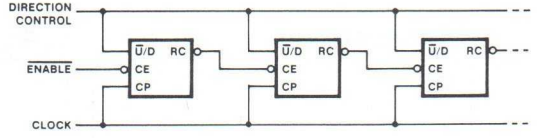


Figure B

SYNCHRONOUS N-STAGE COUNTER WITH PARALLEL GATED CARRY/BORROW

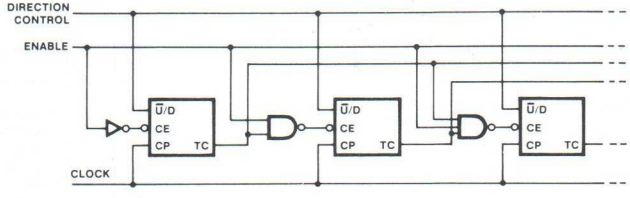
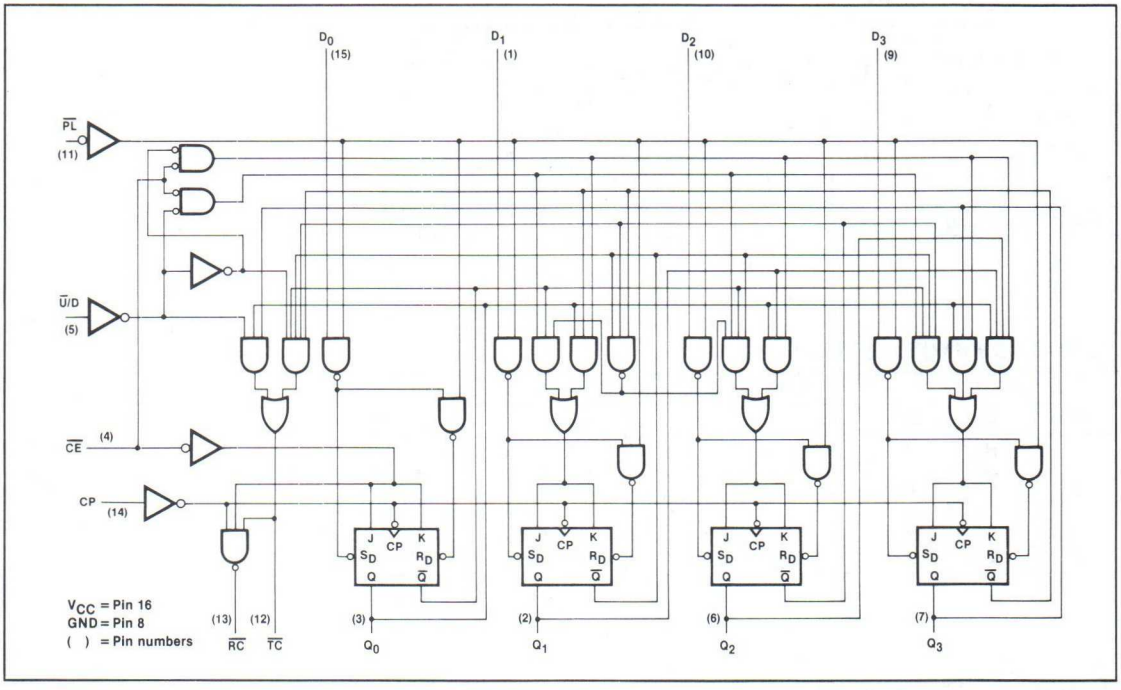
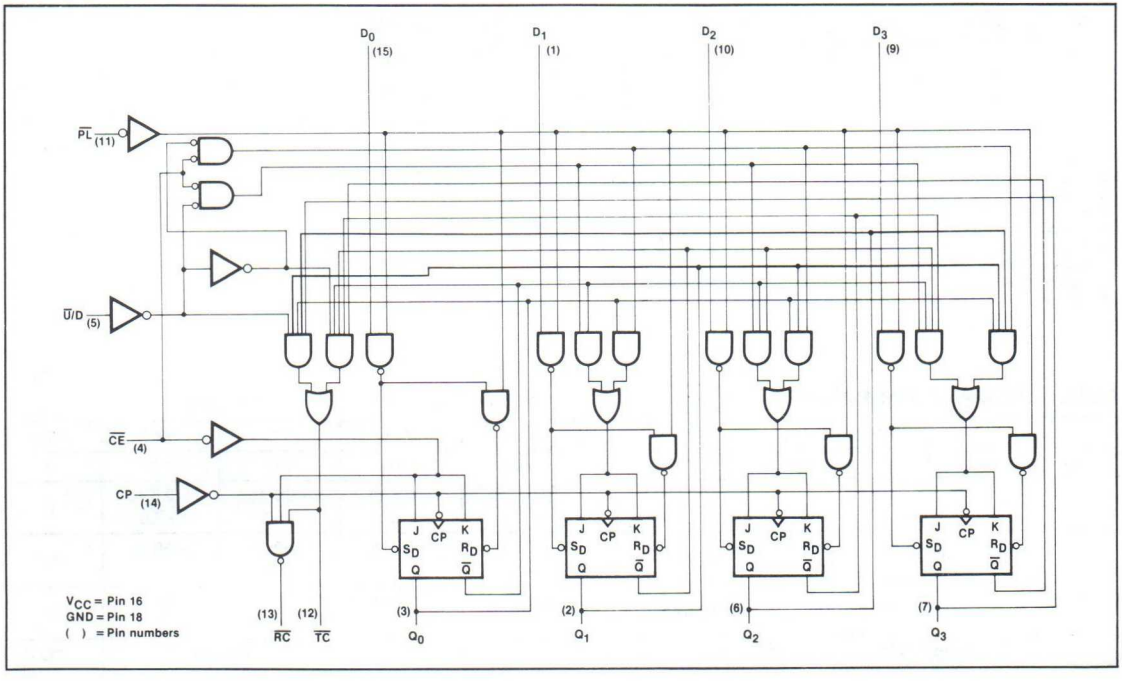


Figure C

LOGIC DIAGRAM '190



LOGIC DIAGRAM '191



MODE SELECT—FUNCTION TABLE, '190, '191

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}$/D	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L L	X X	X X	X X	L H	L H
Count up	H	L	⌐	↑	X	count up
Count down	H	H	⌐	↑	X	count down
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ FUNCTION TABLE, '190

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⌐	H	X	X	H	⌐	⌐
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌐	L	L	L	L	⌐	⌐

TC AND $\overline{RC}$ FUNCTION TABLE, '191

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}$/D	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	H	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⌐	H	H	H	H	⌐	⌐
L	H	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⌐	L	L	L	L	⌐	⌐

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
I = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.
⌐ = LOW pulse.
⌐ = TC goes LOW on a LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8			+ 0.7	V
		Com'l			+ 0.8			+ 0.8	V
I_{IK}	Input clamp current				− 12			− 18	mA
I_{OH}	HIGH-level output current				− 800			− 400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	− 55		+ 125	°C
		Com'l	0		70	0		70	°C

3

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74190, 191			54/74LS191			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MIN, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V	$\overline{CE}$ input						0.3	mA
				Other inputs						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V	$\overline{CE}$ input			120				μA
				Other inputs			40				μA
			V_I = 2.7V	$\overline{CE}$ input						60	μA
				Other inputs						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	$\overline{CE}$ input			-4.8			− 1.2	mA
				Other inputs			− 1.6			− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	-20		-65	-20		-100	mA
				Com'l	-18		-65	-20		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		65	99		20	35	mA
				Com'l		65	105		20	35	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

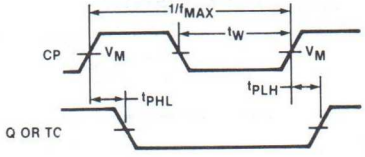
PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	20		20		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Q output	Waveform 1		24 36		24 36	ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{RC}$ output	Waveform 2		20 24		20 24	ns
t_{PLH} t_{PHL}	Propagation delay Clock to TC output	Waveform 1		42 52		42 52	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$ output	Waveform 7		45 45		45 45	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{U}$/D to TC output	Waveform 7		33 33		33 33	ns
t_{PLH} t_{PHL}	Propagation delay Data to Q outputs	Waveform 3		22 50		32 40	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to any output	Waveform 4		33 50		33 50	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$ output	Waveform 2		33 33		33 33	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

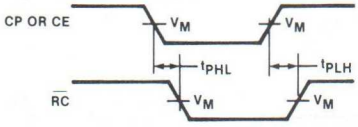
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	CP pulse width	Waveform 1	25		25		ns
t_W	$\overline{PL}$ pulse width	Waveform 5	35		35		ns
t_s	Setup time, Data to $\overline{PL}$	Waveform 6	20		20		ns
t_h	Hold time, Data to $\overline{PL}$	Waveform 6	0		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 5	40		40		ns
$t_s(L)$	Setup time, LOW $\overline{CE}$ to Clock	Waveform 8	40		40		ns
$t_h(L)$	Hold time, LOW $\overline{CE}$ to Clock	Waveform 8	0		0		ns

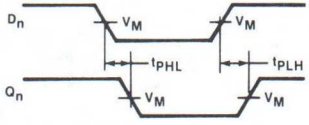
AC WAVEFORMS



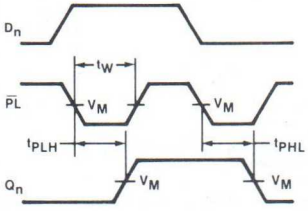
Waveform 1



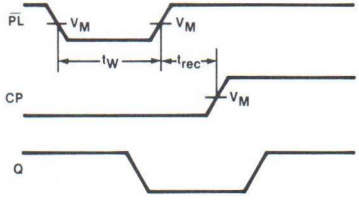
Waveform 2



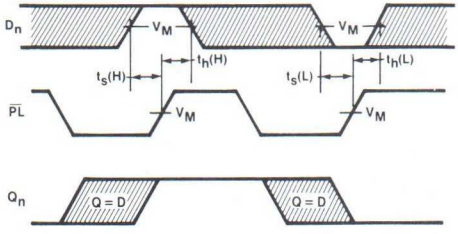
Waveform 3



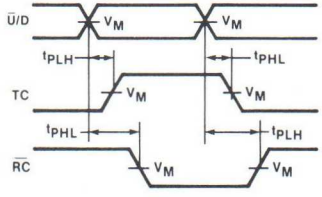
Waveform 4



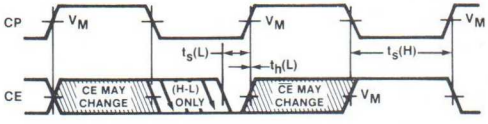
Waveform 5



Waveform 6



Waveform 7

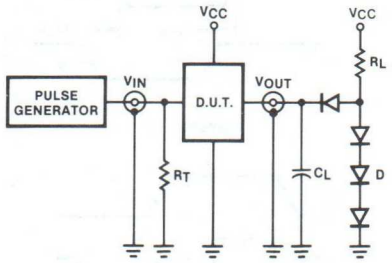


Waveform 8

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

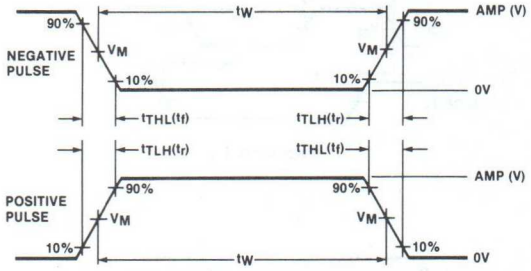
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTERS

54/74192, 54/74193, LS192, LS193

'192 Presettable BCD Decade Up/Down Counter
'193 Presettable 4-Bit Binary Up/Down Counter

- **Synchronous reversible 4-bit binary counting**
- **Asynchronous parallel load**
- **Asynchronous reset (clear)**
- **Expandable without external logic**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74192	32MHz	65mA
74LS192	32MHz	19mA
74193	32MHz	65mA
74LS193	32MHz	19mA

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74192N • N74LS192N N74193N • N74LS193N	
Ceramic DIP	N74192F • N74LS192F N74193F • N74LS193F	S54LS192F S54193F • S54LS193F
Flatpack		S54LS192W S54193W • S54LS193W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

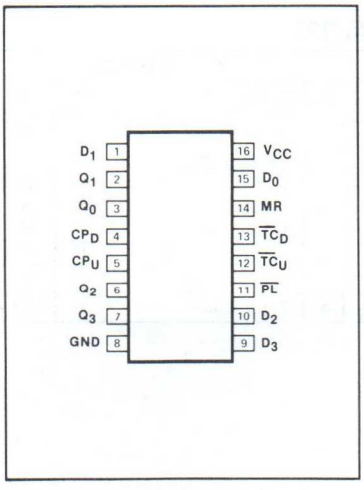
The '192 and '193 are 4-bit synchronous up/down counters — the '192 counts in BCD mode and the '193 counts in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either Clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up . . . if CP_D is pulsed while the CP_U is held HIGH, the device will count down. Only one Clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin — it may also be loaded in parallel by activating the asynchronous parallel load pin.

Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

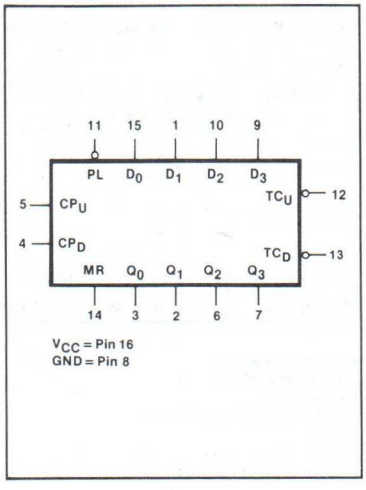
Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CPU_U input will advance the count by one.

One clock should be held HIGH while counting with the other, because the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

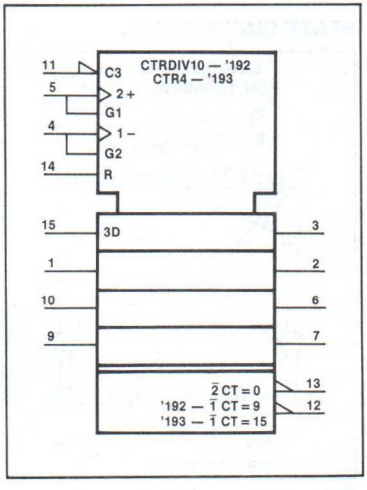
PIN CONFIGURATION



LOGIC SYMBOL



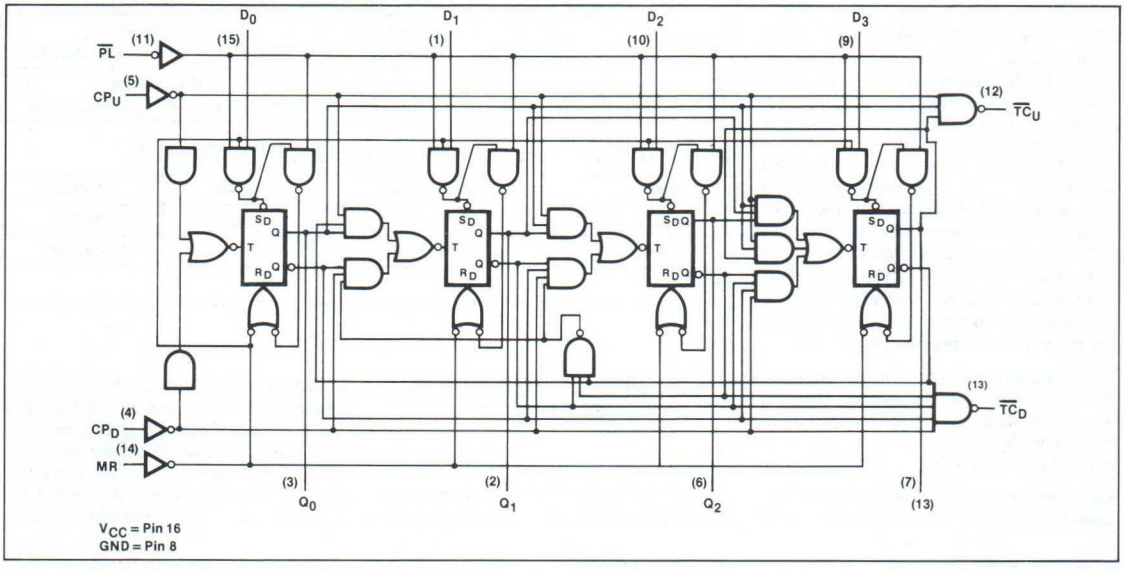
LOGIC SYMBOL (IEEE/IEC)



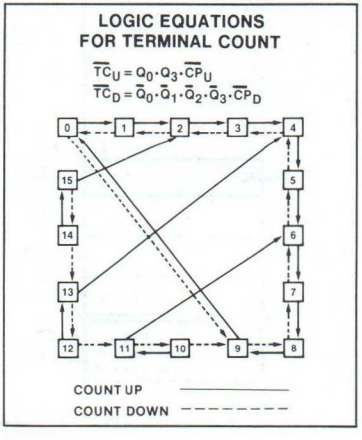
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 9 (for the '192 and 15 for the '193), the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two-gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs (D_0-D_3) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is LOW. A HIGH level on the Master Reset (MR) input will disable the parallel load gates, override both Clock inputs, and set all Q outputs LOW. If one of the Clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

LOGIC DIAGRAM, '192



STATE DIAGRAM, '192



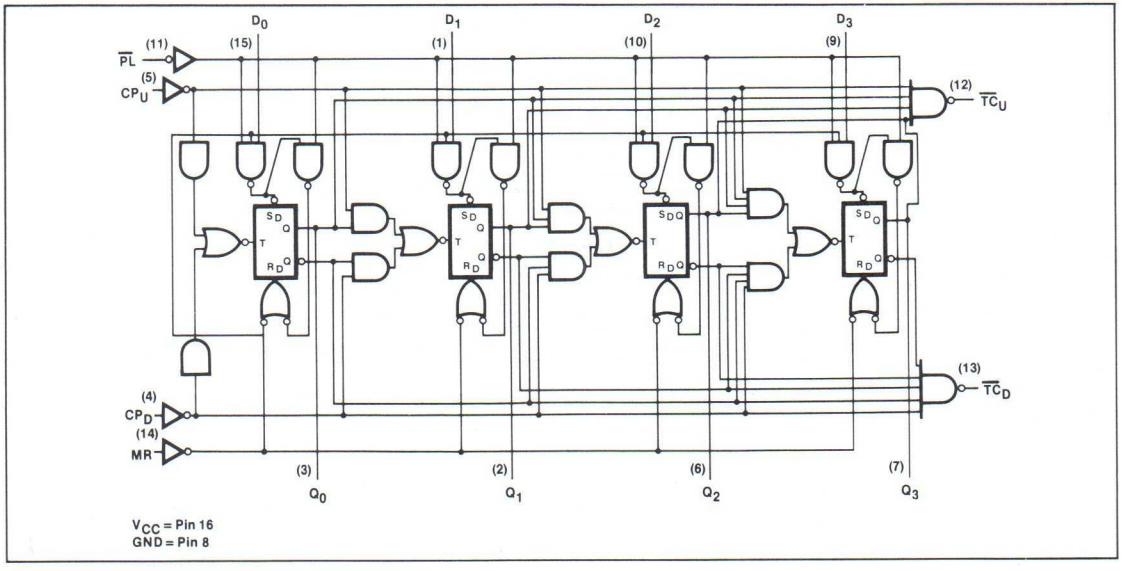
MODE SELECT—FUNCTION TABLE, '192

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	$Q_n = D_n$				L	H
	L	L	H	X	H	X	X	H	$Q_n = D_n$				H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[a]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[b]

H = HIGH voltage level
L = LOW voltage level
X = Dont' care
↑ = LOW-to-HIGH clock transition

NOTES
a. $\overline{TC}_U = CP_U$ at terminal count up (HLLH).
b. $\overline{TC}_D = CP_D$ at terminal count down (LLLL).

LOGIC DIAGRAM, '193

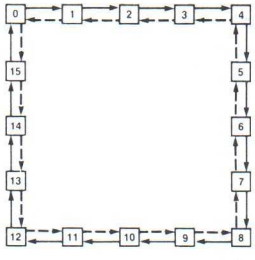


STATE DIAGRAM, '193

LOGIC EQUATIONS FOR TERMINAL COUNT

$\overline{TC}_U = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot \overline{CP}_U$

$\overline{TC}_D = \overline{Q}_0 \cdot \overline{Q}_1 \cdot \overline{Q}_2 \cdot \overline{Q}_3 \cdot \overline{CP}_D$



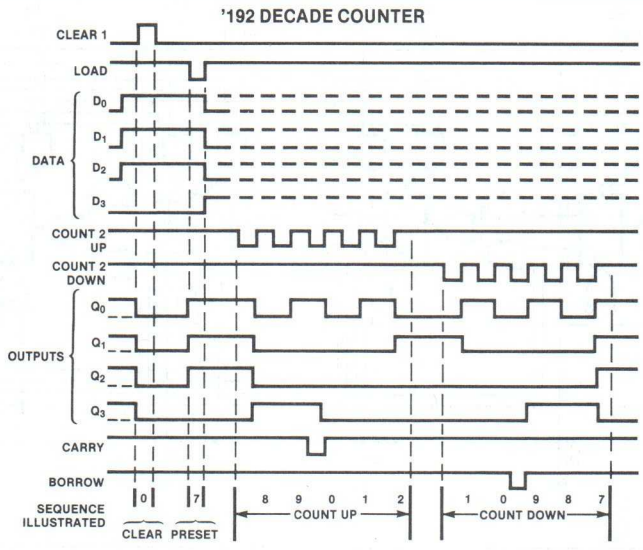
MODE SELECT—FUNCTION TABLE, '193

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[c]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[d]

H = HIGH voltage level
L = LOW voltage level
X = Dont' care
↑ = LOW-to-HIGH clock transition

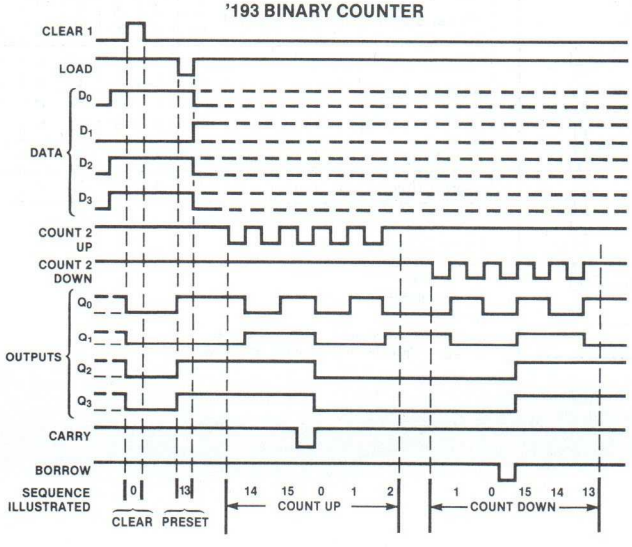
NOTES
c. $TC_U = CP_U$ at terminal count up (HHHH).
d. $TC_D = CP_D$ at terminal count down (LLLL).

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, cout-up input must be high.

FUNCTIONAL WAVEFORMS (Typical clear, load, and count sequences)



NOTES
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be high; when counting down, count-up input must be high.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to ÷5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	mA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74192, '193			54/74LS192, '193			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4	V
				Com'l		0.2	0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−1.6			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	−20		−65	−20		−100	mA
				Com'l	−18		−65	−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		65	89		19	34	mA
				Com'l		65	102		19	34	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Parallel Load and Master Reset inputs grounded, all other outputs at 4.5V and all outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum input count frequency	Waveform 1	25		25		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U input to $\overline{TC}_U$ output	Waveform 2		26 24		26 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_D input to $\overline{TC}_D$ output	Waveform 2		24 24		24 24	ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Q_n outputs	Waveform 1		38 47		38 47	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ input to Q_n output	Waveform 3		40 40		40 40	ns
t_{PHL}	Propagation delay, MR to output	Waveform 4		35		35	ns

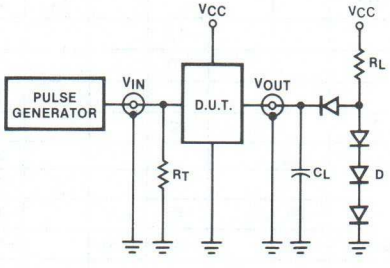
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	CP_U pulse width	Waveform 1	20		20		ns
t_W	CP_D pulse width	Waveform 1	20		20		ns
t_W	$\overline{PL}$ pulse width	Waveform 3	20		20		ns
t_W	MR pulse width	Waveform 4	20		20		ns
t_s	Setup time, Data to $\overline{PL}$	Waveform 5	20		20		ns
t_h	Hold time, Data to $\overline{PL}$	Waveform 5	0		5		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP	Waveform 3	40		40		ns
t_{rec}	Recovery time, MR to CP	Waveform 4	40		40		ns

TEST CIRCUITS AND WAVEFORMS

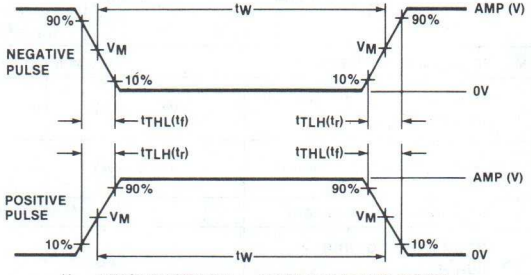
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

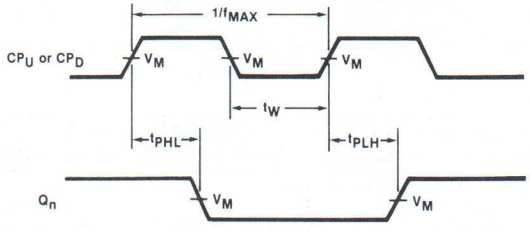


$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

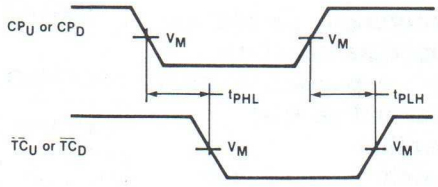
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



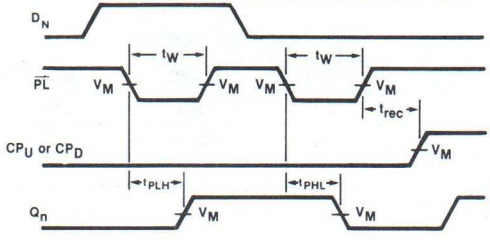
Waveform 1

CLOCK TO TERMINAL COUNT DELAYS



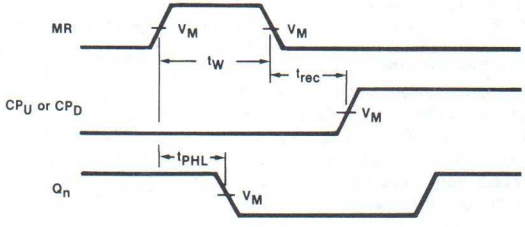
Waveform 2

PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAYS, AND PARALLEL LOAD TO CLOCK RECOVERY TIME



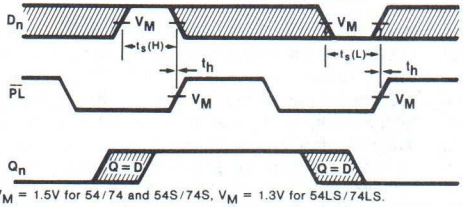
Waveform 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 4

SETUP AND HOLD TIMES DATA TO PARALLEL LOAD (PL)

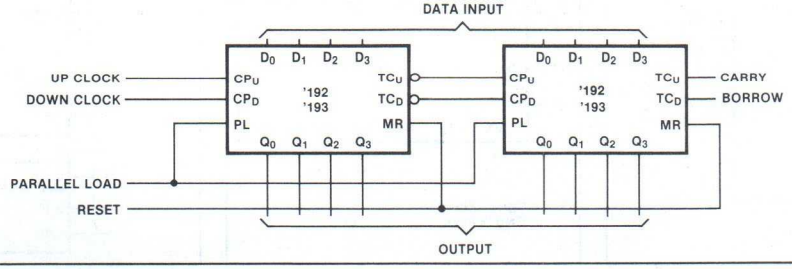


V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 5

APPLICATION

8-BIT UP/DOWN COUNTER WITH PARALLEL LOAD



SHIFT REGISTERS 54/74194, LS194A, S194

4-Bit Bidirectional Universal Shift Register

- **Buffered clock and control inputs**
- **Shift left and shift right capability**
- **Synchronous parallel and serial data transfers**
- **Easily expanded for both serial and parallel operation**
- **Asynchronous Master Reset**
- **Hold (do nothing) mode**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74194	36MHz	39mA
74LS194A	36MHz	15mA
74S194	105MHz	85mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74194N • N74LS194AN N74S194N	
Ceramic DIP	N74194F • N74LS194AF N74S194F	S54194F • S54LS194AF S54S194F
Flatpack		S54194W • S54LS194AW S54S194W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
Q_0–Q_3	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

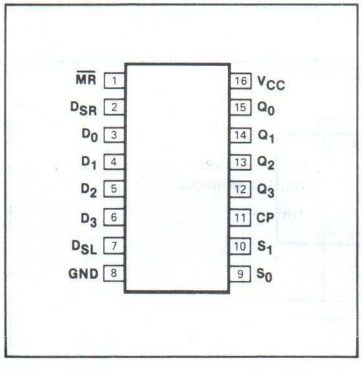
The functional characteristics of the '194 4-Bit Bidirectional Shift Register are indicated in the Logic Diagram and Function Table. The register is fully synchronous, with all operations taking place in less than 20ns (typical) for the 54/74 and 54LS/74LS, and 12ns (typical) for 54S/74S, making the device especially useful for implementing very high speed CPUs, or for memory buffer registers.

The '194 design has special logic features which increase the range of application. The synchronous operation of the device is determined by two Mode Select inputs, S_0 and S_1. As shown in the Mode Select Table, data can be entered and shifted from left to right (shift right, $Q_0 \rightarrow Q_1$, etc.) or, right to left (shift left, $Q_3 \rightarrow Q_2$, etc.) or, parallel data can be entered, loading all 4 bits of the register simultaneously. When both S_0 and S_1 are LOW, existing data is retained in a hold (do nothing) mode. The first and last stages provide D-type Serial Data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

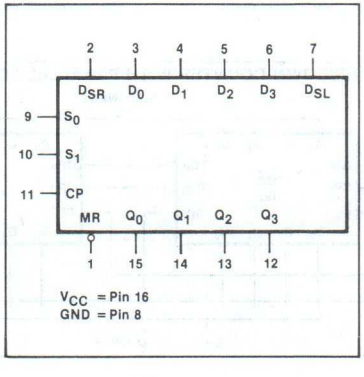
Mode Select and Data inputs on the 54S/74S194 and 54LS/74LS194A are edge-triggered, responding only to the LOW-to-HIGH transition of the Clock (CP). Therefore, the only timing restriction is that the Mode Control and selected Data inputs must be stable one setup time prior to the positive transition of the clock pulse. The Mode Select inputs of the 54/74194 are gated with the clock and should be changed from HIGH-to-LOW only while the Clock input is HIGH.

The four parallel data inputs (D_0–D_3) are D-type inputs. Data appearing on D_0–D_3 inputs when S_0 and S_1 are HIGH is transferred to the Q_0–Q_3 outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous Master Reset ($\overline{MR}$) overrides all other input conditions and forces the Q outputs LOW.

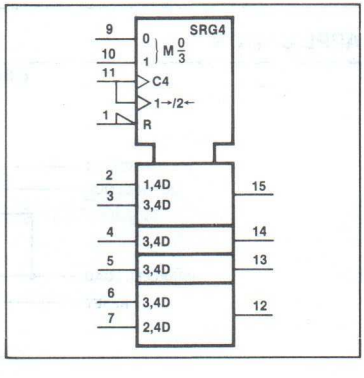
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS							OUTPUTS			
	CP	$\overline{MR}$	S_1	S	D_{SR}	D_{SL}	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	X	L	X	X	X	X	X	L	L	L	L
Hold (do nothing)	X	H	l[a]	l[a]	X	X	X	q_0	q_1	q_2	q_3
Shift Left	↑	H	h	l[a]	X	l	X	q_1	q_2	q_3	L
	↑	H	h	l[a]	X	h	X	q_1	q_2	q_3	H
Shift Right	↑	H	l[a]	h	l	X	X	L	q_0	q_1	q_2
	↑	H	l[a]	h	h	X	X	H	q_0	q_1	q_2
Parallel Load	↑	H	h	h	X	X	d_n	d_0	d_1	d_2	d_3

H = HIGH voltage level

h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.

L = LOW voltage level.

l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.

$d_n(q_n)$ = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.

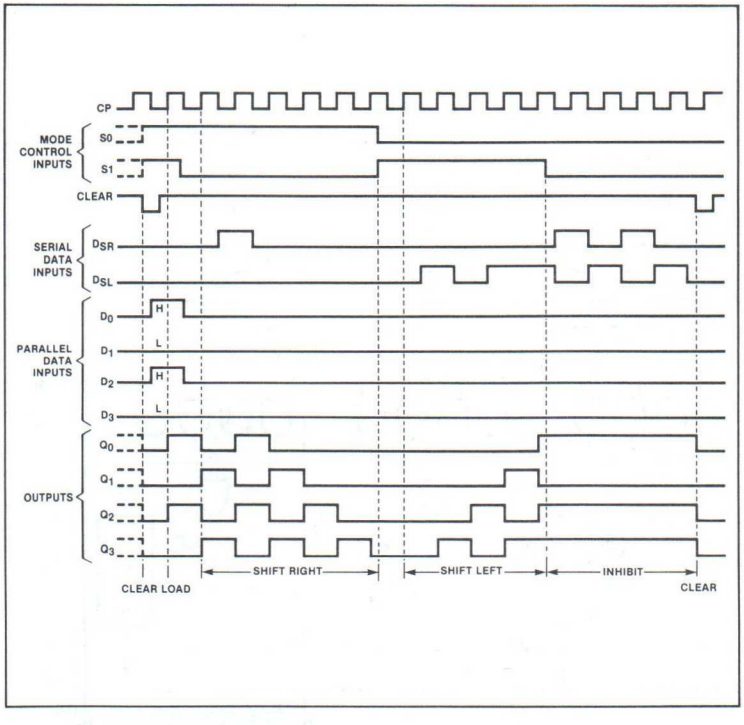
X = Don't care.

↑ = LOW-to-HIGH clock transition.

NOTES

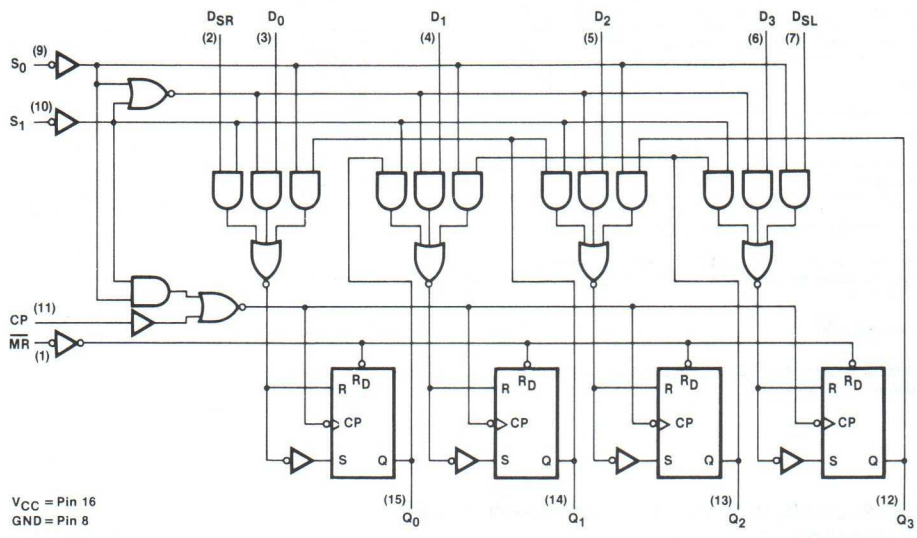
a. The HIGH-to-LOW transition of the S_0 and S_1 inputs on the 54/74194 should only take place while CP is HIGH for conventional operation.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



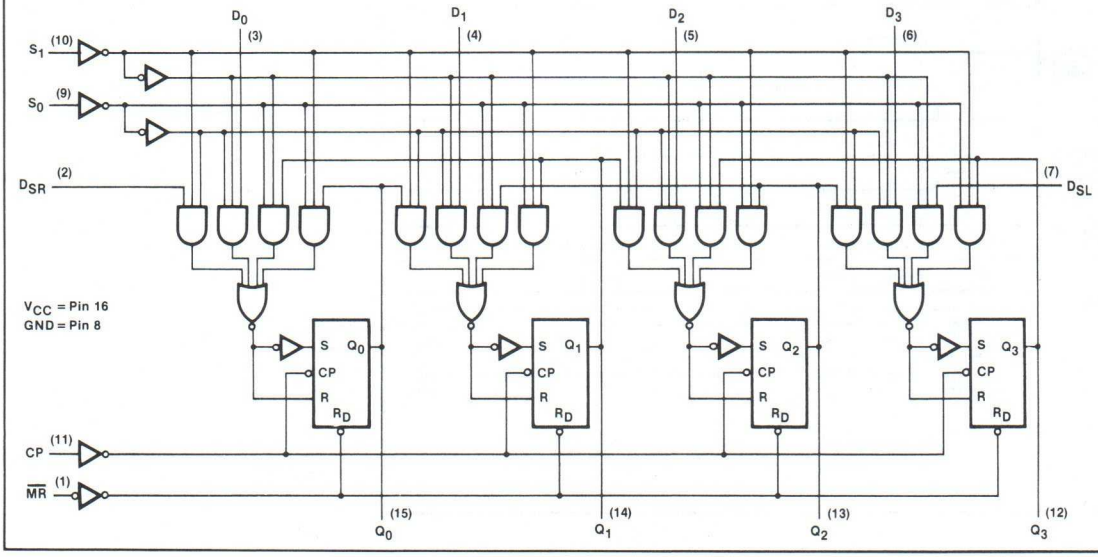
LOGIC DIAGRAM

54/74194



LOGIC DIAGRAM

54S/74S194, 54LS/74LS194A



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74194			54/74LS194A			54/74S194			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.5		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.5		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5[5]	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 1.6			– 0.4				mA
			V_I = 0.5V										– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	– 40		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				39	63		15	23		85	135	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, D_i inputs grounded and 4.5V applied to S_0, S_1, $\overline{MR}$ and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CP.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		25		70		MHz
t_{PLH}	Propagation delay Clock to output	Waveform 1		22		22	4.0	12	ns
t_{PHL}				26		26	4.0	16.5	
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		37		30		18.5	ns

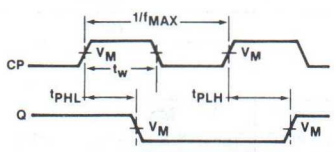
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W(L)	Clock pulse width, HIGH	Waveform 1	20		20		7		ns
t_W(L)	$\overline{MR}$ pulse width, LOW	Waveform 2	20		20		12		ns
t_s	Setup time, Data to Clock	Waveform 3	20		20		5.0		ns
t_h	Hold time, Data to Clock	Waveform 3	0		0		3.0		ns
t_s(L)	Setup time LOW, S_n to CP[(a)]	Waveform 4	30		30		11		ns
t_s(H)	Setup time HIGH, S_N to CP	Waveform 4	30		30		11		ns
t_h	Hold time, S_n to CP	Waveform 4	0		0		3.0		ns
t_{rec}	Recovery time, $\overline{MR}$ to CP	Waveform 2	25		25		9.0		ns

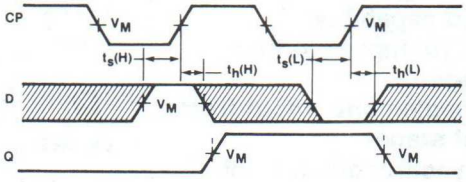
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SET-UP AND HOLD TIMES

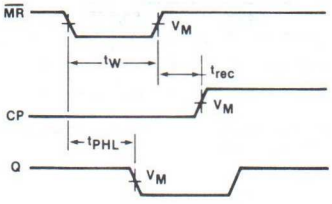


Waveform 3

V_M = 1.5V for 54S/74S; V_M = 1.3V for 54LS/74LS.

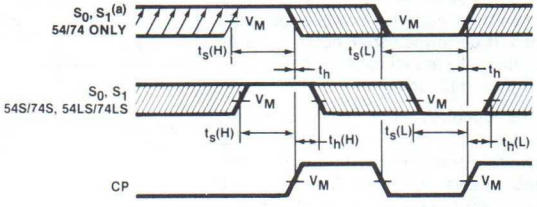
The shaded areas indicate when the input is permitted to change predictable output performance

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

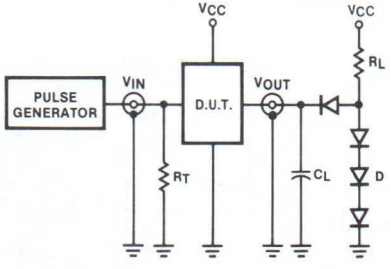
SETUP AND HOLD TIMES FOR S_0 AND S_1 INPUTS



Waveform 4

TEST CIRCUITS AND WAVEFORMS

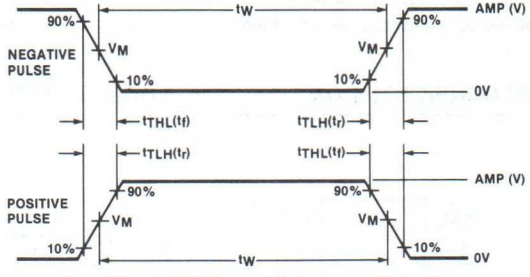
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTERS

54/74195, LS195A, S195

4-Bit Parallel Access Shift Register

- **Buffered Clock and Control inputs**
- **Shift right and parallel load capability**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Complement output from last stage**
- **Asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74195	39MHz	39mA
74LS195A	39MHz	14mA
74S195	105MHz	70mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74195N • N74LS195AN N74S195N	
Ceramic DIP	N74195F • N74LS195AF N74S195F	S54LS195AF
Flatpack		S54LS195AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74	54/74S	54/74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

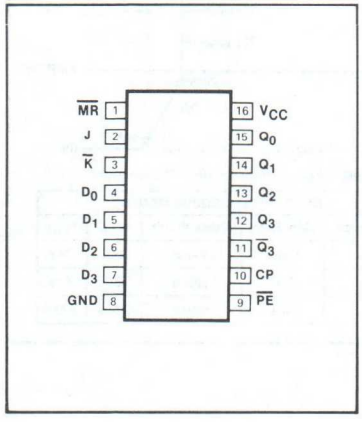
The functional characteristics of the '195 4-Bit Parallel Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial-to-parallel, or parallel-to-serial data transfers at very high speeds.

The '195 operates on two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted 1 bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the JK type input for special applications and, by tying the two pins together, the simple D type input for general applications. The device appears as four common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0–D_3) is transferred to the respective Q_0–Q_3 outputs. Shift left operation ($Q_3 \rightarrow Q_2$) can be achieved by tying the Q_n outputs to the D_{n-1} inputs and holding the $\overline{PE}$ input low.

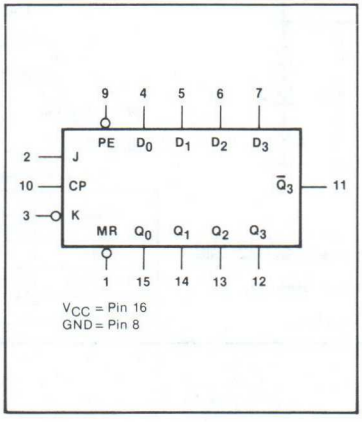
All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '195 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

A LOW on the asynchronous Master Reset ($\overline{MR}$) input sets all Q outputs LOW, independent of any other input condition. The $\overline{MR}$ on the 54/74195 is gated with the clock. Therefore, the LOW-to-HIGH $\overline{MR}$ transition should only occur while the clock is LOW to avoid false clocking on the 54/74195.

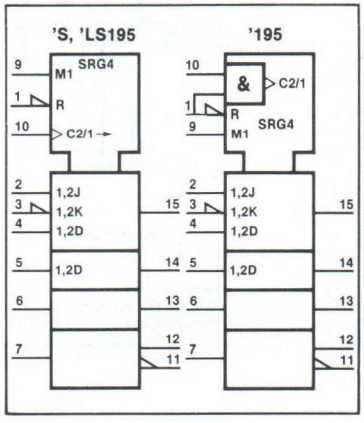
PIN CONFIGURATION



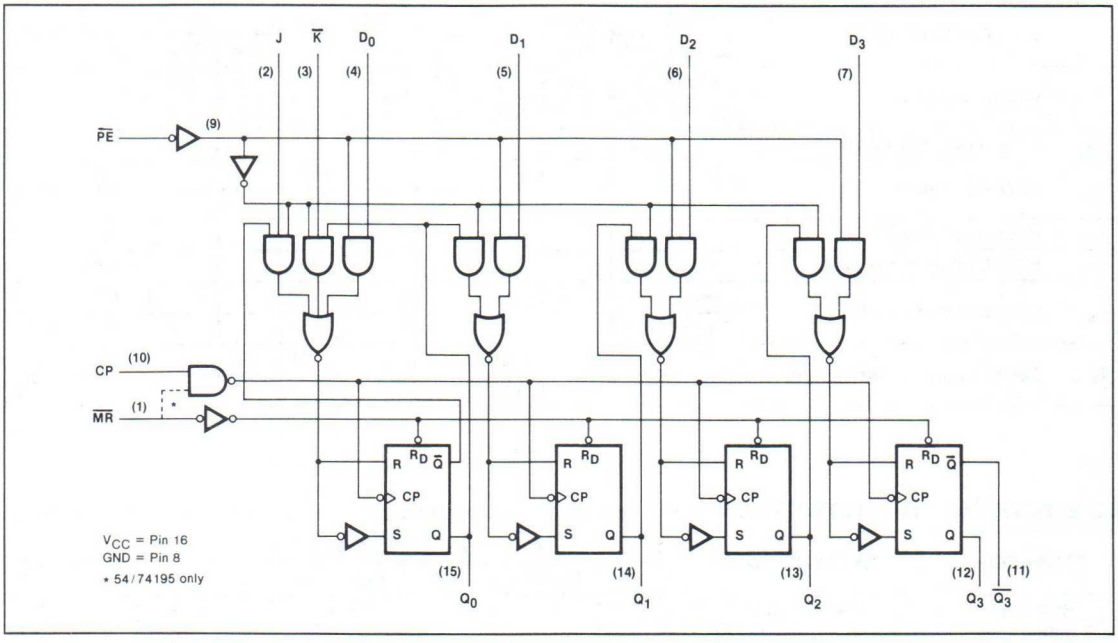
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H = HIGH voltage level.
L = LOW voltage level.
X = Don't care.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
d_n (q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	54S	74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125			0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7			+0.8	V
		Com'l			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18			−18	mA
I_{OH}	HIGH-level output current				−800			−400			−1000	μA
I_{OL}	LOW-level output current	Mil			16			4			20	mA
		Com'l			16			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74195			54/74LS195A			54/74S195			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.2	0.4		0.25	0.4			0.5	V
				Com'l		0.2	0.4		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5			−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0						1.0	mA
			V_I = 7.0V							0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40							μA
			V_I = 2.7V							20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				−1.6			−0.4				mA
			V_I = 0.5V										−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	−20		−57	−20		−100	−40		−100	mA
				Com'l	−18		−57	−20		−100	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX		Mil		39	63		14	21		70	99	mA
				Com'l		39	63		14	21		70	109	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open, $\overline{PE}$ grounded, and 4.5V applied to the J, $\overline{K}$, and Data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5V to $\overline{MR}$, and then a momentary ground, followed by 4.5V to clock.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		54S/74S $C_L = 15pF$, $R_L = 280\Omega$		UNIT
			Min	Max	Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		30		70		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		22 26		22 26		12 16.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		30		30		18.5	ns

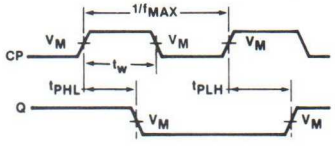
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	16		16		7		ns
t_W	Master Reset pulse width	Waveform 2	12		12		12		ns
t_s	Setup time, J, $\overline{K}$ and Data to Clock	Waveform 3	20		15		5.0		ns
t_h	Hold time, J, $\overline{K}$ and Data to Clock	Waveform 3	0		0		3.0		ns
t_s	Setup time, $\overline{PE}$ to Clock	Waveform 4	25		25		11		ns
t_h	Hold time, $\overline{PE}$ to Clock	Waveform 4	0		0		0		ns
t_{rec}	Recovery time, $\overline{MR}$ to Clock	Waveform 2	25		25		9.0		ns

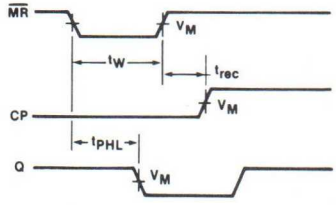
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



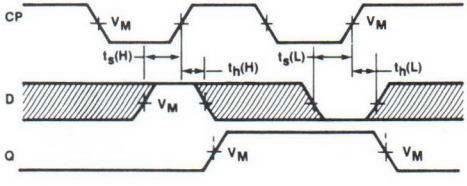
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



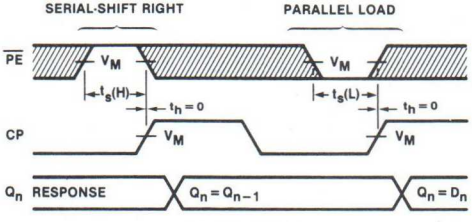
Waveform 2

DATA SET-UP AND HOLD TIMES



Waveform 3

SETUP AND HOLD TIMES PARALLEL ENABLE TO CLOCK

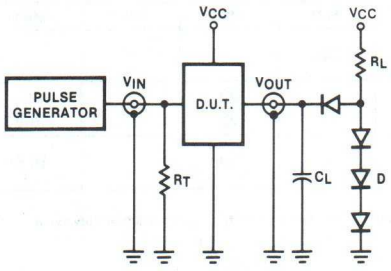


Waveform 4

$V_M = 1.5V$ for 54/74 and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

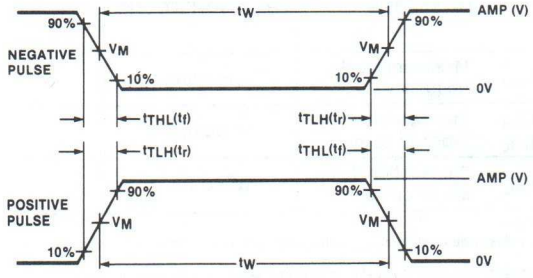
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER 54/74LS197

Presettable 4-Bit Binary Ripple Counter

- **High speed 4-bit binary counting**
- **Asynchronous parallel load for presetting counter**
- **Overriding Master Reset**
- **Buffered Q_0 output drives $\overline{CP}_1$ input plus standard fan-out**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74LS197	40MHz	16mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS197N	
Ceramic DIP	N74LS197F	S54LS197F
Flatpack		S54LS197W

DESCRIPTION

The '197 is an asynchronously presettable binary ripple counter partitioned into divide-by-2 and divide-by-8 sections with each section having a separate Clock input. State changes are initiated in the counting modes by the HIGH-to-LOW transition of the Clock inputs, however, state changes of the Q outputs do not occur simultaneously because of the internal ripple delays. Designers should keep in mind when using external logic to decode the Q outputs, that the unequal delays can lead to decoding spikes, and thus a decoded signal should not be used as a strobe or clock. The Q_0 flip-flop is triggered by the $\overline{CP}_0$ input while the $\overline{CP}_1$ input triggers the divide-by-8 section.

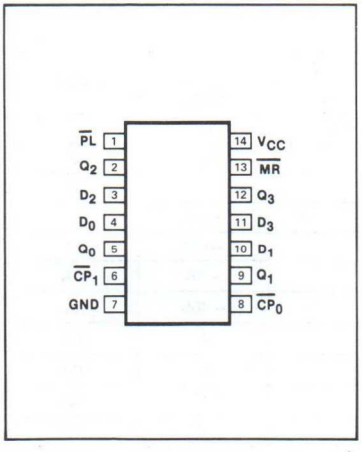
The device has an asynchronous active-LOW Master Reset ($\overline{MR}$) input which overrides all other inputs and forces all outputs LOW. The counter is also asynchronously presettable. A LOW on the Parallel Load ($\overline{PL}$) input overrides the Clock inputs and loads the data from parallel Data (D_0-D_3) inputs into the flip-flops. The counter acts as a transparent latch while the $\overline{PL}$ is LOW and any change in the D_n inputs will be reflected in the outputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

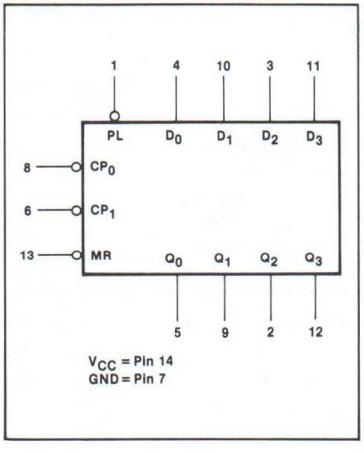
PINS	DESCRIPTION	54/74LS
$\overline{CP}_0$	Clock input	6LSul
$\overline{CP}_1$	Clock input	3.5LSul
All	Other inputs	1LSul
Q_0-Q_3	Outputs	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

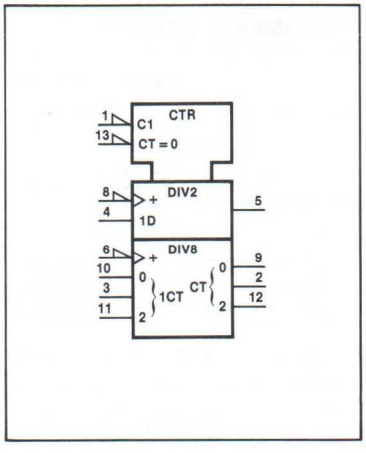
PIN CONFIGURATION



LOGIC SYMBOL

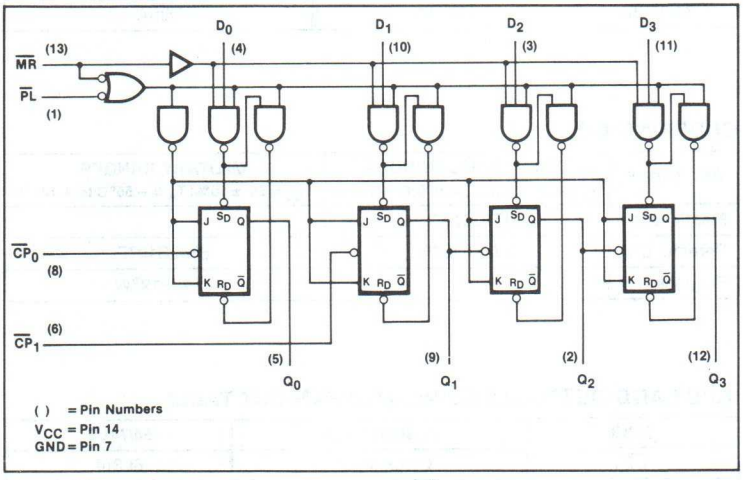


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS197

LOGIC DIAGRAM



COUNT SEQUENCE

COUNT	4-BIT BINARY[1]			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE
1. Q_0 connected to input $\overline{CP}_1$; input applied to $\overline{CP}_0$.

MODE SELECT— FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUT
	$\overline{MR}$	$\overline{PL}$	$\overline{CP}$	D_n	Q_n
Reset (Clear)	L	X	X	X	L
Parallel Load	H	L	X	L	L
	H	L	X	H	H
Count	H	H	↓	X	count

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↓ = HIGH-to-LOW Clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS197			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V	D_0-D_3, $\overline{PL}$				0.1	mA
			$\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$				0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	D_0-D_3, $\overline{PL}$				20	μA
			$\overline{MR}$, $\overline{CP_0}$, $\overline{CP_1}$				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	D_0-D_3, $\overline{PL}$				– 0.4	mA
			$\overline{MR}$ input				– 0.8	mA
			$\overline{CP_0}$ input				– 2.4	mA
			$\overline{CP_1}$ input				– 1.3	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				16	27	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54LS/74LS C_L = 15pF, R_L = 2kΩ		UNIT
				Min	Max	
f_{MAX}	Maximum count frequency	Waveform 1	$\overline{CP_0}$	30		MHz
			$\overline{CP_1}$	15		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP_0}$ to Q_0	Waveform 1			15 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP_1}$ to Q_1	Waveform 1			19 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP_1}$ to Q_2	Waveform 1			51 63	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP_1}$ to Q_3	Waveform 1			78 95	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2			27 44	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to output	Waveform 3			39 45	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 4			51	ns

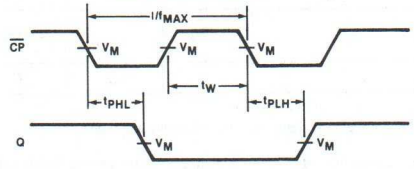
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		54LS/74LS		UNIT
				Min	Max	
t_W	Clock pulse width	Waveform 1	$\overline{CP}_0$	20		ns
			$\overline{CP}_1$	30		ns
t_W	$\overline{MR}$ pulse width	Waveform 4		15		ns
t_W	$\overline{PL}$ pulse width	Waveform 3		20		ns
$t_s(H)$	Setup time HIGH Data to $\overline{PL}$	Waveform 5		10		ns
$t_h(H)$	Hold time HIGH Data to $\overline{PL}$	Waveform 5		20		ns
$t_S(L)$	Setup time LOW Data to $\overline{PL}$	Waveform 5		15		ns
$t_h(L)$	Hold time LOW Data to $\overline{PL}$	Waveform 5		20		ns
t_{rec}	Recovery time $\overline{MR}$ to $\overline{CP}$	Waveform 4		30		ns
t_{rec}	Recovery time $\overline{PL}$ to $\overline{CP}$	Waveform 3		30		ns

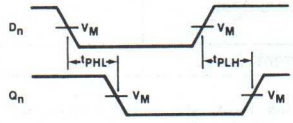
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



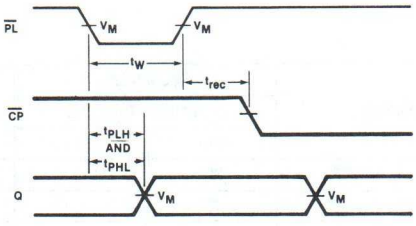
Waveform 1

PARALLEL DATA TO OUTPUT DELAYS



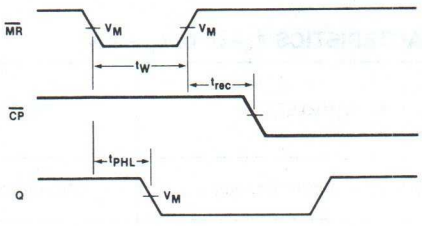
Waveform 2

PARALLEL LOAD PULSE WIDTH, PARALLEL LOAD TO OUTPUT DELAY AND PARALLEL LOAD TO CLOCK RECOVERY TIME



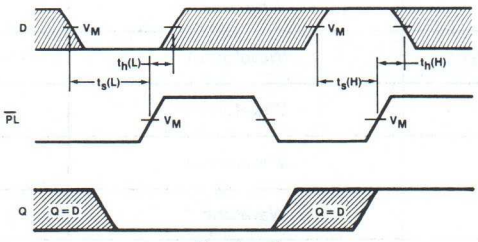
Waveform 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 4

DATA SETUP AND HOLD TIMES

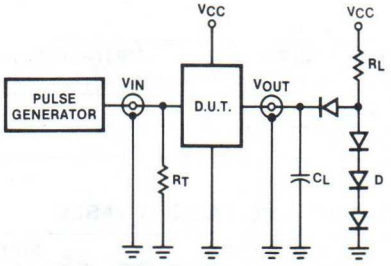


Waveform 5

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

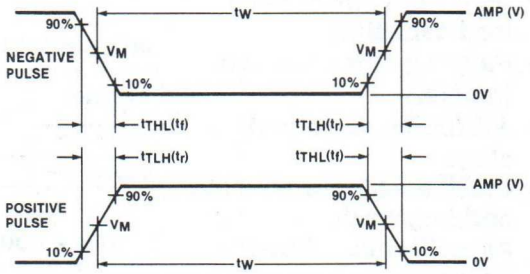
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

SHIFT REGISTER 54/74199

8-Bit Parallel-Access Shift Register

- **Buffered clock and control inputs**
- **Shift right and parallel load capability**
- **Fully synchronous data transfers**
- **J-$\overline{K}$ (D) inputs to first stage**
- **Clock enable for hold (do nothing) mode**
- **Asynchronous Master Reset**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT
74199	35MHz	90mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC}=5V \pm 5\%; T_A=0°C$ to $+70°C$	MILITARY RANGES $V_{CC}=5V \pm 10\%; T_A=-55°C$ to $+125°C$
Plastic DIP	N74199N	
Ceramic DIP	N74199F	

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
All	Inputs	1ul
Q_0-Q_7	Parallel outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} AND −1.6mA I_{IL}.

DESCRIPTION

The functional characteristics of the '199 8-Bit Parallel-Access Shift Register are indicated in the Logic Diagram and Function Table. The device is useful in a wide variety of shifting, counting and storage applications. It performs serial, parallel, serial to parallel, or parallel to serial data transfers at very high speeds.

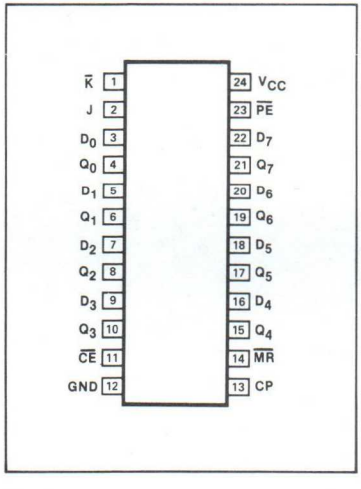
The '199 operates in two primary modes: shift right ($Q_0 \rightarrow Q_1$) and parallel load, which are controlled by the state of the Parallel Enable ($\overline{PE}$) input. Serial data enters the first flip-flop (Q_0) via the J and $\overline{K}$ inputs when the $\overline{PE}$ input is HIGH, and is shifted one bit in the direction $Q_0 \rightarrow Q_1 \rightarrow Q_3$ following each LOW-to-HIGH clock transition. The J and $\overline{K}$ inputs provide the flexibility of the J-K type input for special applications and, by tying the two pins together, the simple D-type input for general applications. The device appears as eight common clocked D flip-flops when the $\overline{PE}$ input is LOW. After the LOW-to-HIGH clock transition, data on the parallel inputs (D_0-D_7) is transferred to the respective Q_0-Q_7 outputs.

All parallel and serial data transfers are synchronous, occuring after each LOW-to-HIGH clock transition. The '199 utilizes edge-triggering, therefore, there is no restriction on the activity of the J, $\overline{K}$, D_n, and $\overline{PE}$ inputs for logic operation, other than the setup and release time requirements.

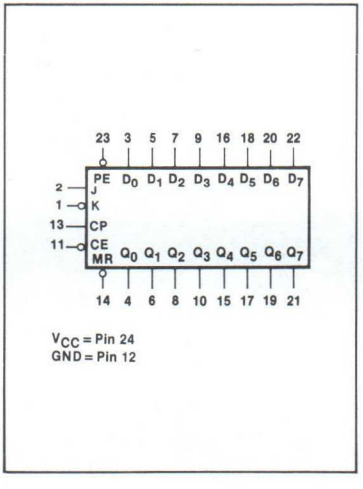
The clock input is a gated OR structure which allows one input to be used as an active-LOW Clock Enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of $\overline{CE}$ input should only take place while the CP is HIGH for conventional operation.

A LOW on the Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all bit positions to a LOW state.

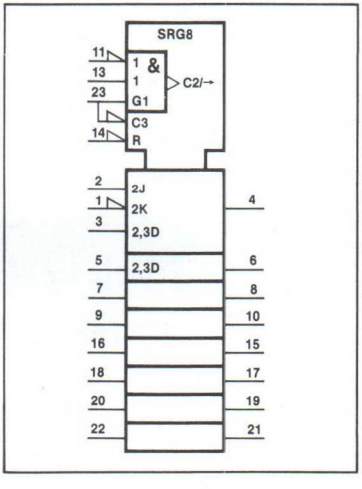
PIN CONFIGURATION



LOGIC SYMBOL

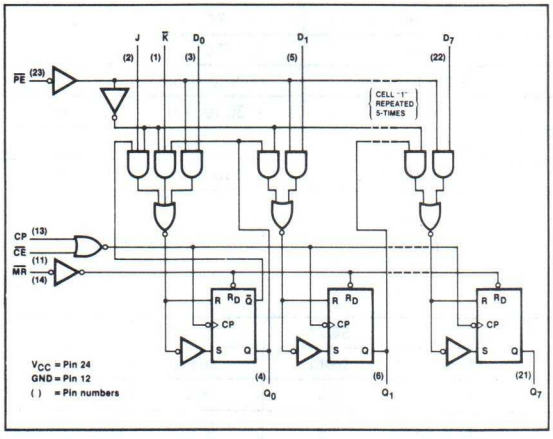


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/74199

LOGIC DIAGRAM



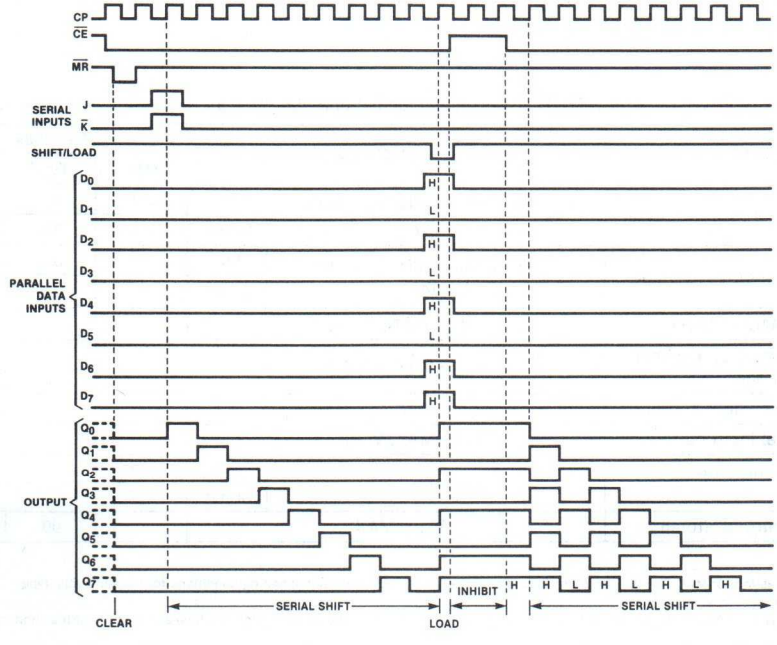
MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS							OUTPUTS
	$\overline{MR}$	CP	$\overline{CE}$	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0 Q_1 ••• Q_6 Q_7
Reset (clear)	L	X	X	X	X	X	X	L L ••• L L
Shift, Set First Stage	H	↑	l	h	h	h	X	H q_0 ••• q_5 q_6
Shift, Reset First Stage	H	↑	l	h	l	l	X	L q_0 ••• q_5 q_6
Shift, Toggle First Stage	H	↑	l	h	h	l	X	$\overline{q}_0$ q_0 ••• q_5 q_6
Shift, Retain First Stage	H	↑	l	h	l	h	X	q_0 q_0 ••• q_5 q_6
Parallel Load	H	↑	l	l	X	X	d_n	d_0 d_1 ••• d_6 d_7
Hold (do nothing)	H	↑	h[a]	X	X	X	X	q_0 q_1 ••• q_6 q_7

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
d_n(q_n) = Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH clock transition.
↑ = LOW-to-HIGH clock transition.

NOTE
a. The LOW-to-HIGH transition of $\overline{CE}$ should only occur while CP is HIGH for conventional operation.

TYPICAL CLEAR, LOAD, RIGHT-SHIFT, LEFT-SHIFT, INHIBIT AND CLEAR SEQUENCES



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74199			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	−20		−57	mA
			Com'l	−18		−57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			90	127	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with $\overline{R}$, J and D inputs at 4.5V, momentary ground clock, then apply 4.5V, ground $\overline{CE}$, $\overline{MR}$ and $\overline{PE}$.

SHIFT REGISTER 54/74199

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74 $C_L = 15pF$, $R_L = 400\Omega$		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		26 30	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 2		35	ns

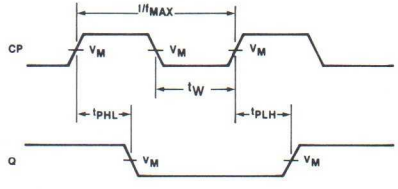
Per industry convention, f_{MAX} is the worst case of the maximum device operating frequency with no constraints on t_f, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_W	$\overline{MR}$ pulse width	Waveform 2	20		ns
t_s	Setup time, J, $\overline{K}$ and Data to clock	Waveform 3	20		ns
t_h	Hold time, J, $\overline{K}$ and Data to clock	Waveform 3	0		ns
t_s	Setup time, $\overline{CE}$ to clock	Waveform 3	30		ns
t_h	Hold time, $\overline{CE}$ to clock	Waveform 3	0		ns
t_s	Setup time, $\overline{PE}$ to clock	Waveform 3	30		ns
t_h	Hold time, $\overline{PE}$ to clock	Waveform 3	0		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	30		ns

AC WAVEFORMS

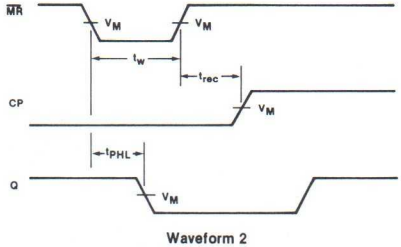
CLOCK TO OUTPUT DELAYS & CLOCK PULSE WIDTH



The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

Waveform 1

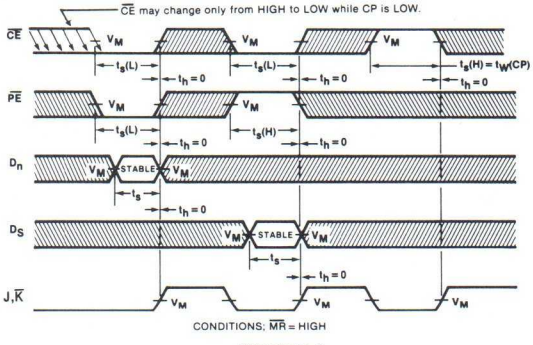
MASTER RESET PULSE WIDTH MASTER RESET TO OUTPUT DELAY & MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.

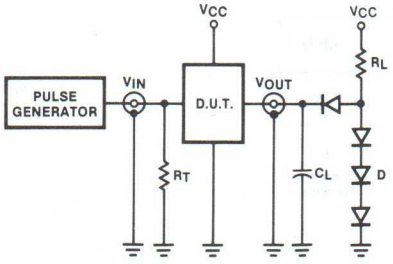
The shaded areas indicate when the input is permitted to change for predictable performances.



Waveform 3

TEST CIRCUITS AND WAVEFORMS

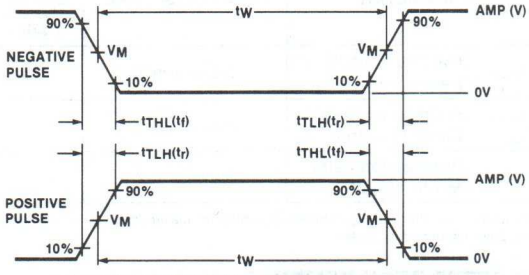
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

MULTIVIBRATOR 54/74221

Dual Monostable Multivibrator

- **Pulse width variance is typically less than ±0.5% for 98% of the units**
- **The '221 demonstrates electrical and switching characteristics that are virtually identical to the '121 one-shots**
- **Pin-out is identical to the '123**
- **Overriding Reset terminates output pulse**
- **B input has hysteresis for improved noise immunity**
- **Maximum pulse width: 54221: 21 seconds 74221: 28 seconds**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74221	42ns	36mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74221N	
Ceramic DIP	N74221F	S54221F
Flatpack		S54221W

3

FUNCTION TABLE

(Each monostable)

INPUTS			OUTPUTS	
$\overline{R}_D$	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

In addition, see description and switching characteristics.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
↑ = LOW-to-HIGH transition
↓ = HIGH-to-LOW transition
⎍ = One HIGH-level pulse
⎎ = One LOW-level pulse

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74
$\overline{A}$	Input	1ul
B, $\overline{R}_D$	Inputs	2ul
All	Outputs	10ul

NOTE
A 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}.

DESCRIPTION

The '221 is a dual monostable multivibrator with performance characteristics virtually identical to those of the '121. Each multivibrator features an active LOW going edge input ($\overline{A}$) and an active HIGH going edge input (B), either of which can be used as an Enable input.

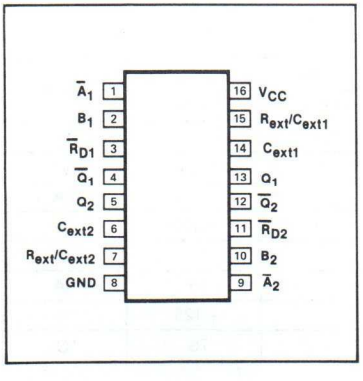
Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the $\overline{A}$ and B inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW Reset ($\overline{R}_D$). Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 35 nanoseconds to the maximums shown in the FEATURES by choosing appropriate timing components. With R_{ext} = 2kΩ and C_{ext} = 0, an output pulse of typically 30 nanoseconds is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

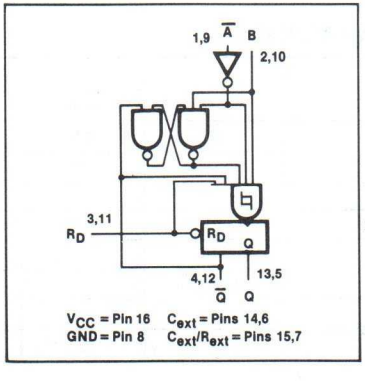
Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In

(Continued)

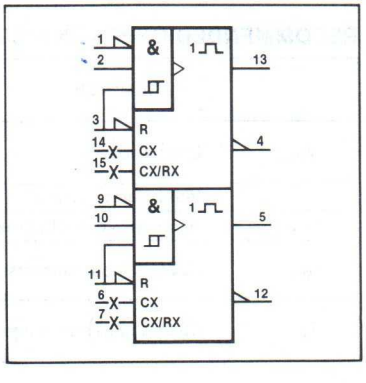
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



MULTIVIBRATOR 54/74221

DESCRIPTION (Continued)

most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10pF to 10μF) and more than one decade of timing resistance (2kΩ to 30kΩ for the 54221 and 2kΩ to 40kΩ for the 74221). Throughout these ranges, pulse width is defined by the following relationship: (see Figure A)

$$t_W(out) = C_{ext} R_{ext} \ln 2$$
$$t_W(out) \cong 0.7 C_{ext} R_{ext}$$

In circuits where pulse cutoff is not critical, timing capacitance up to 1000μF and timing resistance as low as 1.4kΩ may be used.

Pin assignments for these devices are identical to those of the '123 so that the '221 can be substituted for those products in systems not using the retrigger by merely changing the value of R_{ext} and/or C_{ext}.

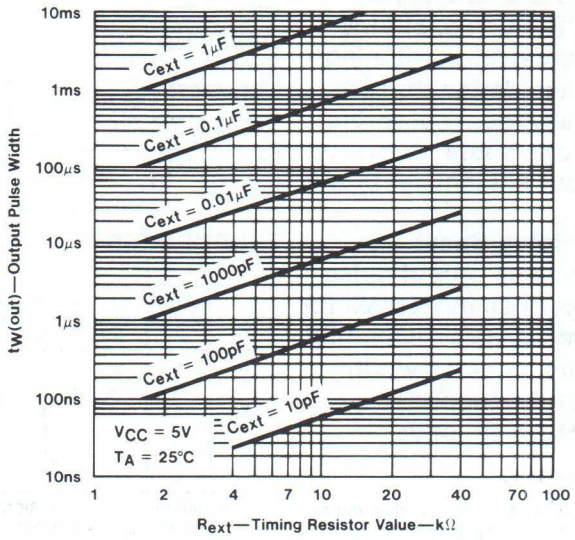


Figure A

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	µA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74221 Min	54/74221 Typ[2]	54/74221 Max	UNIT
V_{T+}	Positive-going threshold at $\overline{A}$ and B	V_{CC} = MIN				2.0	V
V_{T-}	Negative-going threshold at $\overline{A}$ and B	V_{CC} = MIN		0.8			V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V	$\overline{A}$ input			40	μA
			B, $\overline{R}_D$ inputs			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{A}$ input			– 1.6	mA
			B, $\overline{R}_D$ inputs			– 3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	– 20		– 55	mA
			Com'l	– 18		– 55	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	Quiescent		26	50	mA
			Triggered		46	80	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

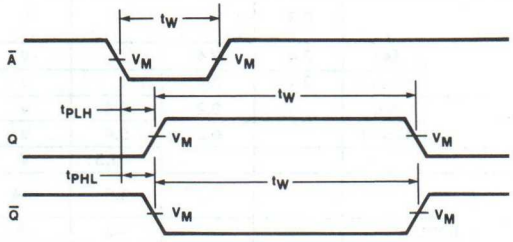
PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay $\overline{A}$ input to Q & $\overline{Q}$ output	Waveform 1 C_{ext} = 80pF, R_{ext} = 2kΩ		70 80	ns ns
t_{PLH} t_{PHL}	Propagation delay B input to Q & $\overline{Q}$ output	Waveform 2 C_{ext} = 80pF, R_{ext} = 2kΩ		55 65	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{R}_D$ input to Q & $\overline{Q}$ output	Waveform 3 C_{ext} = 80pF, R_{ext} = 2kΩ		40 27	ns ns
t_W	Minimum output pulse width	C_{ext} = 0pF, R_{ext} = 2kΩ	20	50	ns
t_W	Output pulse width	C_{ext} = 80pF, R_{ext} = 2kΩ	70	150	ns
		C_{ext} = 100pF, R_{ext} = 10kΩ	650	750	ns
		C_{ext} = 1μF, R_{ext} = 10kΩ	6.5	7.5	ms

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54/74 Min	54/74 Max	UNIT
t_W	Minimum input pulse width to trigger	Waveforms 1 & 2		50		ns
t_W	Minimum Reset pulse width	Waveform 3		20		ns
t_{rec}	Recovery time from Reset to trigger input	Waveform 3		15		ns
R_{ext}	External timing resistor range		Mil	1.4	30	kΩ
			Com'l	1.4	40	kΩ
C_{ext}	External timing capacitance range			0	1000	μF
	Output duty cycle	R_{ext} = 2kΩ			67	%
		R_{ext} = R_{ext}(MAX)			90	%

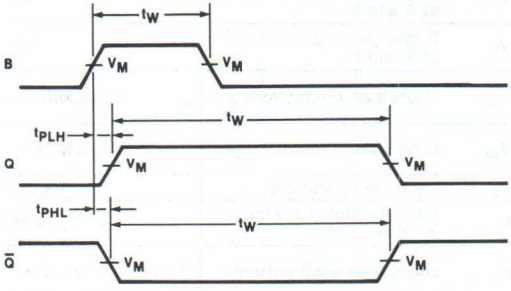
AC WAVEFORMS

PROPAGATION DELAY $\overline{A}$ INPUT TO Q AND $\overline{Q}$ OUTPUTS, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 1

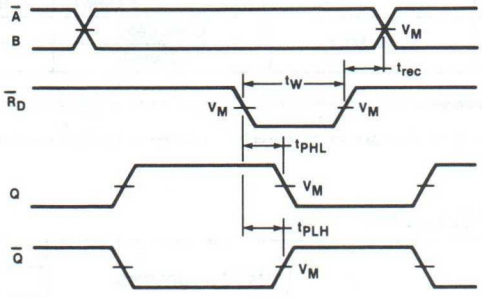
PROPAGATION DELAY B INPUT TO Q AND $\overline{Q}$ OUTPUT, AND INPUT AND OUTPUT PULSE WIDTHS



Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

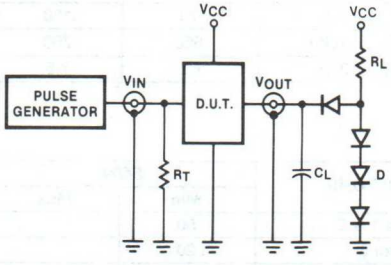
DIRECT RESET DELAYS AND RECOVERY TIME



Waveform 3

TEST CIRCUITS AND WAVEFORMS

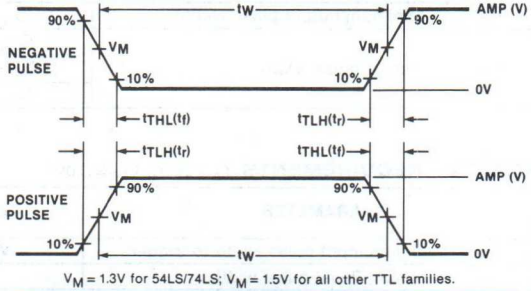
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

'240 Octal Inverter Buffer (3-State)
'241 Octal Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS240	11ns	24mA
74S240	4.5ns	93mA
74LS241	12ns	25mA
74S241	6ns	112mA

FUNCTION TABLE, '240

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	$\overline{Y}_a$	$\overline{Y}_b$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	(Z)	(Z)

FUNCTION TABLE, '241

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	OE_b	I_b	Y_a	Y_b
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ORDERING CODE

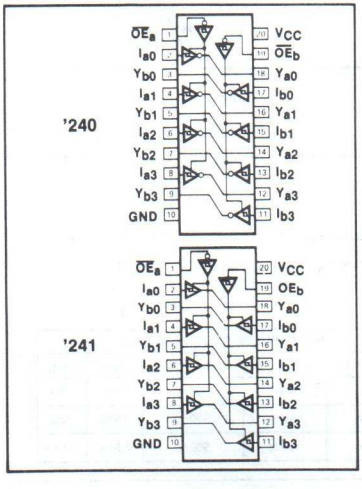
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74LS240N • N74S240N N74LS241N • N74S241N	
Ceramic DIP	N74LS240F • N74S240F N74LS241F • N74S241F	S54LS240F • S54S240F S54LS241F • S54S241F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

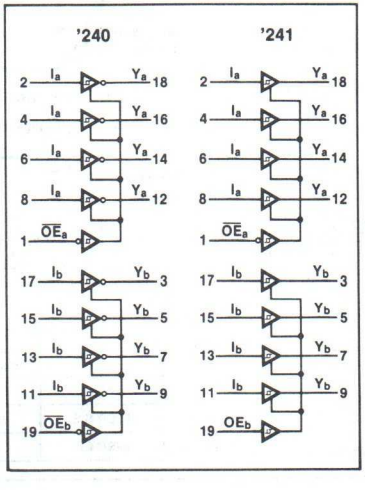
PINS	DESCRIPTION	54/74S	54/74LS
I_{a0}–I_{a3}, I_{b0}–I_{b3}	Inputs	1Sul	1LSul
$\overline{OE}_a$, $\overline{OE}_b$, OE_b	Inputs	1Sul	1LSul
All	Outputs	24Sul	32LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

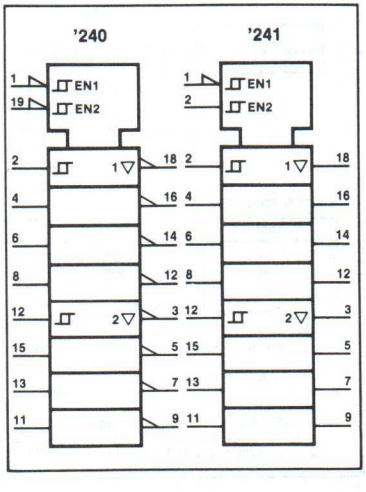
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

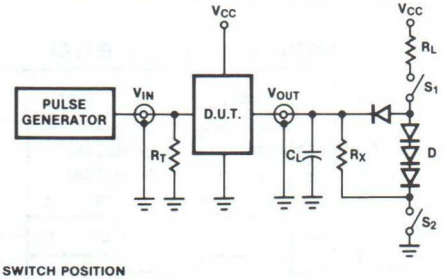
PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−12			−12	mA
		Com'l			−15			−15	mA
I_{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C
External resistance between any input or V_{CC} and ground								40	kΩ

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



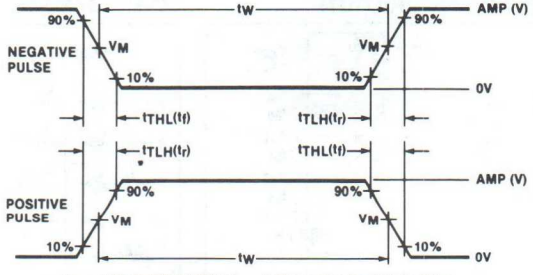
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]				54/74LS240, 241			54/74S240, 241			UNIT
						Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN				0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX				2.0			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = −3mA			2.4	3.4		2.4	3.4		V
			I_{OH} = −1mA	74S					2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil				0.4			0.55	V
				Com'l				0.5			0.55	V
			I_{OL} = 12mA	74LS				0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}						−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 2.4V								50	μA
			V_O = 2.7V					20				μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 0.4V					−20				μA
			V_O = 0.5V								−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V								1.0	mA
			V_I = 7.0V					0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V						20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V					−0.2				mA
			V_I = 0.5V	I_{a0}–I_{a3}, I_{b0}–I_{b3} inputs							−400	μA
				$\overline{OE}_a$, $\overline{OE}_b$, OE_b inputs							−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX				−40		−130	−50		−225	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	'LS240	Mil & Com'l		17	27				mA
			I_{CCL}				26	44				mA
			I_{CCZ}				29	50				mA
			I_{CCH}	'LS241	Mil & Com'l		17	27				mA
			I_{CCL}				27	46				mA
			I_{CCZ}				32	54				mA
			I_{CCH}	'S240	Mil					80	123	mA
					Com'l					80	135	mA
			I_{CCL}		Mil					100	145	mA
					Com'l					100	150	mA
			I_{CCZ}		Mil					100	145	mA
					Com'l					100	150	mA
			I_{CCH}	'S241	Mil					95	147	mA
					Com'l					95	160	mA
			I_{CCL}		Mil					120	170	mA
					Com'l					120	180	mA
			I_{CCZ}		Mil					120	170	mA
					Com'l					120	180	mA

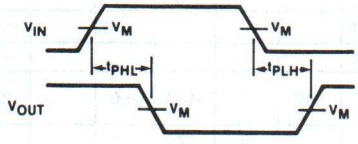
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS		54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$		54S/74S $C_L = 50pF$, $R_L = 90\Omega$		UNIT
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '240			14 18		7 7	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '241			18 18		9 9	ns
t_{PZH}	Enable to HIGH	Waveform 3	LS		23			ns
			'S240				10	ns
			'S241				12	ns
t_{PZL}	Enable to LOW	Waveform 4			30		15	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5pF$			18		9	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5pF$			25		15	ns

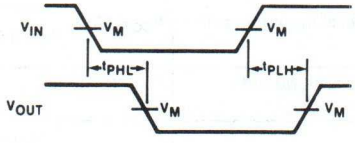
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



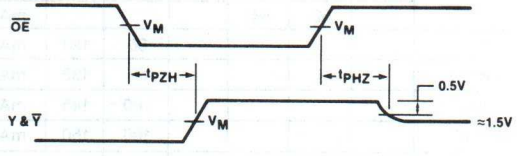
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



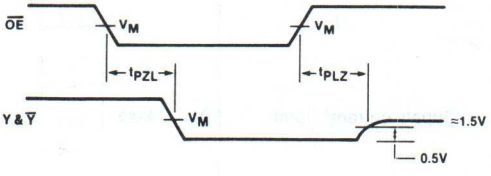
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

$V_M = 1.3V$ for 54LS/74LS. $V_M = 1.5V$ for all other TTL families.

'242 Quad Inverting Transceiver (3-State)
'243 Quad Transceiver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURENT (Total)
74LS242	10ns	27mA
74LS243	12ns	28mA

FUNCTION TABLE, '242

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	$B = \overline{A}$
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	$A = \overline{B}$	INPUT

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS242N • N74LS243N	
Ceramic DIP	N74LS242F • N74LS243F	S54LS242F • S54LS243F
Flatpack		S54LS242W • S54LS243W

FUNCTION TABLE, '243

INPUTS		INPUT/OUTPUT	
$\overline{OE}_A$	OE_B	A_n	B_n
L	L	INPUT	B = A
H	L	(Z)	(Z)
L	H	(a)	(a)
H	H	A = B	INPUT

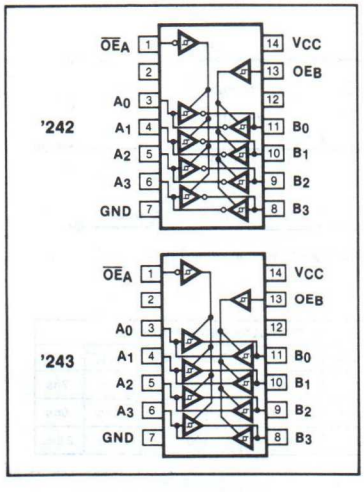
H = HIGH voltage level
L = LOW voltage level
(Z) = HIGH impedance (off) state
(a) = This condition is not allowed due to excessive currents.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

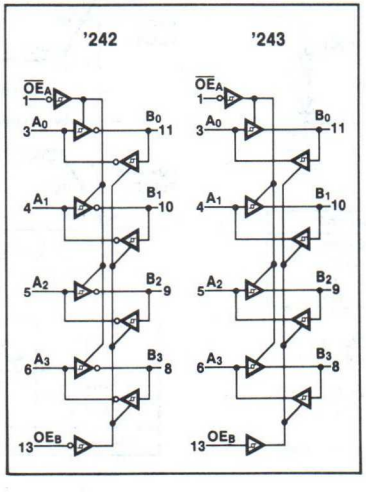
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
A, B	Outputs	30LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

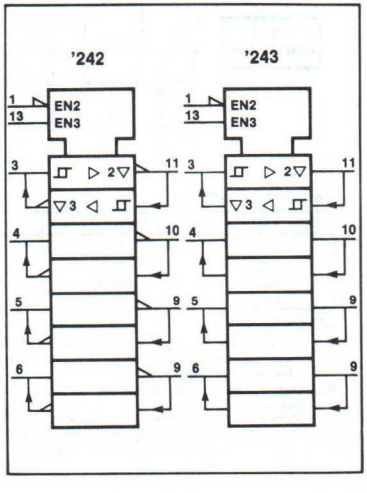
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

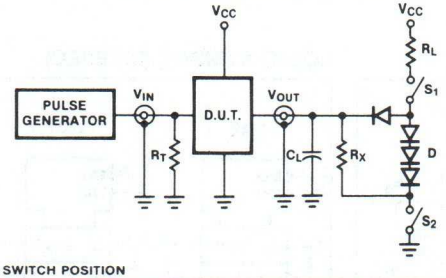
NOTE
V_{IN} limited to +5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

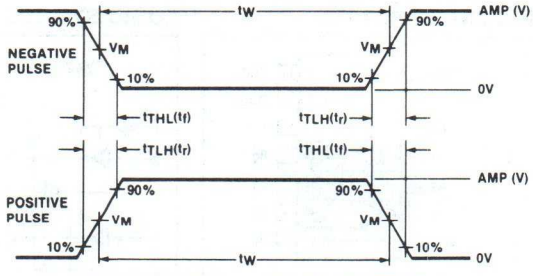


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS242 54/74LS243			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.7V					40	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	$\overline{OE}_A$, OE_B inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	A inputs $\overline{OE}_A$, OE_B = V_{IL} = MAX				−0.2	mA
			B inputs $\overline{OE}_A$, OE_B = V_{IH} = MIN				−0.2	mA
			$\overline{OE}_A$, OE_B inputs				−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH '242		22	38	mA
			I_{CCL}	Outputs LOW '242		29	50	mA
			I_{CCZ}	Outputs OFF '242		29	50	mA
			I_{CCH}	Outputs HIGH '243		22	38	mA
			I_{CCL}	Outputs LOW '243		29	50	mA
			I_{CCZ}	Outputs OFF '243		32	54	mA

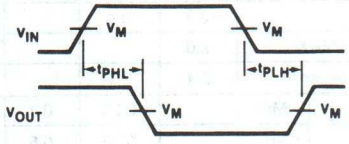
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open and transceivers enabled in one direction only, or with all transceivers disabled.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS242 C_L = 45pF, R_L = 667Ω		54/74LS243 C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1		14 18			ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2				18 18	ns
t_{PZH}	Enable to HIGH	Waveform 3		23		23	ns
t_{PZL}	Enable to LOW	Waveform 4		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 3, C_L = 5pF		18		18	ns
t_{PLZ}	Disable from LOW	Waveform 4, C_L = 5pF		25		25	ns

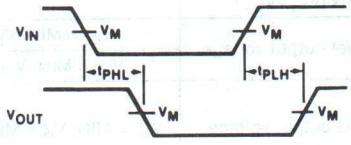
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

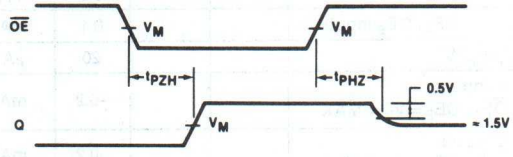
WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

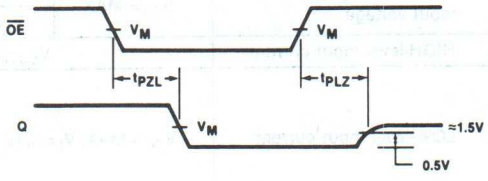
V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

Octal Buffers (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS244	12ns	25mA
74S244	6ns	112mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS244N • N74S244N	
Ceramic DIP	74LS244F • N74S244F	S54LS244F • S54S244F

FUNCTION TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

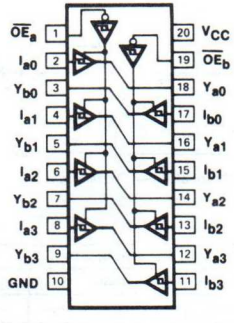
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

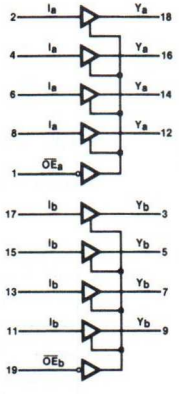
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	24Sul	30LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

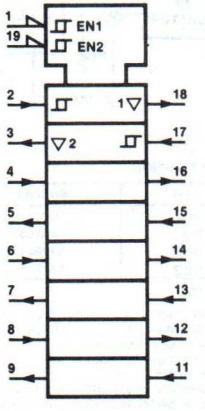
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

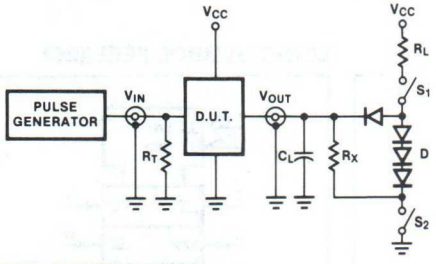
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−12			−12	mA
		Com'l			−15			−15	mA
I_{OL}	LOW-level output current	Mil			12			48	mA
		Com'l			24			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

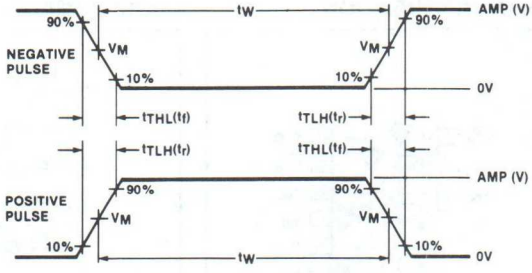


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS244			54/74S244			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.4		2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4			0.55	V
				Com'l			0.5			0.55	V
			I_{OL} = 12mA	74LS			0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX	V_O = 0.4V				−20				μA
			V_O = 0.5V							−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				−0.2				mA
			V_I = 0.5V	$\overline{OE}$ inputs						−2.0	mA
				Other inputs						−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	−50		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH} Outputs HIGH	Mil		17	27		95	147	mA
				Com'l		17	27		95	160	mA
			I_{CCL} Outputs LOW	Mil		27	46		120	170	mA
				Com'l		27	46		120	180	mA
			I_{CCZ} Outputs OFF	Mil		32	54		120	170	mA
				Com'l		32	54		120	180	mA

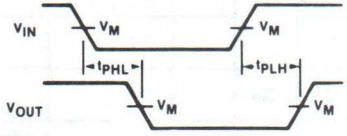
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 50pF, R_L = 90Ω		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		18		9	ns
t_{PHL}	Propagation delay	Waveform 1		18		9	ns
t_{PZH}	Enable to HIGH	Waveform 2		23		12	ns
t_{PZL}	Enable to LOW	Waveform 3		30		15	ns
t_{PHZ}	Disable from HIGH	Waveform 2, C_L = 5pF		18		9	ns
t_{PLZ}	Disable from LOW	Waveform 3, C_L = 5pF		25		15	ns

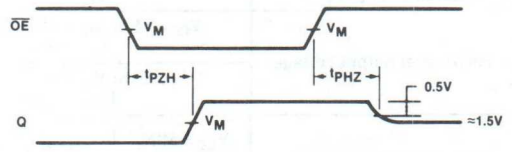
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



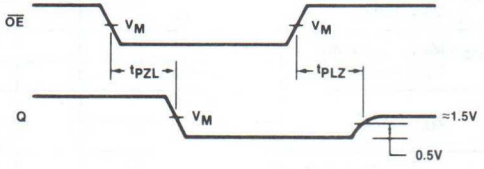
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

TRANSCEIVER 54/74LS245

Octal Transceiver (3-State)

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS245	8ns	58mA

DESCRIPTION

The 'LS245 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable (CE) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS245N	
Ceramic DIP	N74LS245F	S54LS245F

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUT	B = A
H	X	(Z)	(Z)

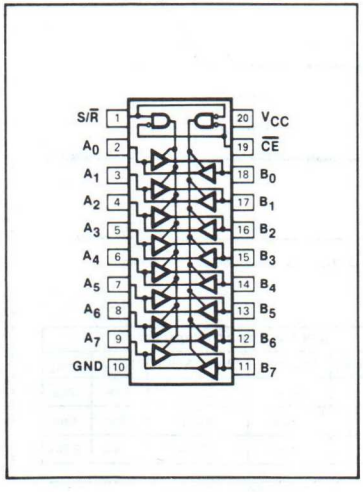
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

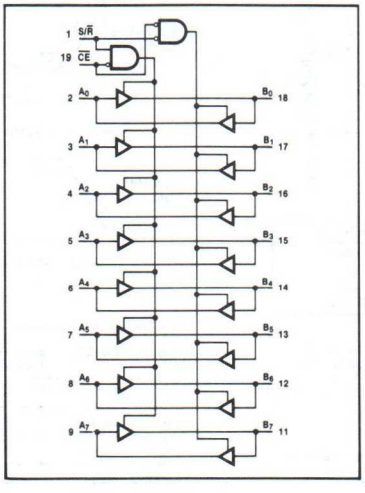
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

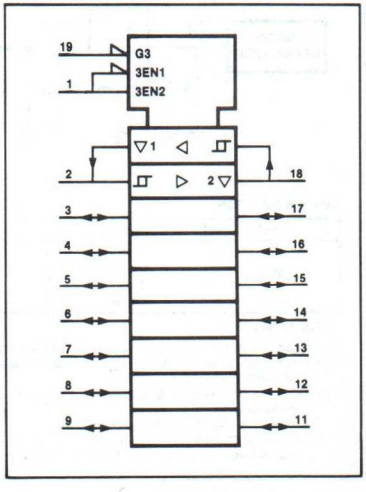
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER 54/74LS245

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

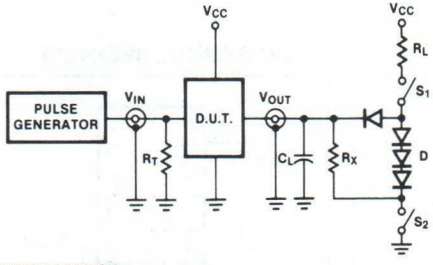
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

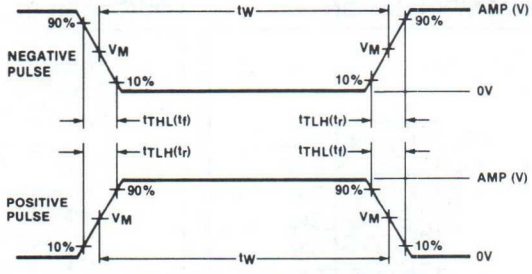


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

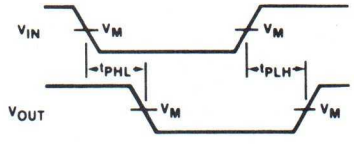
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS245			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			V
			I_{OH} = −3mA		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4	V
				Com'l			0.5	V
			I_{OL} = 12mA	74LS			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V, $\overline{CE}$ = 2.0V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V, $\overline{CE}$ = 2.0V					−200	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A, B inputs			0.1	mA
			V_I = 7.0V	S/$\overline{R}$, $\overline{CE}$ inputs			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70	mA
			I_{CCL}	Outputs LOW		62	90	mA
			I_{CCZ}	Outputs OFF		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

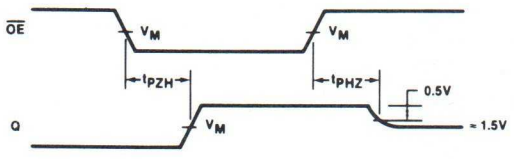
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

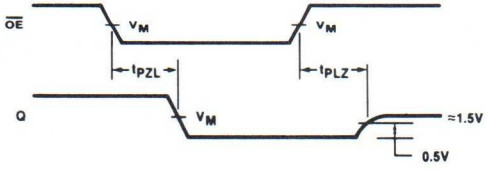
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS. V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12	ns
t_{PHL}	Propagation delay	Waveform 1		12	ns
t_{PZH}	Enable to HIGH	Waveform 2		40	ns
t_{PZL}	Enable to LOW	Waveform 3		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, $C_L = 5pF$		25	ns

MULTIPLEXERS 54/74LS251A, S251

8-Input Multiplexer (3-State)

- **High speed 8-to-1 multiplexing**
- **True and complement outputs**
- **Both outputs are 3-State for further multiplexer expansion**
- **3-State outputs are buffer type with 12mA/24mA outputs for Military/ Commercial applications**

TYPE	TYPICAL PROPAGATION DELAY (Data to Y)	TYPICAL SUPPLY CURRENT (Total)
74LS251A	18ns	9mA
74S251	8ns	55mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S251N • N74LS251AN	
Ceramic DIP	N74S251F • N74LS251AF	S54S251F • S54LS251AF
Flatpack		S54S251W • S54LS251AW

3

DESCRIPTION

The '251 is a logical implementation of a single-pole, 8-position switch with the state of three Select inputs (S_0, S_1, S_2) controlling the switch position. Assertion (Y) and Negation ($\overline{Y}$) outputs are both provided. The Output Enable input ($\overline{OE}$) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \overline{OE} \cdot (I_0 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_1 \cdot S_0 \cdot \overline{S}_1 \cdot \overline{S}_2 + I_2 \cdot \overline{S}_0 \cdot S_1 \cdot \overline{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \overline{S}_2 + I_4 \cdot \overline{S}_0 \cdot \overline{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \overline{S}_1 \cdot S_2 + I_6 \cdot \overline{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2).$$

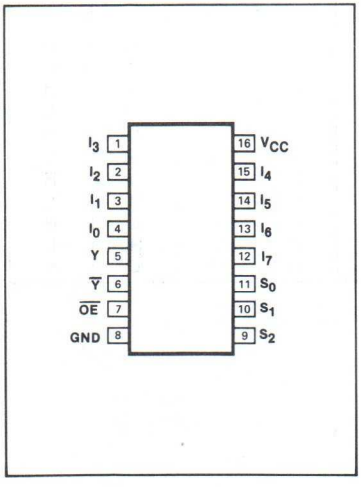
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

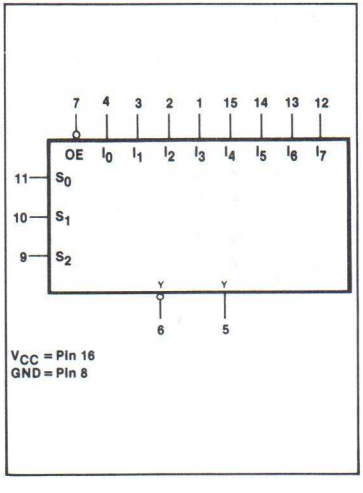
NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

Both outputs are in the HIGH impedance (HIGH Z) state when the output enable is HIGH, allowing multiplexer expansion by tying the outputs of up to 128 devices together. All but one device must be in the HIGH impedance state to avoid high currents that would exceed the maximum ratings, when the outputs of the 3-State devices are tied together. Design of the output enable signals must ensure there is no overlap in the active LOW portion of the enable voltages.

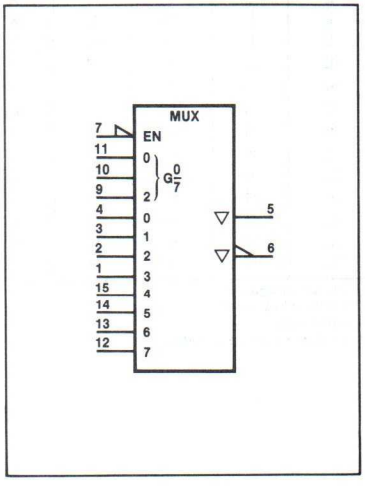
PIN CONFIGURATION



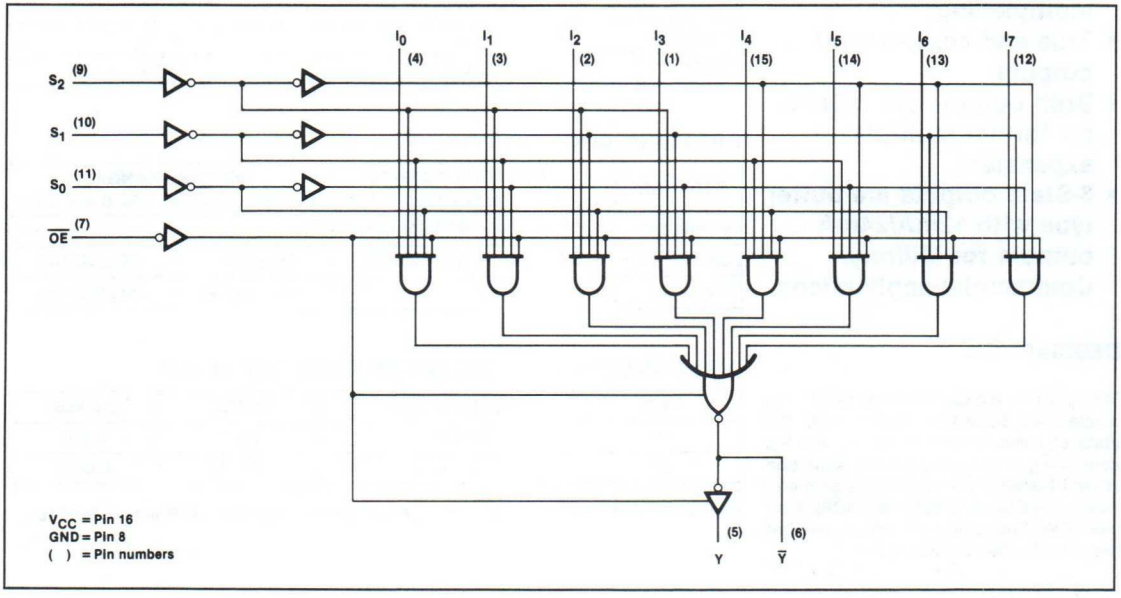
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS												OUTPUTS	
$\overline{OE}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	(Z)	(Z)
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output for HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

3

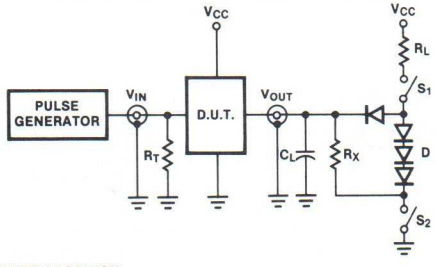
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



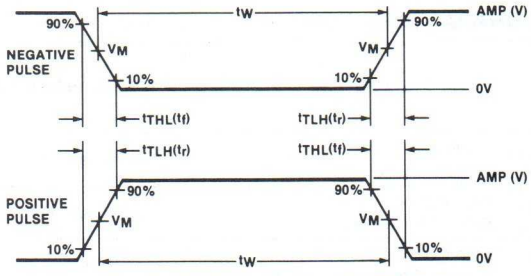
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS251A			54/74S251			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5			2.4	3.4		V
				Com'l	2.7			2.4	3.2		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.4V							50	μA
			V_O = 2.7V				20				μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				-20				μA
			V_O = 0.5V							-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V				20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				-0.4				mA
			V_I = 0.5V							-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-30		-130	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Outputs "on"				12				mA
			Outputs "off"				15			85	mA

NOTES

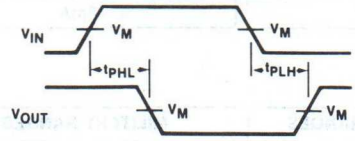
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} on the 54/74S251 with all inputs at 4.5V and all outputs open. Measure I_{CC} on the 54/74LS251A in the following manner: 1. *Outputs "on"*: Data and select inputs at 4.5V, output enable grounded and all outputs open. 2. *Outputs "off"*: Data and select inputs at 4.5V, output enable at 4.5V and all outputs open.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 45pF, R_L = 667Ω		54S/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Select to Y output	Waveform 2		35 40		18 19.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to $\overline{Y}$ output	Waveform 1		28 33		15 13.5	ns
t_{PLH} t_{PHL}	Propagation delay Data to Y output	Waveform 2		28 28		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Y}$ output	Waveform 1		15 15		7.0 7.0	ns
t_{PZH}	Output enable to HIGH level	Waveform 3 C_L = 50pF for 'S251		25		19.5	ns
t_{PZL}	Output enable to LOW level	Waveform 4 C_L = 50pF for 'S251		25		21	ns
t_{PHZ}	Output disable from HIGH level	Waveform 3, C_L = 5pF		30		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 4, C_L = 5pF		20		14	ns

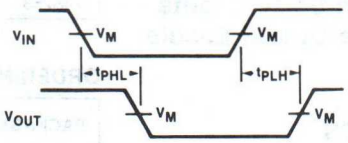
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



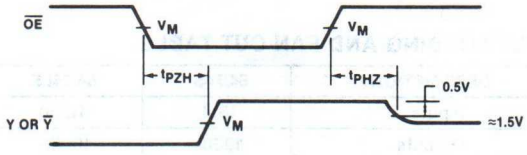
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



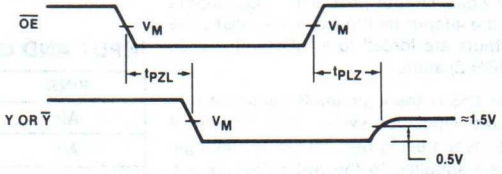
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

3

MULTIPLEXERS 54/74LS253, S253

Dual 4-Input Multiplexer (3-State)

- **3-State outputs for bus interface and multiplex expansion**
- **Common Select inputs**
- **Separate Output Enable inputs**

TYPE	TYPICAL PROPAGATION DELAY (From Data)	TYPICAL SUPPLY CURRENT (Total)
74LS253	15ns	8mA
74S253	8ns	48mA

DESCRIPTION

The '253 has two identical 4-input multiplexers with 3-State outputs which select two bits from four sources selected by common Select inputs (S_0, S_1). When the individual Output Enable ($\overline{E}_{0a}$, $\overline{E}_{0b}$) inputs of the 4-input multiplexers are HIGH, the outputs are forced to a HIGH impedance (HIGH Z) state.

The '253 is the logic implementation of a 2-pole, 4-position switch; the position of the switch being determined by the logic levels supplied to the two Select inputs. Logic equations for the outputs are shown below:

$$Y_a = \overline{OE}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Y_b = \overline{OE}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

All but one device must be in the HIGH impedance state to avoid high currents exceeding the maximum ratings, if the outputs of the 3-State devices are tied together. Design of the Output Enable signals must ensure that there is no overlap.

ORDERING CODE

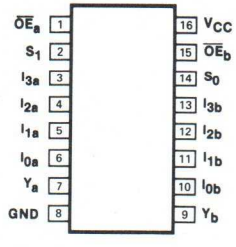
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S253N • N74LS253N	
Ceramic DIP	N74S253F • N74LS253F	S54S253F • S54LS253F
Flatpack		S54S253W • S54LS253W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

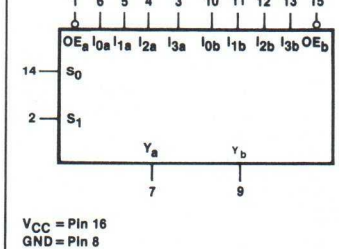
PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1SuI	1LSuI
All	Outputs	10SuI	10LSuI

NOTE
A 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

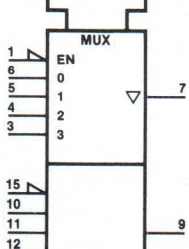
PIN CONFIGURATION



LOGIC SYMBOL

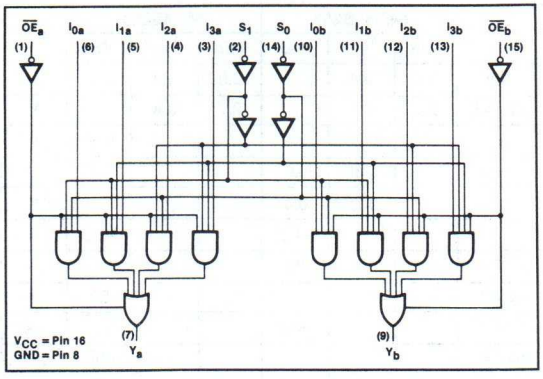


LOGIC SYMBOL (IEEE/IEC)



MULTIPLEXERS 54/74LS253, S253

LOGIC DIAGRAM



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS253			54/74S253			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.1		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				-20				μA
			V_O = 0.5V							-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V				20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				-0.4				mA
			V_I = 0.5V							-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-15		-100	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1			7	12			70	mA
			Condition 2			8.5	14				mA

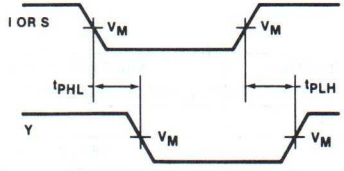
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured under the following conditions with the outputs open: *Condition 1:* All inputs grounded. *Condition 2:* $\overline{OE}$ at 4.5V, all inputs grounded.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ		54S/74S C_L = 15pF, R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		25 20		9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		45 32		18 18	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		28		13	ns
t_{PZL}	Output enable to LOW level	Waveform 3		23		14	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		41		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		27		14	ns

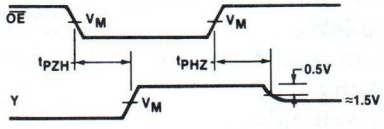
AC WAVEFORMS

PROPAGATION DELAY DATA OR SELECT TO OUTPUT



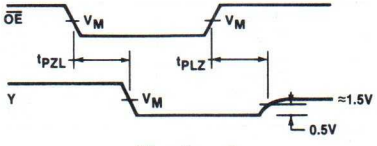
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL

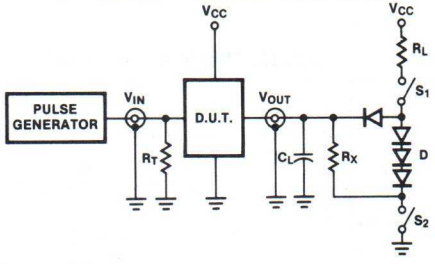


Waveform 3

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for 54/74 and 54/74LS.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



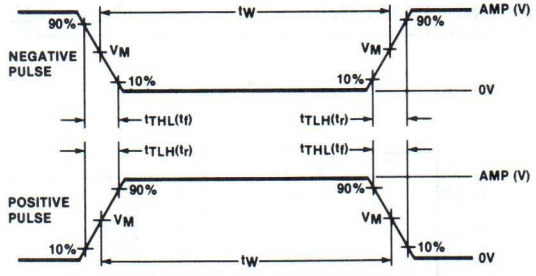
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74LS256

Dual 4-Bit Addressable Latch

- **Combines dual demultiplexer and 8-bit latch**
- **Serial-to-parallel capability**
- **Output from each storage bit available**
- **Random (addressable) data entry**
- **Easily expandable**
- **Common Clear input**
- **Useful as dual 1-of-4 active HIGH decoder**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS256	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS256N	
Ceramic DIP	N74LS256F	S54LS256F
Flatpack		S54LS256W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
$\overline{E}$	Input	2LSul
Other	Inputs	1LSul
All	Outputs	10LSul

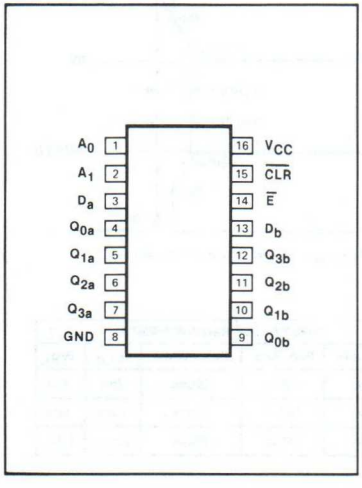
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

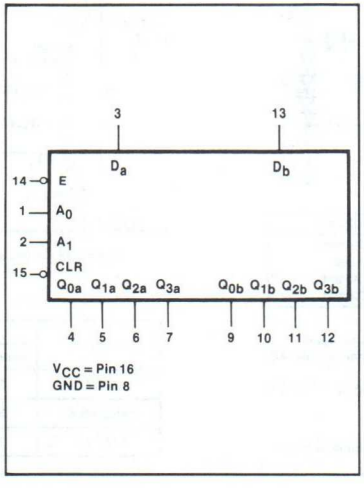
The '256 dual addressable latch has four distinct modes of operation and are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states.

In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibilty of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the dual 1-of-4 decoding or demultiplexing mode ($\overline{CLR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

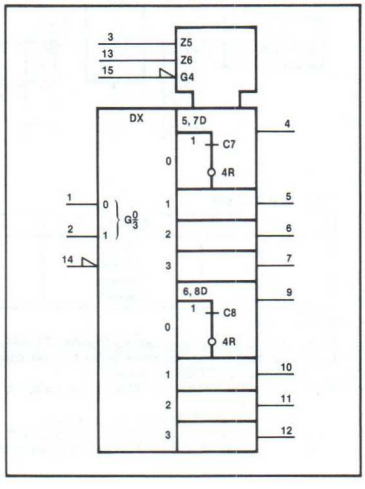
PIN CONFIGURATION



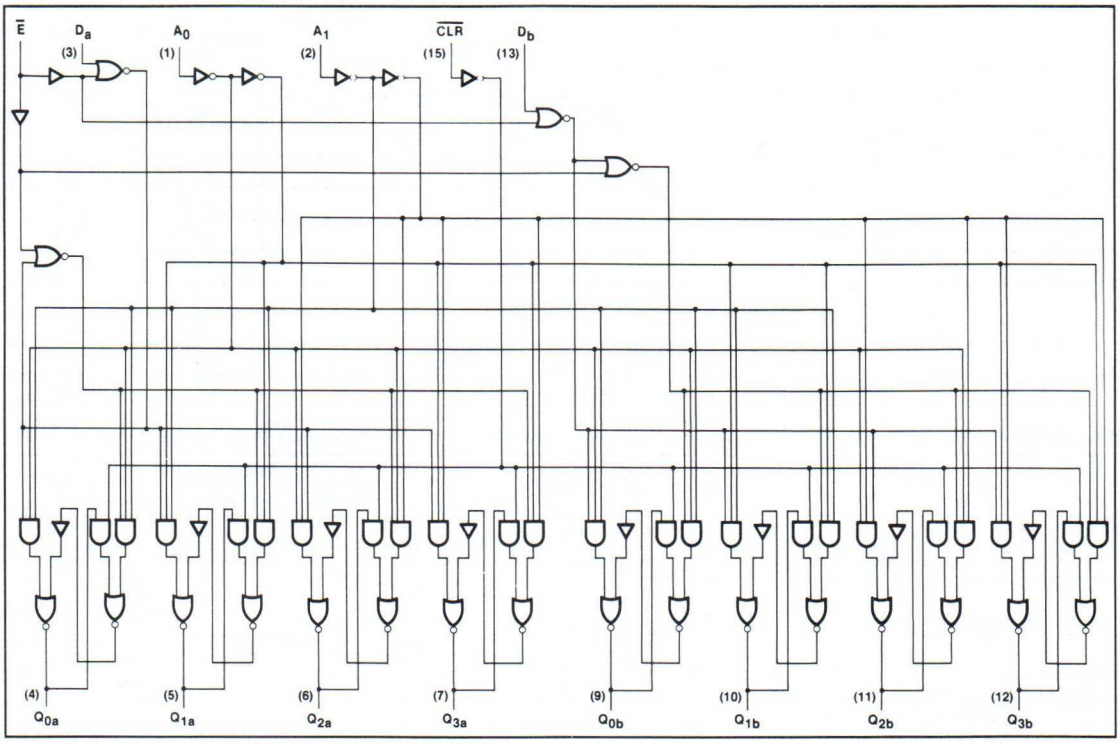
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



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MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS			
	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	Q_0	Q_1	Q_2	Q_3
Clear	L	H	X	X	X	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	Q = d	L	L	L
	L	L	d	H	L	L	Q = d	L	L
	L	L	d	L	H	L	L	Q = d	L
	L	L	d	H	H	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	q_0	q_1	q_2	q_3
Addressable latch	H	L	d	L	L	Q = d	q_1	q_2	q_3
	H	L	d	H	L	q_0	Q = d	q_2	q_3
	H	L	d	L	H	q_0	q_1	Q = d	q_3
	H	L	d	H	H	q_0	q_1	q_2	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output for HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current				– 400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS256			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5			V
				Com'l	2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4	V
				Com'l			0.5	V
			I_{OL} = 4mA	74LS			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	$\overline{E}$ input				40	μA
			Other inputs				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	$\overline{E}$ input				– 0.8	mA
			Other inputs				– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 15		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX				22	36	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3		38 29	ns
t_{PHL}	Propagation delay, Clear to output	Waveform 4		27	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Enable pulse width	Waveform 1	15		ns
t_W	Clear pulse width	Waveform 4	15		ns
$t_s(H)$	Setup time HIGH, Data to Enable	Waveform 5	15		ns
$t_h(H)$	Hold time HIGH, Data to Enable	Waveform 5	0		ns
$t_S(L)$	Setup time LOW, Data to Enable	Waveform 5	15		ns
$t_h(L)$	Hold time LOW, Data to Enable	Waveform 5	0		ns
t_s	Setup time, Address to Enable[a]	Waveform 6	15		ns
t_h	Hold time, Address to Enable[b]	Waveform 6	0		ns

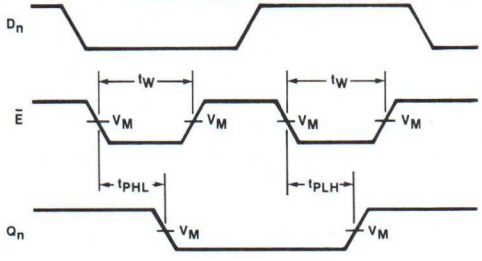
NOTES

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

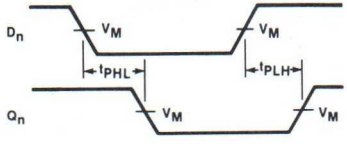
AC WAVEFORMS

PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



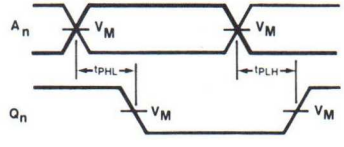
Waveform 1

PROPAGATION DELAY DATA TO OUTPUT



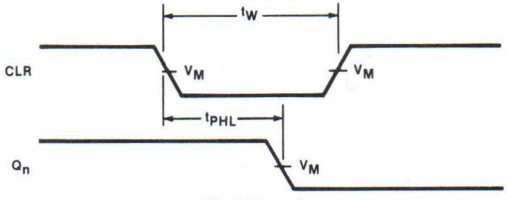
Waveform 2

PROPAGATION DELAY ADDRESS TO OUTPUT



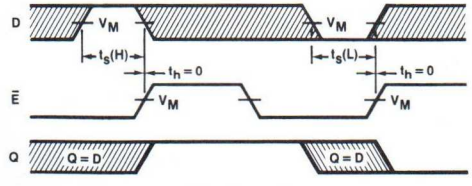
Waveform 3

CLEAR TO OUTPUT DELAY AND CLEAR PULSE WIDTH



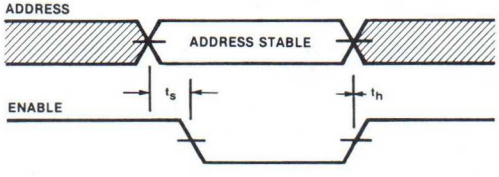
Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

ADDRESS SETUP AND HOLD TIMES



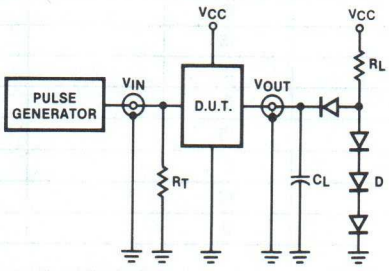
Waveform 6

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

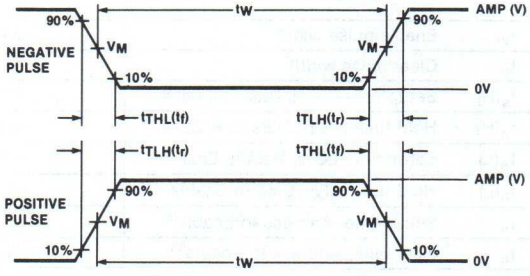
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DATA SELECTORS/MULTIPLEXERS 54/74LS257A, S257

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- **Multifunction capability**
- **Non-inverting data path**
- **3-State outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS257A	13ns	9mA
74S257	6.6ns	56mA

DESCRIPTION

The '257 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in true (non-inverted) form from the selected outputs.

The '257 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs are tied together. Design of the output enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

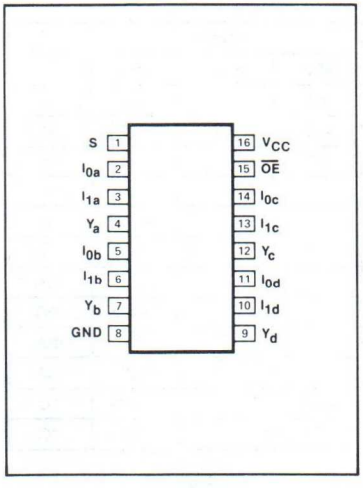
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S257N • N74LS257AN	
Ceramic DIP	N74S257F • N74LS257AF	S54S257F • S54LS257AF
Flatpack		S54S257W • S54LS257AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

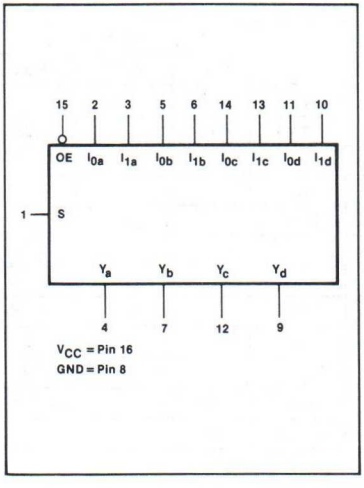
PINS	DESCRIPTION	54/74S	54/74LS
S	Input	2Sul	2LSul
Other	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

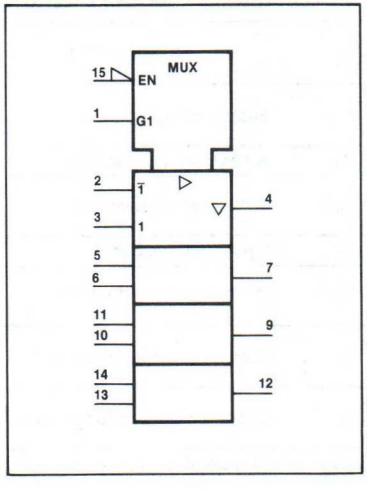
PIN CONFIGURATION



LOGIC SYMBOL

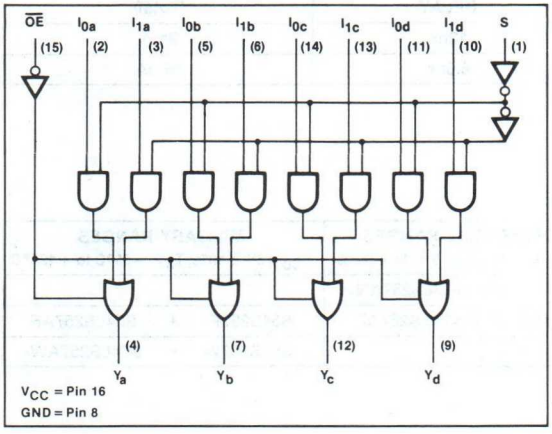


LOGIC SYMBOL (IEEE/IEC)



DATA SELECTORS/MULTIPLEXERS 54/74LS257A, S257

LOGIC DIAGRAM



FUNCTION TABLE

ENABLE	SELECT INPUT	INPUTS		OUTPUT
$\overline{OE}$	S	I_0	I_1	Y
H	X	X	X	(Z)
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

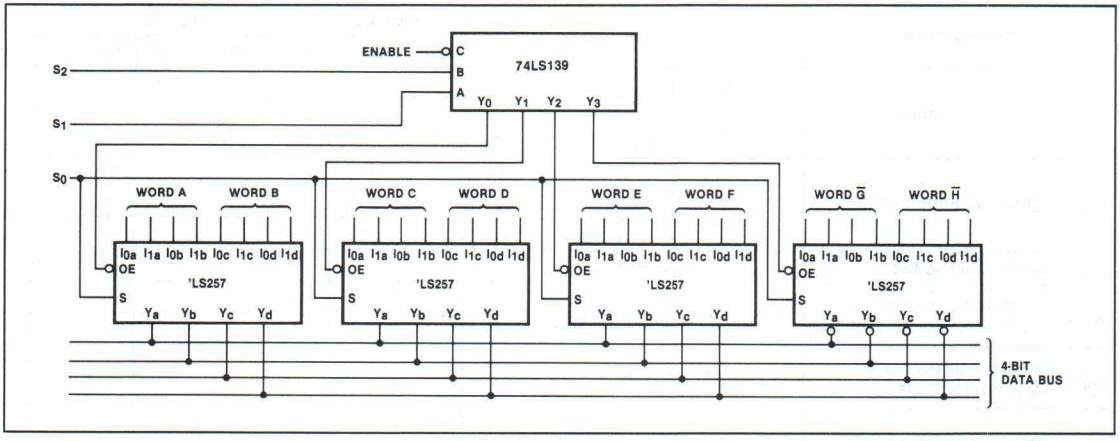
PARAMETER		TEST CONDITIONS[1]			54/74LS257A			54/74S257			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4	3.4		2.4	3.4		V
				Com'l	2.4	3.1		2.4	3.2		V
			I_{OH} = − 1mA	74S				2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				-20				μA
			V_O = 0.5V							-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V	S input			0.2				mA
				Other inputs			0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	S input			40			100	μA
				Other inputs			20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	S input			-0.8				mA
				Other inputs			-0.4				mA
			V_I = 0.5V	S input						-4	mA
				Other inputs						-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-30		-130	-40		-100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		6.2	10		44	68	mA
			I_{CCL}	Outputs LOW		10	16		60	93	mA
			I_{CCZ}	Outputs OFF		12	19		64	99	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

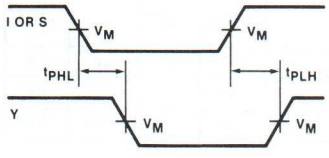
PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		18 18		7.5 7.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		21 21		15 15	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		30		19.5	ns
t_{PZL}	Output enable to LOW level	Waveform 3		30		21	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		30		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		25		14	ns

APPLICATION



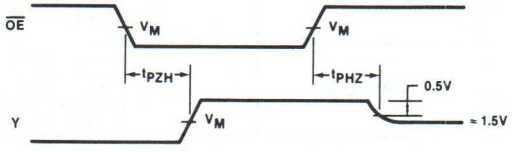
AC WAVEFORMS

PROPAGATION DELAY DATA AND SELECT TO OUTPUT



Waveform 1

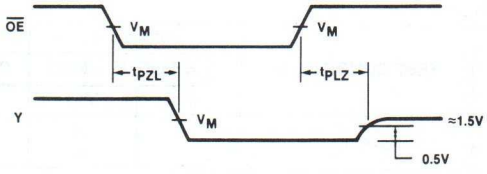
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

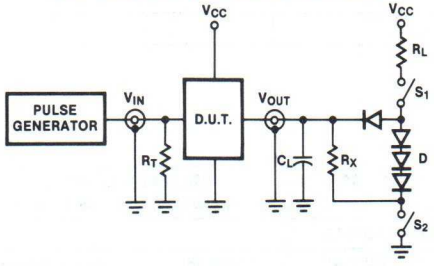
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



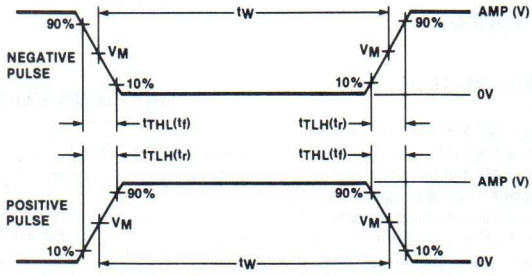
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

DATA SELECTORS/MULTIPLEXERS 54/74LS258A, S258

Quad 2-Line To 1-Line Data Selector/Multiplexer (3-State)

- **Multifunction capability**
- **Inverting data path**
- **3-State outputs**
- **See '257 for non-inverting version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS258A	13ns	9mA
74S258	6ns	48mA

DESCRIPTION

The '258 has four identical 2-input multiplexers with 3-State outputs which select 4 bits of data from two sources under control of a common Data Select input (S). The I_0 inputs are selected when the Select input is LOW and the I_1 inputs are selected when the Select input is HIGH. Data appears at the outputs in inverted (complementary) form.

The '258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

Outputs are forced to a HIGH impedance "off" state when the Output Enable input ($\overline{OE}$) is HIGH. All but one device must be in the HIGH impedance state to avoid currents exceeding the maximum ratings if outputs of the 3-state devices are tied together. Design of the Output Enable signals must ensure that there is no overlap when outputs of 3-state devices are tied together.

ORDERING CODE

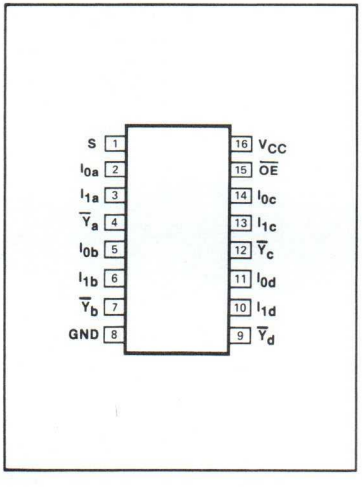
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S258N • N74LS258AN	
Ceramic DIP	N74S258F • N74LS258AF	S54S258F • S54LS258AF
Flatpack		S54S258W • S54LS258AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

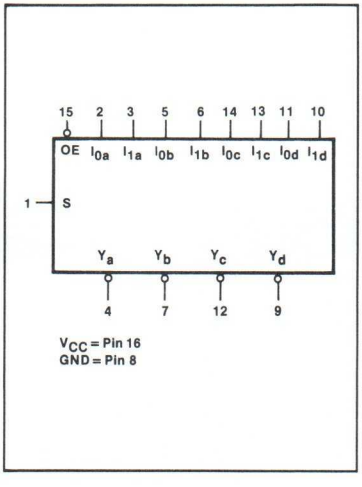
PINS	DESCRIPTION	54/74S	54/74LS
S	Input	2SuI	2LSuI
Other	Inputs	1SuI	1LSuI
All	Outputs	10SuI	30LSuI

NOTE
Where a 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

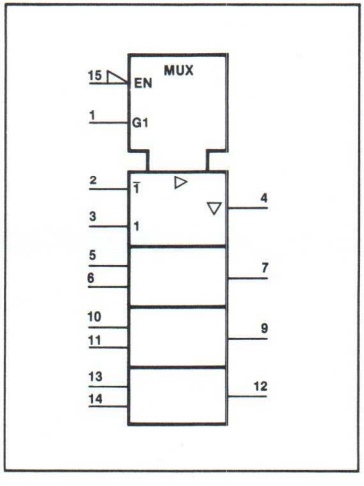
PIN CONFIGURATION



LOGIC SYMBOL

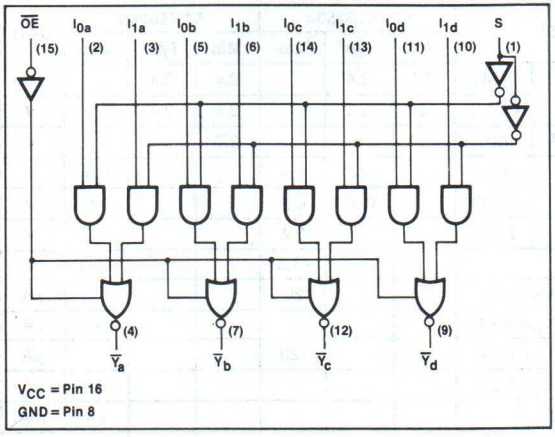


LOGIC SYMBOL (IEEE/IEC)



DATA SELECTORS/MULTIPLEXERS 54/74LS258A, S258

LOGIC DIAGRAM



FUNCTION TABLE

OUTPUT ENABLE	SELECT INPUT	DATA INPUTS		OUTPUTS
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	(Z)
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

	PARAMETER		54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS258A			54/74S258			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX	Mil	2.4	3.4		2.4	3.4		V
				Com'l	2.4	3.1		2.4	3.2		V
			I_{OH} = −1mA	74S				2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[5]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				−20				μA
			V_O = 0.5V							−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V	S input			0.2				mA
				Other inputs			0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V	S input			40			100	μA
				Other inputs			20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V	S input			−0.8				mA
				Other inputs			−0.4				mA
			V_I = 0.5V	S input						−4	mA
				Other inputs						−2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−30		−130	−40		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		4	7		36	56	mA
			I_{CCL}	Outputs LOW		8.8	14		52	81	mA
			I_{CCZ}	Outputs OFF		12	19		56	87	mA

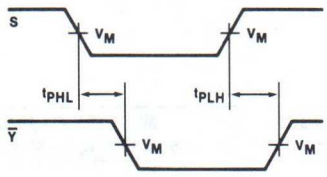
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open and all possible inputs grounded while achieving the stated output conditions.
5. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		18 18		6.0 6.0	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveforms 1 & 4		21 21		12 12	ns
t_{PZH}	Output enable to HIGH level	Waveform 2		30		19.5	ns
t_{PZL}	Output enable to LOW level	Waveform 3		30		21	ns
t_{PHZ}	Output disable from HIGH level	Waveform 2, C_L = 5pF		30		8.5	ns
t_{PLZ}	Output disable from LOW level	Waveform 3, C_L = 5pF		25		14	ns

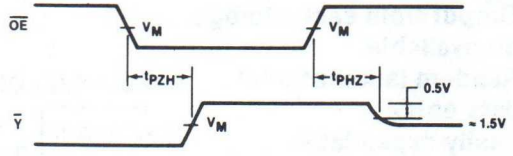
AC WAVEFORMS

PROPAGATION DELAY SELECT OUTPUT



Waveform 1

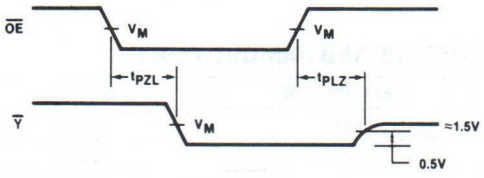
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

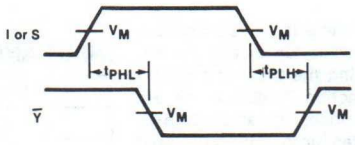
V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

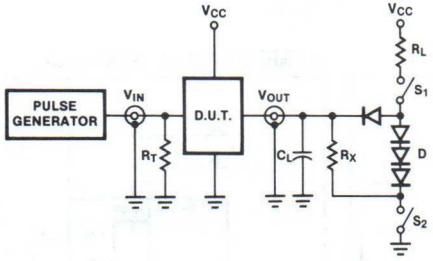
PROPAGATION DELAY DATA AND SELECT OUTPUT



Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



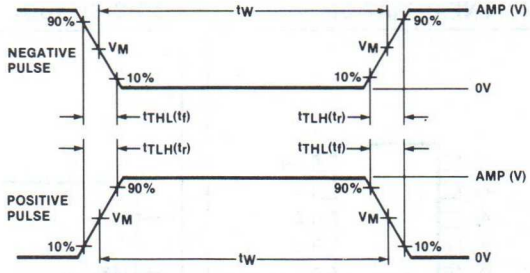
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74LS259

8-Bit Addressable Latch

- Combines demultiplexer and 8-bit latch
- Serial-to-parallel capability
- Output from each storage bit available
- Random (addressable) data entry
- Easily expandable
- Common Clear input
- Useful as a 1-of-8 active HIGH decoder

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS259	19ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS259N	
Ceramic DIP	N74LS259F	S54LS259F
Flatpack		S54LS259W

DESCRIPTION

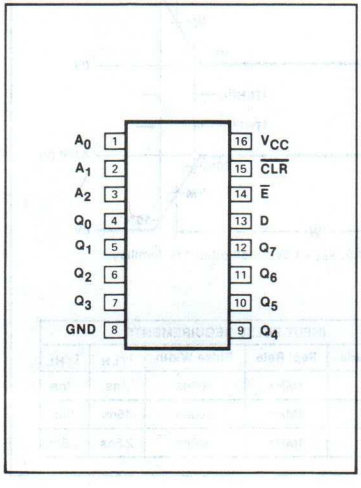
The '259 addressable latch has four distinct modes of operation that are selectable by controlling the Clear and Enable inputs (see Function Table). In the addressable latch mode, data at the Data (D) inputs is written into the addressed latches. The addressed latches will follow the Data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the Data or Address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held HIGH (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode ($\overline{CLR}$ = $\overline{E}$ = LOW), addressed outputs will follow the level of the D inputs, with all other outputs LOW. In the clear mode, all outputs are LOW and unaffected by the Address and Data inputs.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

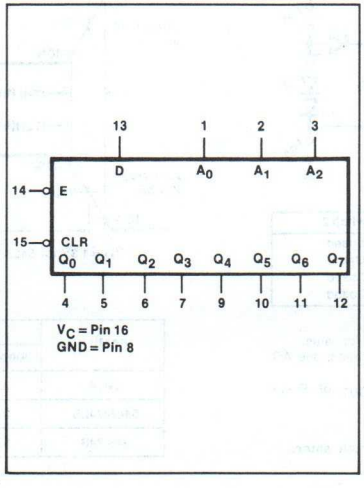
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

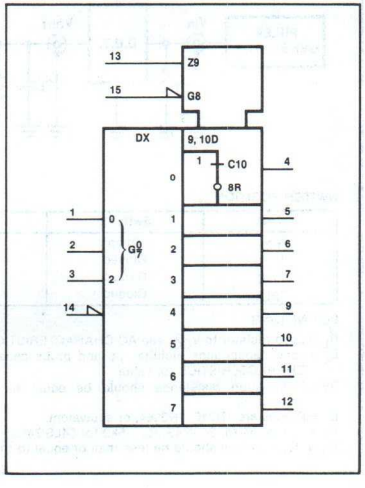
PIN CONFIGURATION



LOGIC SYMBOL

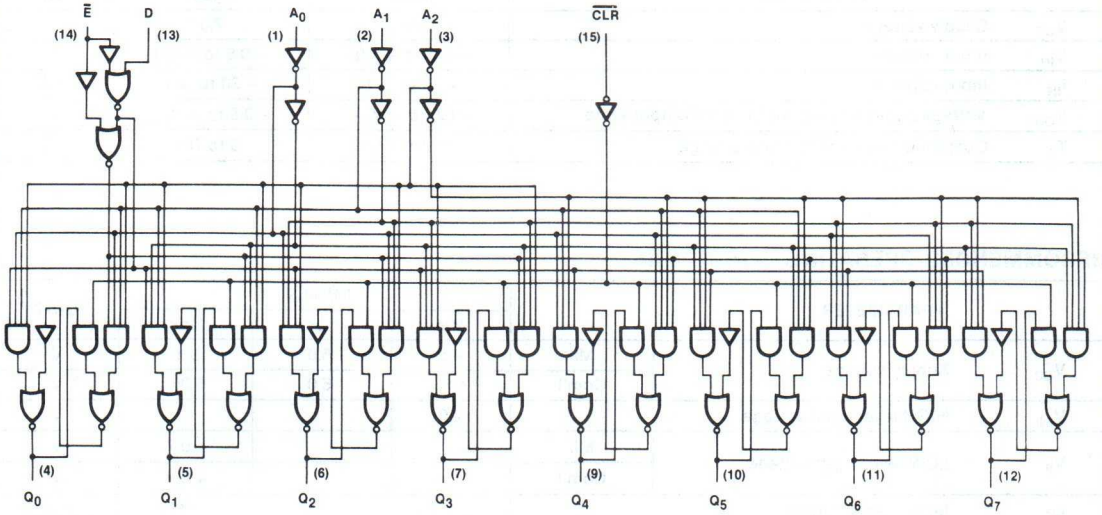


LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74LS259

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS							
	$\overline{CLR}$	$\overline{E}$	D	A_0	A_1	A_2	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
Clear	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (active HIGH decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (do nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable latch	H	L	d	L	L	L	Q = d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q = d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q = d	q_3	q_4	q_5	q_6	q_7
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q = d

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
X = Don't care.
d = HIGH or LOW data one setup time prior to the LOW-to-HIGH Enable transition.
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

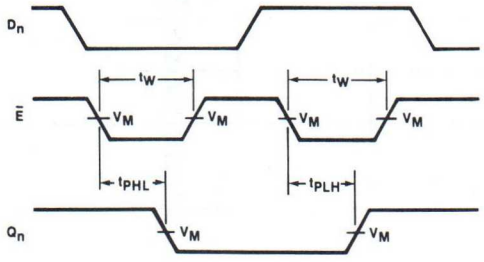
PARAMETER		TEST CONDITIONS[1]			54/74LS259			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				22	36	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the inputs grounded and the outputs open.

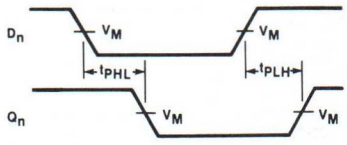
AC WAVEFORMS

PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH



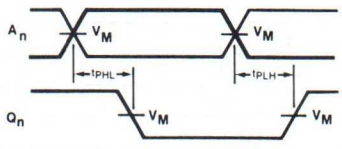
Waveform 1

PROPAGATION DELAY DATA TO OUTPUT



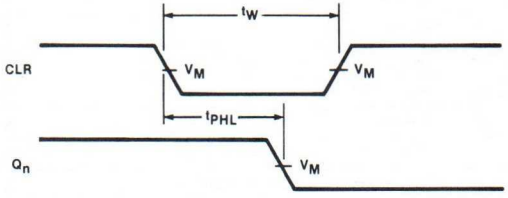
Waveform 2

PROPAGATION DELAY ADDRESS TO OUTPUT



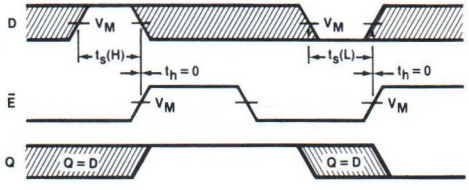
Waveform 3

CLEAR TO OUTPUT DELAY AND CLEAR PULSE WIDTH



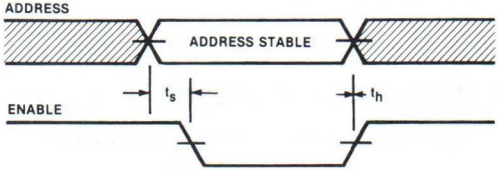
Waveform 4

DATA SETUP AND HOLD TIMES



Waveform 5

ADDRESS SETUP AND HOLD TIMES



Waveform 6

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$ Min	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1		35 24	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2		32 21	ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 3		38 29	ns
t_{PHL}	Propagation delay, Clear to output	Waveform 4		27	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	Enable pulse width	Waveform 1	15		ns
t_W	Clear pulse width	Waveform 4	15		ns
$t_s(H)$	Setup time HIGH, Data to Enable	Waveform 5	15		ns
$t_h(H)$	Hold time HIGH, Data to Enable	Waveform 5	5		ns
$t_S(L)$	Setup time LOW, Data to Enable	Waveform 5	15		ns
$t_h(L)$	Hold time LOW, Data to Enable	Waveform 5	5		ns
t_s	Setup time, Address to Enable[a]	Waveform 6	15		ns
t_h	Hold time, Address to Enable[b]	Waveform 6	15		ns

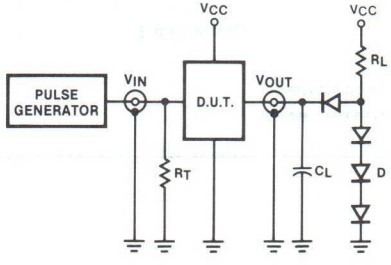
NOTES

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

TEST CIRCUITS AND WAVEFORMS

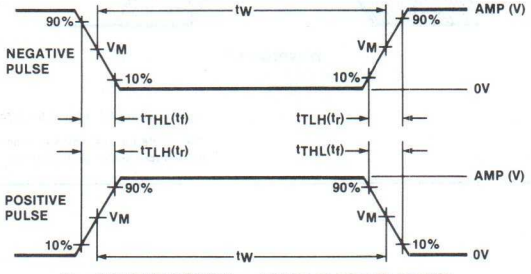
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



$V_M = 1.3V$ for 54LS/74LS; $V_M = 1.5V$ for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Dual 5-Input NOR Gate

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS260	9ns	4mA
74S260	4ns	22mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74S260N • N74LS260N	
Ceramic DIP	N74S260F • N74LS260F	S54S260F • S54LS260F
Flatpack		S54S260W • S54LS260W

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	E	Y
H	X	X	X	X	L
X	H	X	X	X	L
X	X	H	X	X	L
X	X	X	H	X	L
X	X	X	X	H	L
L	L	L	L	L	H

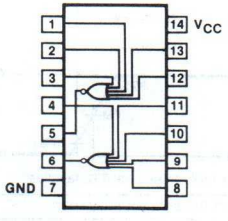
H = HIGH voltage level
L = LOW voltage level
X = Don't care

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

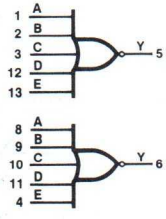
PINS	DESCRIPTION	54/74S	54/74LS
A-E	Inputs	1SuI	1LSuI
Y	Outputs	10SuI	10LSuI

NOTE
Where a 54/74S unit load (SuI) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSuI) is 20μA I_{IH} and −0.4mA I_{IL}.

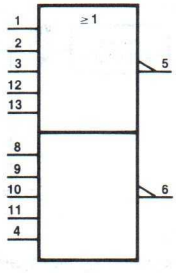
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

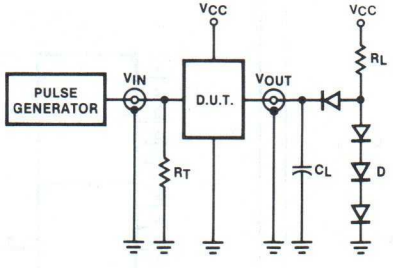
RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

TEST CIRCUITS AND WAVEFORMS

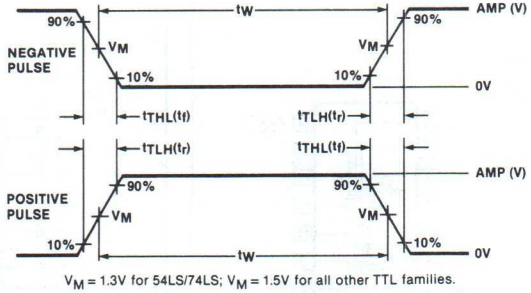
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

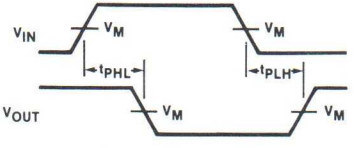
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS260			54/74S260			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5			2.5			V
				Com'l	2.7			2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN	I_{OL} = MAX	Mil			0.4			0.5[4]	V
				Com'l			0.5			0.5	V
			I_{OL} = 4mA	74LS			0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.7V				20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 15		– 100	– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH			4		17	29	mA
			I_{CCL}	Outputs LOW			5.5		26	45	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC WAVEFORM

WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

Waveform 1

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
t_{PLH}	Propagation delay	Waveform 1		12		5.5	ns
t_{PHL}				12		6.0	

GATE 54/74LS266

Quad 2-Input Exclusive-NOR Gate (Open Collector)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS266	18ns	8mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS266N	
Ceramic DIP	N74LS266F	S54LS266F
Flatpack		S54LS266W

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

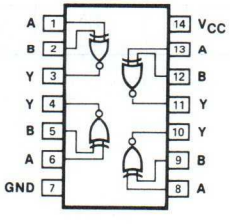
H = HIGH voltage level
L = LOW voltage level

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

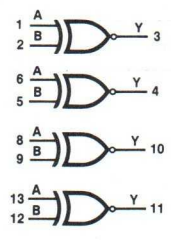
PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
Y	Output	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

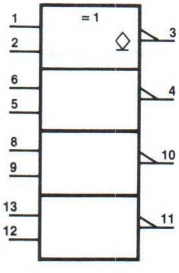
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

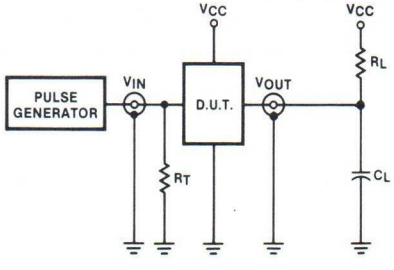
PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

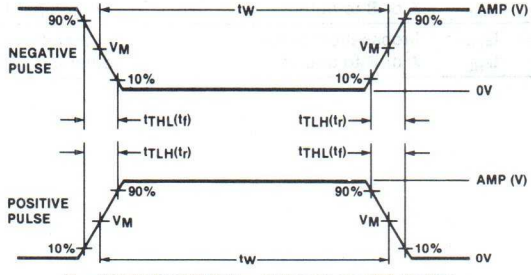
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

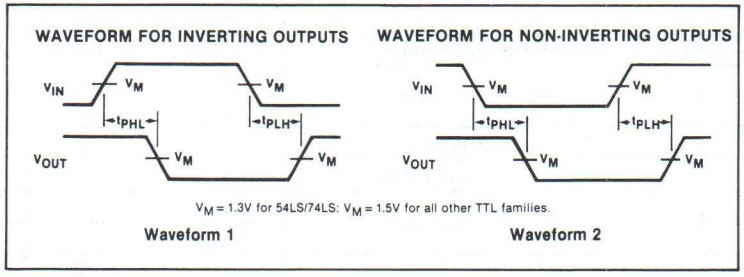
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS266			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 0.8	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				8	13	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with one input of each gate at 4.5V, the other inputs grounded and the outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 1, other input LOW		30 30	ns
t_{PLH} t_{PHL}	Propagation delay A or B to output	Waveform 2, other input HIGH		30 30	ns

Octal D Flip-Flops

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- High speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-pin plastic and ceramic DIP packages
- See '377 for Clock Enable version
- See '373 for transparent latch version
- See '374 for 3-state version

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS273	40MHz	17mA
74S273	95MHz	109mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S273N • N74LS273N	
Ceramic DIP	N74S273F • N74LS273F	S54LS273F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	10LSul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

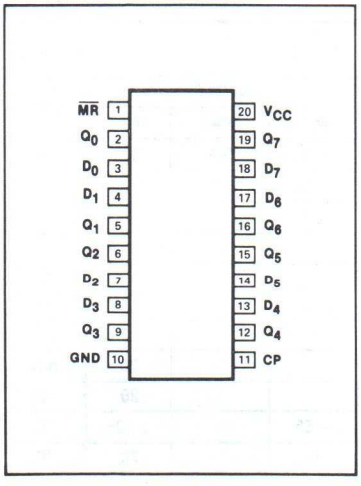
DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

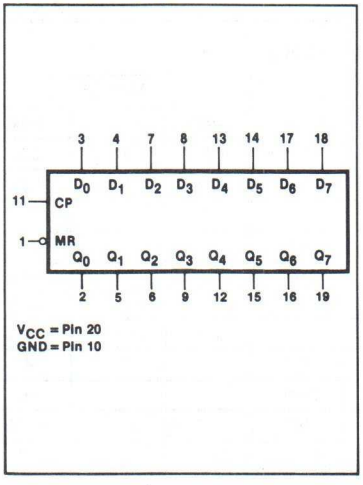
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

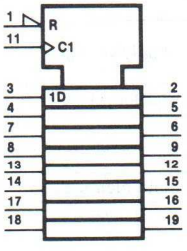
PIN CONFIGURATION



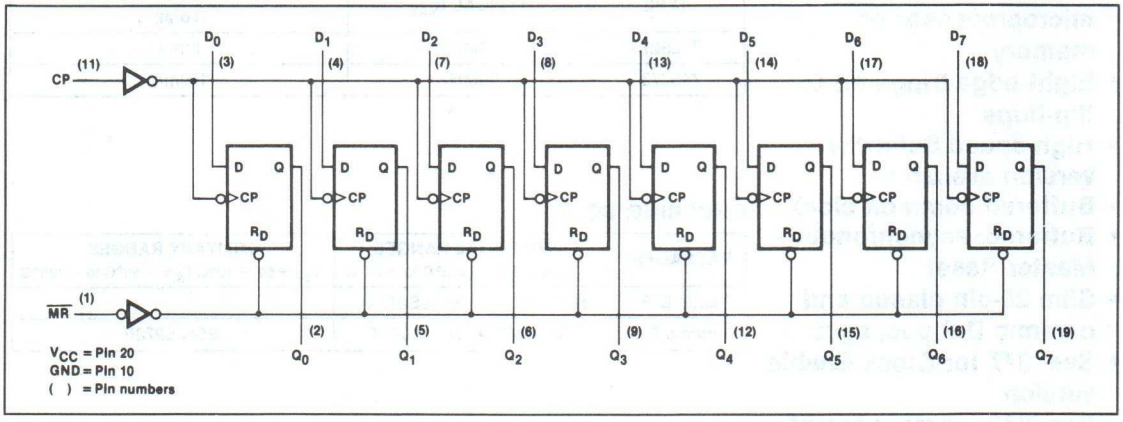
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



MODE SELECT--FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current				−400			−1000	μA
I_{OL}	LOW-level output current	Mil			4			20	mA
		Com'l			8			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS273			54/74S273			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		2.5			V
				Com'l	2.7	3.4		2.7			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V							1.0	mA
			V_I = 7.0V				0.1				mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	– 40		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				17	27		109	150	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} after a momentary ground, then 4.5V is applied to clock with all outputs open and 4.5V applied to all Data inputs and the Master Reset input.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			C_L = 15pF, R_L = 2kΩ		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27		15 15	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		27		15	ns

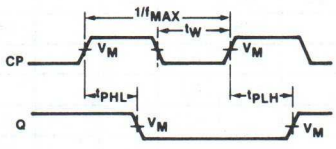
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_f, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		54S/74S		UNIT
			Min	Max	Min	Max	
t_W(L)	Clock pulse width (LOW)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
t_s(H)	Setup time, HIGH data to CP	Waveform 3	20		5.0		ns
t_h(H)	Hold time, HIGH data to CP	Waveform 3	5.0		3.0		ns
t_s(L)	Setup time, LOW data to CP	Waveform 3	20		5.0		ns
t_h(L)	Hold time, LOW data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

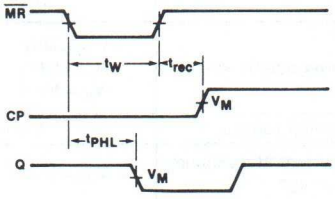
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



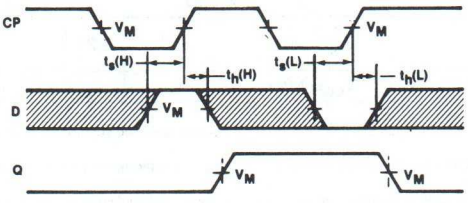
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



Waveform 2

DATA SET-UP AND HOLD TIMES

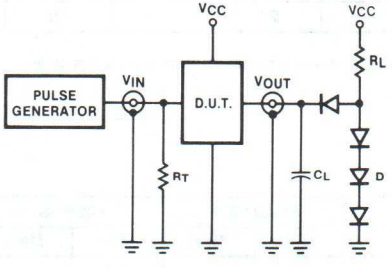


Waveform 3

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

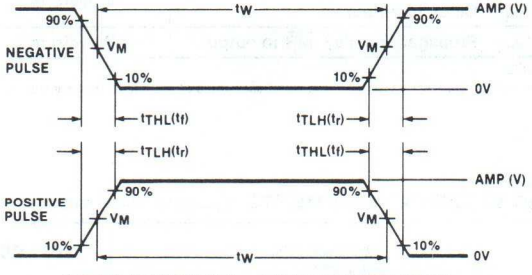
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74279

Quad Set-Reset Latch

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74279	13ns	18mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74279N	
Ceramic DIP	N74279F	S54279F
Flatpack		S54279W

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{S}_1$	$\overline{S}_2$	$\overline{R}$	Q
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No change

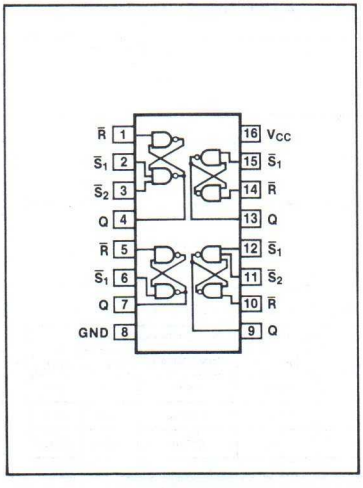
L = LOW voltage level.
H = HIGH voltage level.
X = Don't care.
h = The output is HIGH as long as $\overline{S}_1$ or $\overline{S}_2$ is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the truth table.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

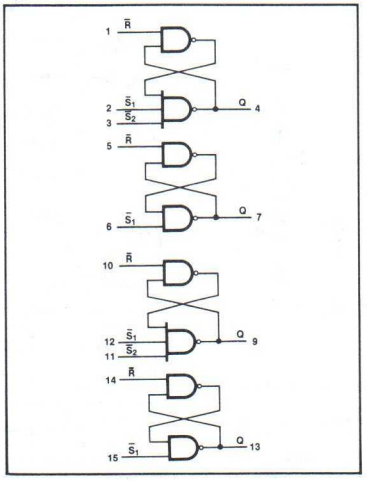
PINS	DESCRIPTION	54/74
All	Inputs	1ul
Q	Output	10ul

NOTE
A 54/74 unit load (ul) is 40μA I_{IH} and −1.6mA I_{IL}.

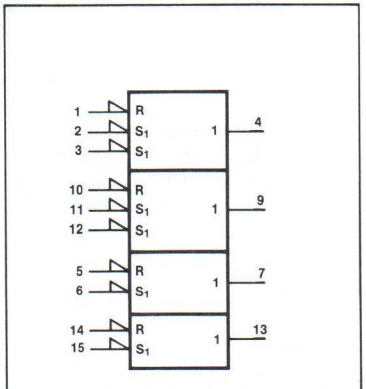
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74279

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

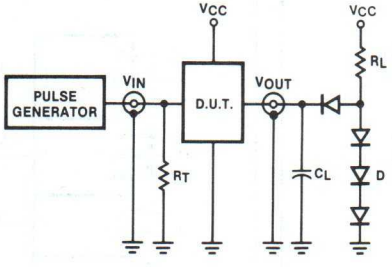
PARAMETER		54	74	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−12	mA
I_{OH}	HIGH-level output current				−800	μA
I_{OL}	LOW-level output current	Mil			16	mA
		Com'l			16	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

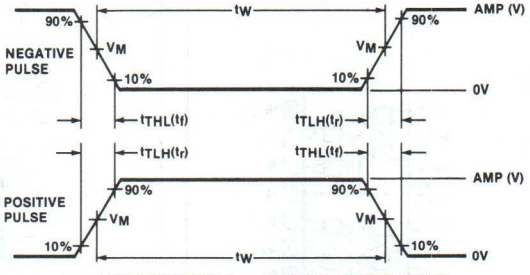
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

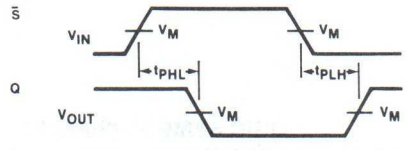
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

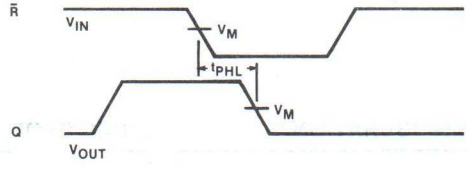
PARAMETER		TEST CONDITIONS[1]		54/74279 Min	54/74279 Typ[2]	54/74279 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4	3.4		V
			Com'l	2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil		0.2	0.4	V
			Com'l		0.2	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Mil	– 18		– 55	mA
			Com'l	– 18		– 57	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX			18	30	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V, and all outputs open.

AC WAVEFORMS



Waveform 1



Waveform 2

V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74 C_L = 15pF, R_L = 400Ω Min	54/74 C_L = 15pF, R_L = 400Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Set to output	Waveform 1		22 15	ns
t_{PHL}	Propagation delay Reset to output	Waveform 2		27	ns

PARITY GENERATOR/CHECKER 54/74S280

9-Bit Odd/Even Parity Generator/Checker

- **Buffered inputs — one normalized load**
- **Word-length easily expanded by cascading**
- **Similar pin configuration to '180 for easy system up-grading**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT
74S280	16ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S280N	
Ceramic DIP	N74S280F	S54S280F
Flatpack		S54S280W

DESCRIPTION

The '280 is a 9-bit parity generator or checker commonly used to detect errors in high-speed data transmission or data retrieval systems. Both Even and Odd parity outputs are available for generating or checking even or odd parity on up to 9 bits.

The Even parity output (Σ_E) is HIGH when an even number of Data inputs (I_0-I_8) are HIGH. The Odd parity output (Σ_O) is HIGH when an odd number of data inputs are HIGH.

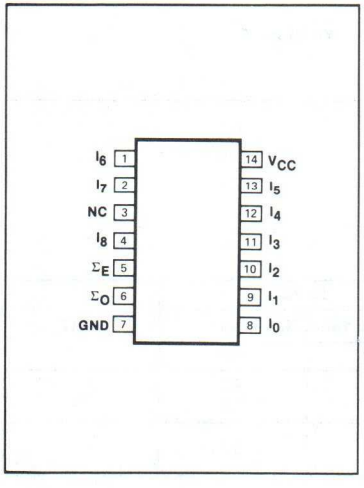
Expansion to larger word sizes is accomplished by tying the Even outputs (Σ_E) of up to nine parallel devices to the Data inputs of the final stage. This expansion scheme allows an 81-bit data word to be checked in less than 40ns with the 'S280.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

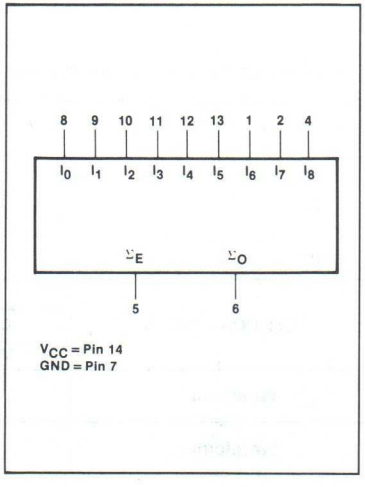
PINS	DESCRIPTION	54/74S
I_0-I_8	Data inputs	1Sul
Σ_E, Σ_O	Parity outputs	10Sul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

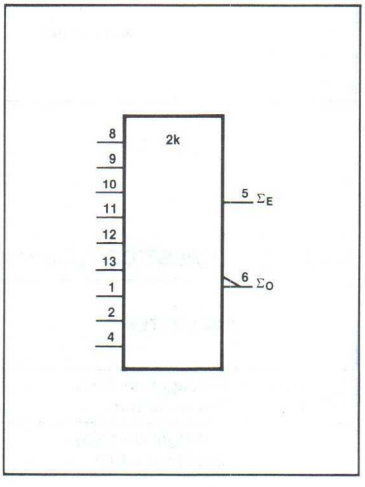
PIN CONFIGURATION



LOGIC SYMBOL

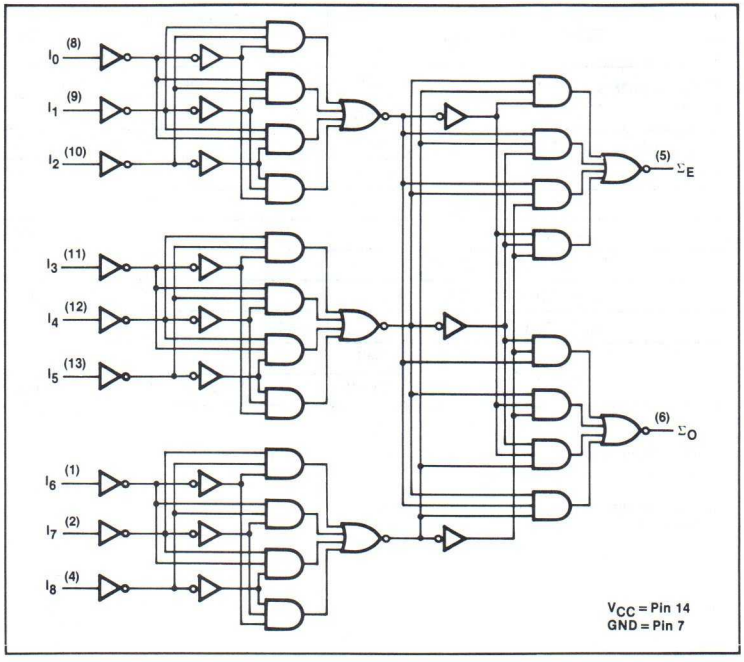


LOGIC SYMBOL (IEEE/IEC)



PARITY GENERATOR/CHECKER 54/74S280

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS	OUTPUTS	
Number of HIGH Data inputs (I_0–I_8)	Σ_E	Σ_O
Even	H	L
Odd	L	H

H = HIGH voltage level
L = LOW voltage level

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−1000	μA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

PARITY GENERATOR/CHECKER 54/74S280

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S280 Min	54/74S280 Typ[2]	54/74S280 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN	Mil	2.5	3.4		V
			Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = MAX, V_{IL} = MAX	Mil			0.5[5]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				− 1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				− 2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		− 40		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Mil			99	mA
			Com'l			105	mA

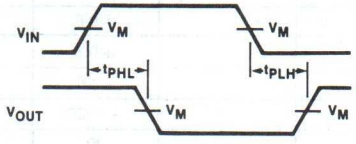
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all inputs grounded and all outputs open.
5. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74S280 C_L = 15pF, R_L = 280Ω Min	54/74S280 C_L = 15pF, R_L = 280Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Data to Even output	Waveforms 1 & 2		21 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to Odd output	Waveforms 1 & 2		21 18	ns

AC WAVEFORMS

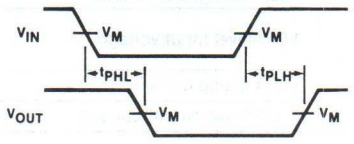
WAVEFORM FOR INVERTING OUTPUTS



V_M = 1.5V for 54/74 and 54S/74S

Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

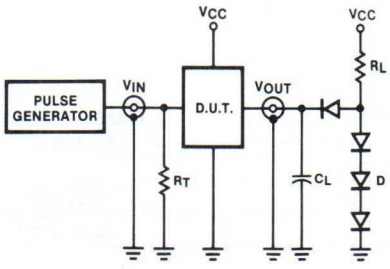


V_M = 1.5V for 54/74 and 54S/74S

Waveform 2

TEST CIRCUITS AND WAVEFORMS

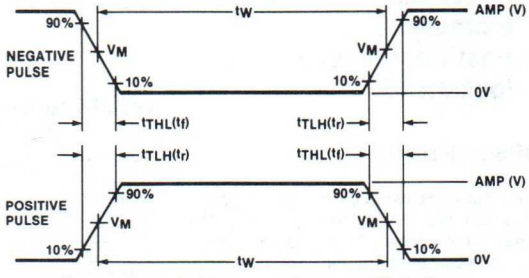
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

ADDER 54/74LS283

4-Bit Full Adder With Fast Carry

- **High-speed 4-bit binary addition**
- **Cascadable in 4-bit increments**
- **Fast internal carry lookahead**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS283	13ns	20mA

DESCRIPTION

The '283 adds two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the Sum outputs ($\Sigma_1 - \Sigma_4$) and the outgoing carry (C_{OUT}) according to the equation:

$$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + 4(A_3 + B_3) + 8(A_4 + B_4) = \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$$

Where (+) = plus.

Due to the symmetry of the binary add function, the '283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic)—see Function Table. In case of all active LOW operands the results Σ_1-Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} cannot be left open; it must be held LOW when no "carry in" is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can arbitrarily be assigned to pins 5, 6, 7, etc.

ORDERING CODE

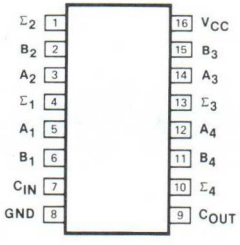
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS283N	
Ceramic DIP	N74LS283F	S54LS283F
Flatpack		S54LS283W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

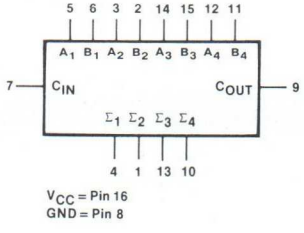
PINS	DESCRIPTION	54/74LS
A, B	Inputs	2LSul
C_{IN}	Input	1LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

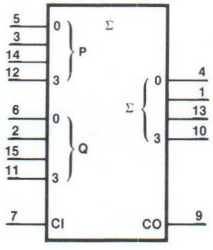
PIN CONFIGURATION



LOGIC SYMBOL

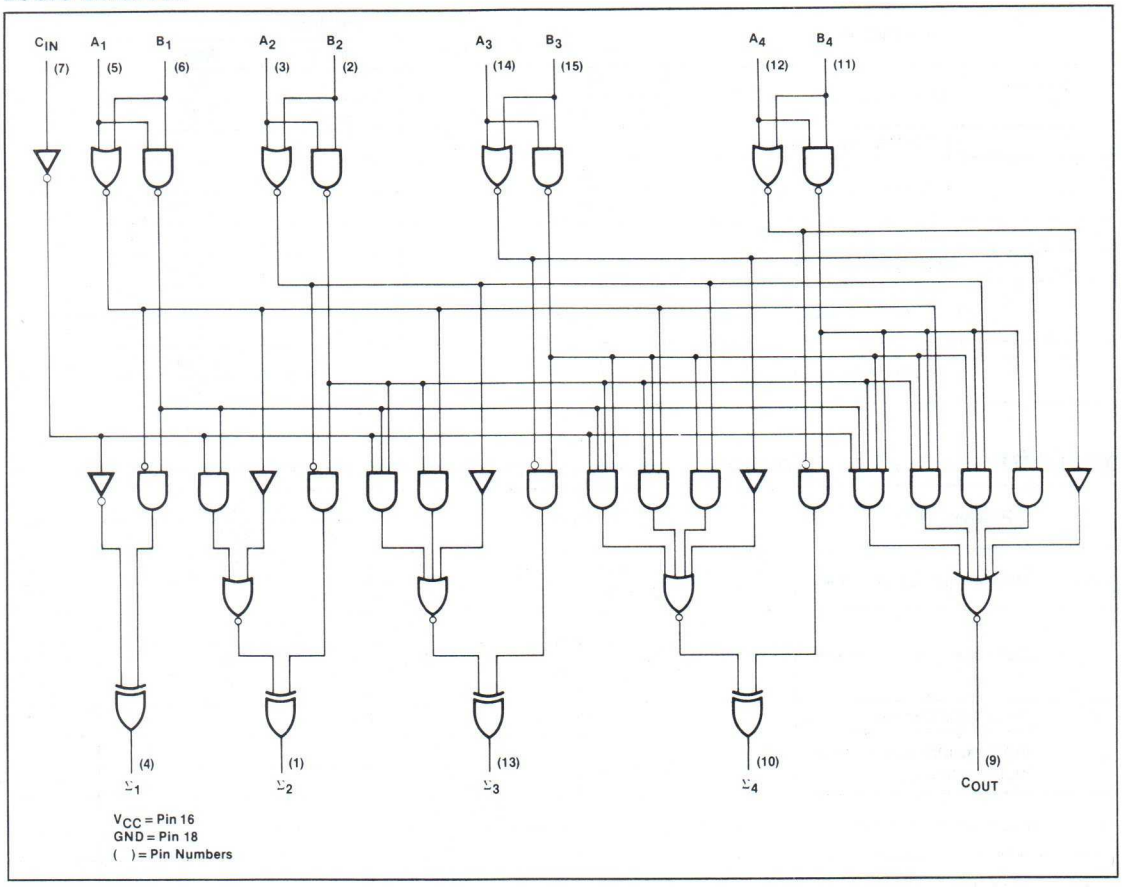


LOGIC SYMBOL (IEEE/IEC)



ADDER 54/74LS283

LOGIC DIAGRAM



FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0

H = LOW voltage level
L = LOW voltage level

Example:
1001
1010
10011
(10 + 9 = 19)
(carry + 5 + 6 = 12)

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 1	− 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

ADDER 54/74LS283

RECOMMENDED OPERATING CONDITIONS

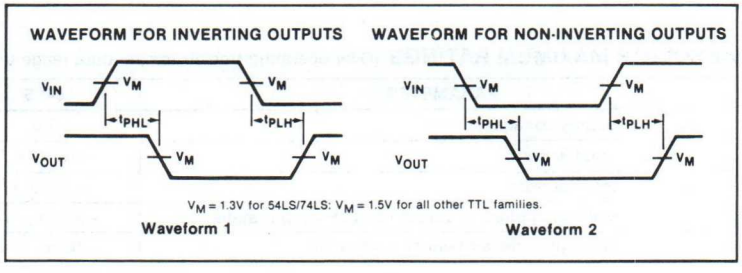
PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS283			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	A, B inputs				0.2	mA
			C_{IN} input				0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	A, B inputs				40	μA
			C_{IN} input				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	A, B inputs				− 0.8	mA
			C_{IN} input				− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1			22	39	mA
			Condition 2			19	34	mA
			Condition 3			19	34	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} should be measured with all outputs open and the following conditions:
   Condition 1: All inputs grounded.
   Condition 2: All B inputs LOW, other inputs at 4.5V.
   Condition 3: All inputs at 4.5V.

AC WAVEFORMS



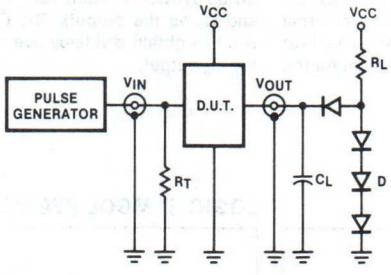
AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
		Min	Max	
t_{PLH} / t_{PHL} Propagation delay C_{IN} to Σ_1	Waveforms 1 & 2		24 24	ns
t_{PLH} / t_{PHL} Propagation delay C_{IN} to Σ_2	Waveforms 1 & 2		24 24	ns
t_{PLH} / t_{PHL} Propagation delay C_{IN} to Σ_3	Waveforms 1 & 2		24 24	ns
t_{PLH} / t_{PHL} Propagation delay C_{IN} to Σ_4	Waveforms 1 & 2		24 24	ns
t_{PLH} / t_{PHL} Propagation delay A_i or B_i to Σ_i	Waveforms 1 & 2		24 24	ns
t_{PLH} / t_{PHL} Propagation delay C_{IN} to C_{OUT}	Waveform 2		17 22	ns
t_{PLH} / t_{PHL} Propagation delay A_i or B_i to C_{OUT}	Waveforms 1 & 2		17 17	ns

3

TEST CIRCUITS AND WAVEFORMS

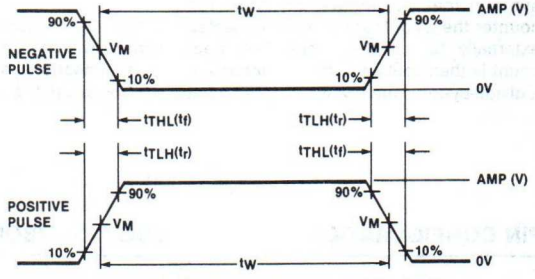
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER 54/74LS290

Decade Counter

DESCRIPTION

The '290 is a 4-bit, ripple type decade counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-five section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset ($MR_1 \cdot MR_2$) is provided which overrides both clocks and resets (clears) all the flip-flops. Also provided is a gated AND asynchronous Master Set ($MS_1 \cdot MS_2$) which overrides the Clock and MR Inputs, setting the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a BCD (8421) counter the $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count, producing a BCD count sequence. In a symmetrical bi-quinary divide-by-ten counter the Q_3 output must be connected externally to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0. To operate as a divide-by-two and a divide-by-five counter, no external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain divide-by-five operation at the Q_3 output.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS290	42MHz	9mA

ORDERING CODE

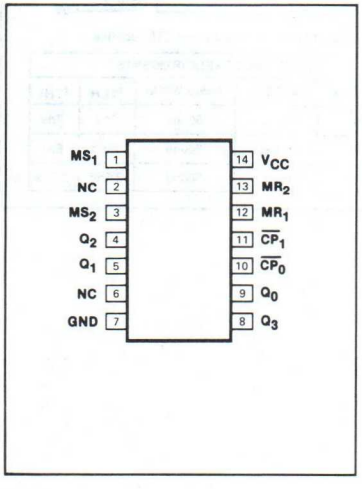
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS290N	
Ceramic DIP	N74LS290F	S54LS290F
Flatpack		S54LS290W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

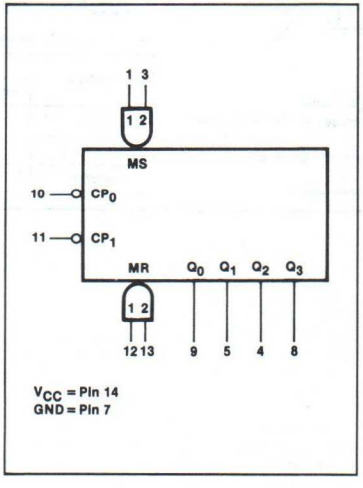
PINS	DESCRIPTION	54/74LS
MR, MS	Inputs	1LSul
$\overline{CP}_0$	Input	4LSul
$\overline{CP}_1$	Input	8LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

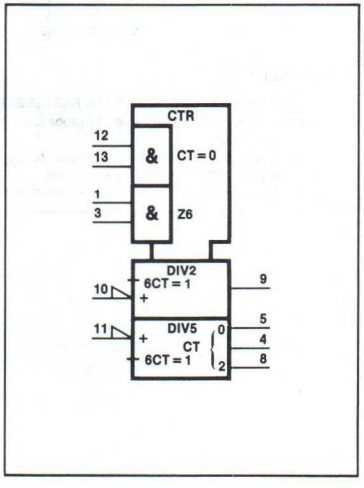
PIN CONFIGURATION



LOGIC SYMBOL

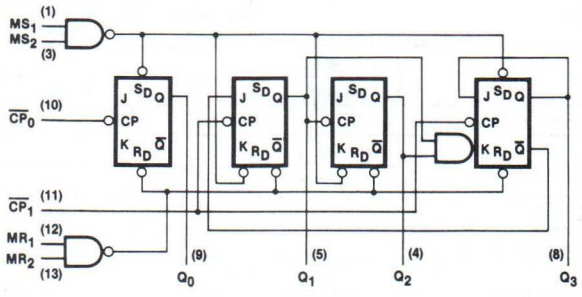


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS290

LOGIC DIAGRAM



V_{CC} = Pin 14
GND = Pin 7
( ) Pin numbers

MODE SELECTION—FUNCTION TABLE

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE—FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to +5.5V on CP_0 and CP_1 inputs only.

COUNTER 54/74LS290

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS290			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR, MS inputs			0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ input			0.2	mA
				$\overline{CP}_1$ input			0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR, MS inputs			20	μA
				$\overline{CP}_0$ input[5]			40	μA
				$\overline{CP}_1$ input[5]			80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR, MS inputs			−0.4	mA
				$\overline{CP}_0$ input			−2.4	mA
				$\overline{CP}_1$ input			−3.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−20		−100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				9	15	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with all outputs open, both MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.
5. The maximum limit for the 54LS290 only is 80μA for $\overline{CP}_0$ and 160μA for $\overline{CP}_1$ inputs.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

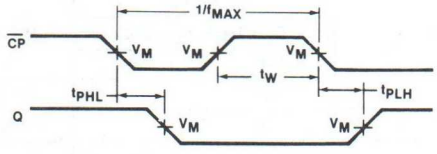
PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX}	$\overline{CP}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		48 50	ns
t_{PHL}	MR input to any output	Waveform 2		40	ns
t_{PLH}	MS input to Q_0 and Q_3 outputs	Waveform 3		30	ns
t_{PHL}	MS input to Q_1 and Q_2 outputs	Waveform 2		40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

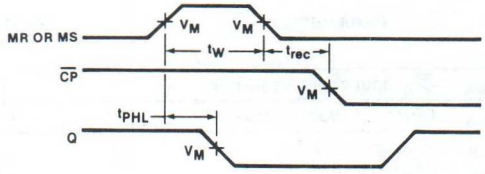
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	30		ns
t_W	MR pulse width	Waveform 2	15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns
t_{rec}	Recovery time, MS to $\overline{CP}$	Waveforms 2 and 3	25		ns

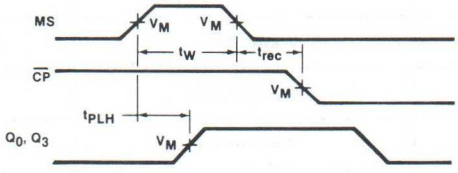
AC WAVEFORMS



Waveform 1



Waveform 2



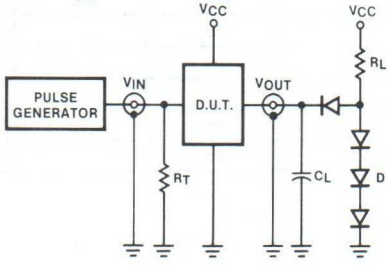
Waveform 3

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Function Tables.

TEST CIRCUITS AND WAVEFORMS

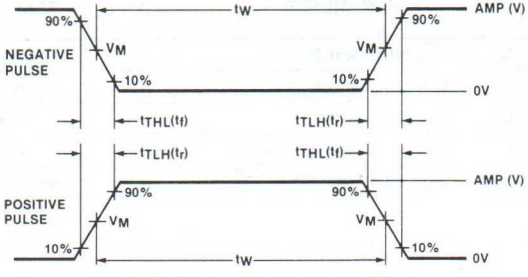
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER 54/74LS293

4-Bit Binary Ripple Counter

DESCRIPTION

The '293 is a 4-bit ripple type binary counter. The device consists of four master-slave flip-flops internally connected to provide a divide-by-two section and a divide-by-eight section. Each section has a separate Clock input to initiate state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes.

A gated AND asynchronous Master Reset (MR_1 MR_2) is provided which overrides both clocks and resets (clears) all the flip-flops.

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the device may be operated in various counting modes. In a 4-bit ripple counter the output Q_0 must be connected externally to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8 and 16 are performed at the Q_0, Q_1, Q_2 and Q_3 outputs as shown in the function table. As a 3-bit ripple counter the input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4 and 8 are available at the Q_1, Q_2 and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS293	42MHz	9mA

ORDERING CODE

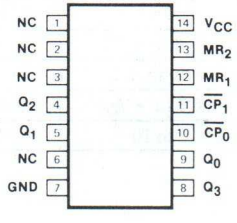
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS293N	
Ceramic DIP	N74LS293F	S54LS293F
Flatpack		S54LS293W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

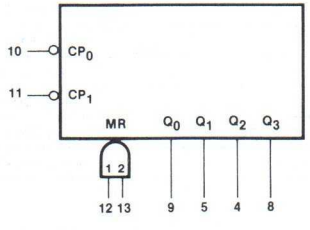
PINS	DESCRIPTION	54/74LS
MR	Inputs	1LSul
$\overline{CP}_0$	Input	6LSul
$\overline{CP}_1$	Input	4LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

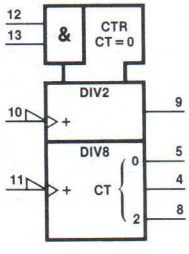
PIN CONFIGURATION



LOGIC SYMBOL

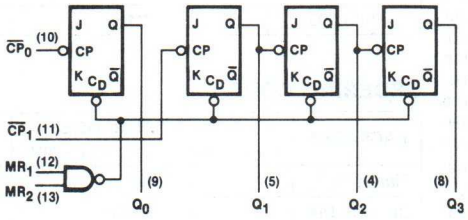


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS293

LOGIC DIAGRAM



( ) = Pin numbers
V_{CC} = Pin 14
GND = Pin 7

MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

FUNCTION TABLE

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS293			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR inputs			0.1	mA
			V_I = 5.5V	$\overline{CP}$ inputs			0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR inputs			20	μA
				$\overline{CP}$ inputs[5]			40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR inputs			− 0.4	mA
				$\overline{CP}_0$ input			− 2.4	mA
				$\overline{CP}_1$ input			− 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				9	15	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Clock inputs grounded, all outputs open, both MR inputs grounded following momentary connection to 4.5V.
5. The maximum limit for the 54LS293 is 80μA for $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

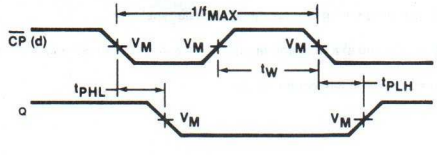
PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$ Min	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$ Max	UNIT
f_{MAX}	$\overline{CP}_0$ input count frequency	Waveform 1	32		MHz
f_{MAX}	$\overline{CP}_1$ input count frequency	Waveform 1	16		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_0 output	Waveform 1		16 18	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_1 output	Waveform 1		16 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_2 output	Waveform 1		32 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ input to Q_3 output	Waveform 1		51 51	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ input to Q_3 output	Waveform 1		70 70	ns
t_{PHL}	MR input to any output	Waveform 2		40	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

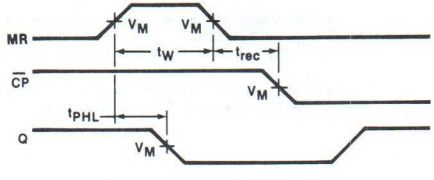
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	$\overline{CP}_0$ pulse width	Waveform 1	15		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	30		ns
t_W	MR pulse width	Waveform 2	15		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

AC WAVEFORMS



Waveform 1

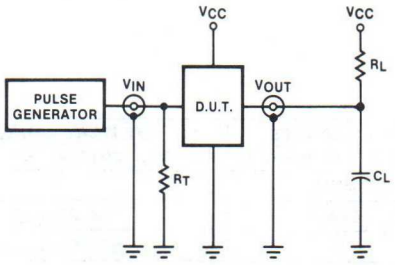


Waveform 2

$V_M = 1.5V$ for 54/74 and 54S/74S, $V_M = 1.3V$ for 54LS/74LS.
The number of Clock Pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

TEST CIRCUITS AND WAVEFORMS

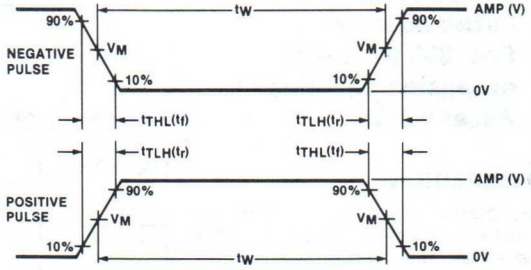
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

SHIFT REGISTER 54/74LS295B

4-Bit Shift Register With 3-State Outputs

- **4-bit parallel load shift register**
- **Independent 3-State buffer outputs**
- **See '395 for serial expansion and Master Reset version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS295B	45MHz	17mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS295BN	
Ceramic DIP	N74LS295BF	S54LS295BF
Flatpack		S54LS295BW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

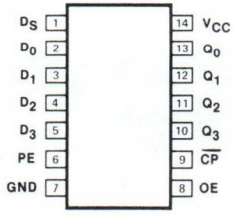
NOTE
A 54/74LS unit load (LSul) is 20μA and I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

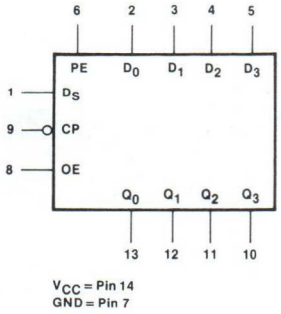
The '295B is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-State buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data outputs (D_0–D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative transition of the Clock. The PE and Data inputs are fully edge triggered and must be stable only one setup time prior to the HIGH-to-LOW transition of the Clock.

The 3-State output buffers are designed to drive heavily loaded 3-state buses or large capacitive loads. The active HIGH Output Enable (OE) controls all four 3-state buffers independent of the register operation. When OE is HIGH the data in the register appears at the outputs. When OE is LOW the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

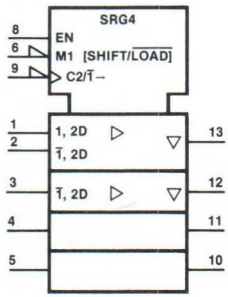
PIN CONFIGURATION



LOGIC SYMBOL

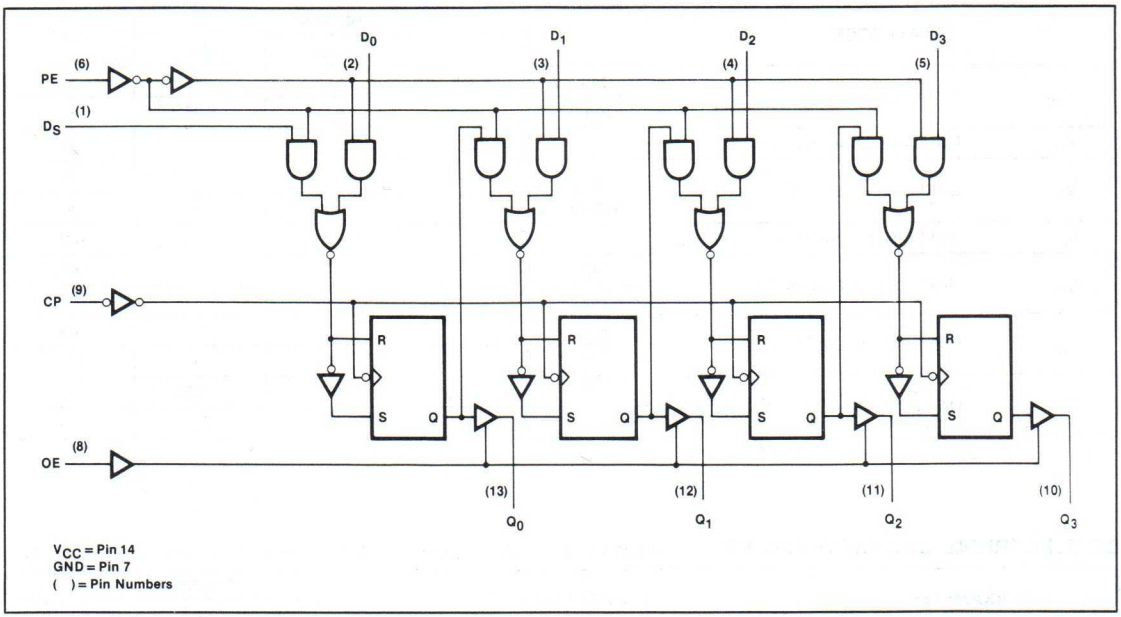


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/74LS295B

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS				REGISTER OUTPUTS			
	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Shift right	↓	l	l	X	L	q_0	q_1	q_2
	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	↓	h	X	l	L	L	L	L
	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	OE	Q_n (Register)	Q_0, Q_1, Q_2, Q_3
Read	H	L	L
	H	H	H
Disabled	L	X	(Z)

H = HIGH voltage level.
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition.
L = LOW voltage level.
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition.
X = Don't care.
(Z) = HIGH impedance "off" state.
↓ = HIGH-to-LOW clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current	Mil			– 1.0	mA
		Com'l			– 2.6	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS295B			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					–1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IL} = MAX, V_O = 2.7V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1			16	29	mA
			Condition 2			17	33	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with the outputs open, D_S and PE at 4.5V, and the Data inputs grounded under the following conditions:
   Condition 1: OE at 4.5V and a momentary 3V, then ground, applied to the Clock input.
   Condition 2: OE and Clock input grounded.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		23 30	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		26	ns
t_{PZL}	Enable time to LOW level	Waveform 3		30	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5pF$		20	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5pF$		20	ns

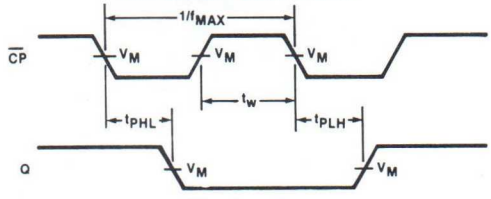
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	16		ns
t_s	Setup time, Data to clock	Waveform 4	20		ns
t_h	Hold time, Data to clock	Waveform 4	20		ns
t_s	Setup time, PE to clock	Waveform 4	20		ns
t_h	Hold time, PE to clock	Waveform 4	10		ns

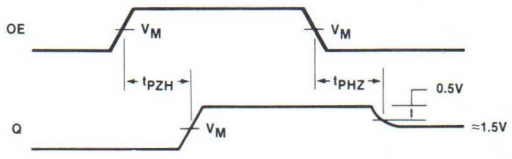
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL

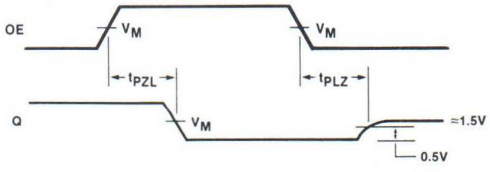


Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

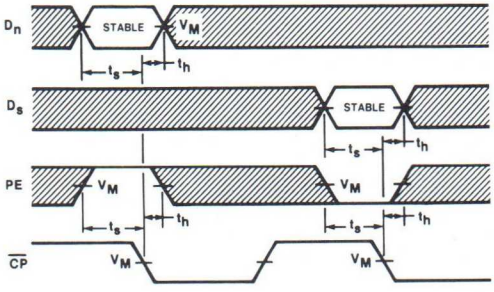
The shaded areas indicate when the input is permitted to change for predictable output performance.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

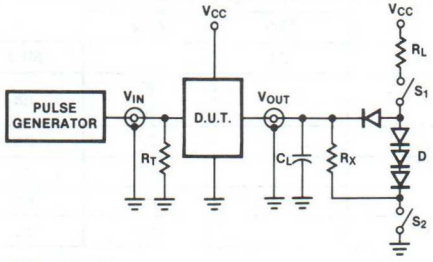
PARALLEL ENABLE AND DATA SETUP AND HOLD TIMES



Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



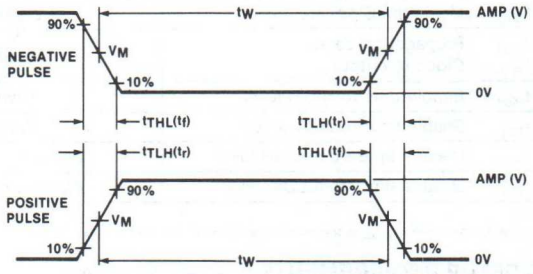
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

PORT REGISTERS 54/74298, LS298

Quad 2-Port Register

- **Fully synchronous operation**
- **Select from two data sources**
- **Buffered, negative edge triggered clock**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74298	19ns	39mA
74LS298	19ns	13mA

DESCRIPTION

This device is a high-speed Quad 2-Port Register. It selects 4 bits of data from two sources (Ports) under the control of a common Select input (S). The selected data is transferred to the 4-bit output register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). The 4-bit register is fully edge triggered. The Data inputs (I_0 and I_1) and Select input (S) must be stable only one setup time prior to the HIGH-to-LOW transition of the clock for predictable operation.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74298N • N74LS298N	
Ceramic DIP	N74298F • N74LS298F	S54LS298F
Flatpack		S54LS298W

MODE SELECT— FUNCTION TABLE

OPERATING MODE	INPUTS				OUTPUTS
	$\overline{CP}$	S	I_0	I_1	Q_n
Load Source "0"	↓	l	l	X	L
	↓	l	h	X	H
Load Source "1"	↓	h	X	l	L
	↓	h	X	h	H

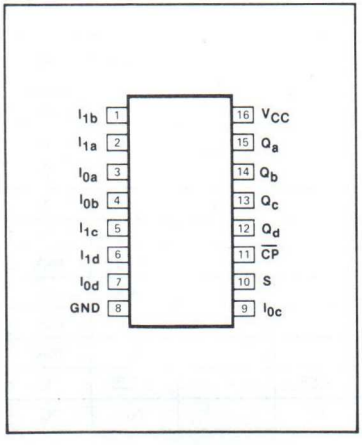
H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition.
X = Don't care
↓ = HIGH-to-LOW clock transition.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

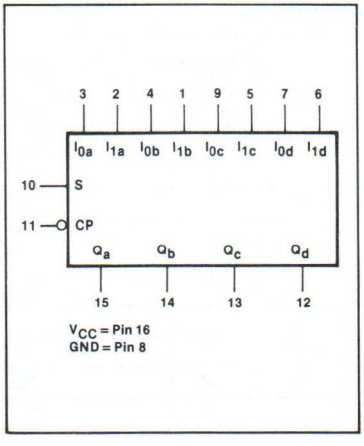
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	10ul	10LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

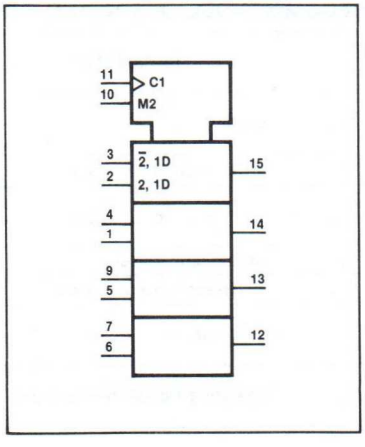
PIN CONFIGURATION



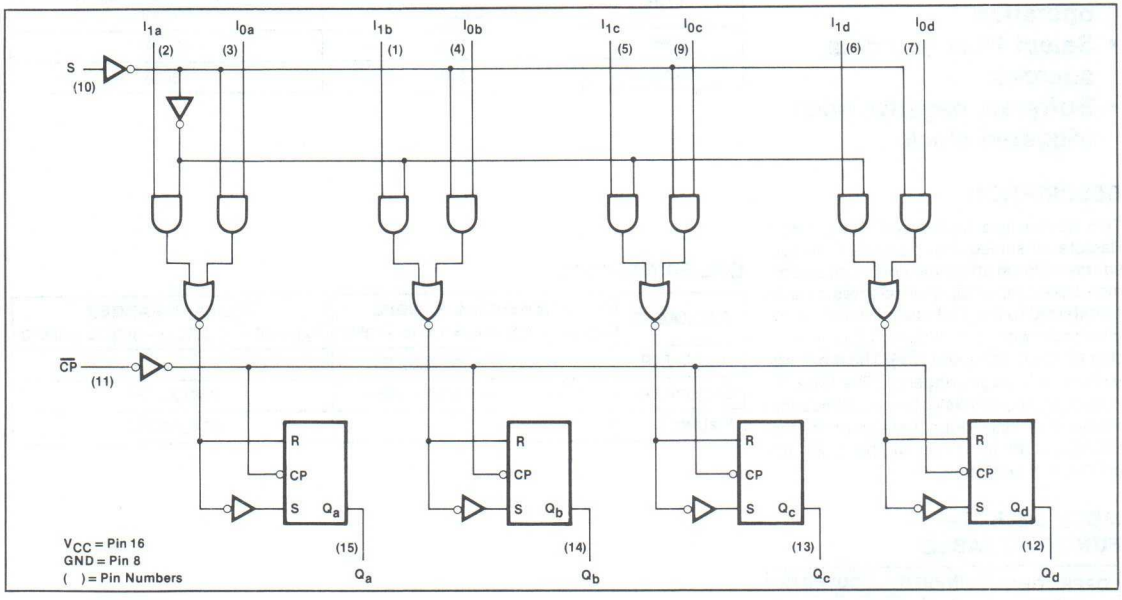
LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current				−800			−400	μA
I_{OL}	LOW-level output current	Mil			16			4	mA
		Com'l			16			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74298			54/74LS298			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.5	3.4		V
				Com'l	2.4	3.4		2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 4mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 1.6			– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		Mil	– 20		– 57	– 20		– 100	mA
				Com'l	– 18		– 57	– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				39	65		13	21	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured after applying a momentary 4.5V, followed by ground to the Clock input, with all other inputs low and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

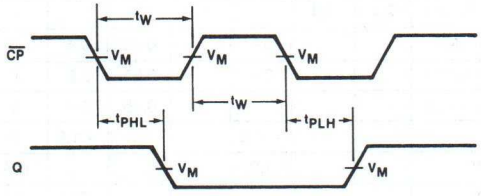
PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			C_L = 15pF, R_L = 400Ω		C_L = 15pF, R_L = 2kΩ		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 32		27 32	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74		54LS/74LS		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		ns
t_s	Setup time, Data to Clock	Waveform 2	15		15		ns
t_h	Hold time, Data to Clock	Waveform 2	5		5		ns
t_s	Setup time, Select to Clock	Waveform 2	25		25		ns
t_h	Hold time, Select to Clock	Waveform 2	0		0		ns

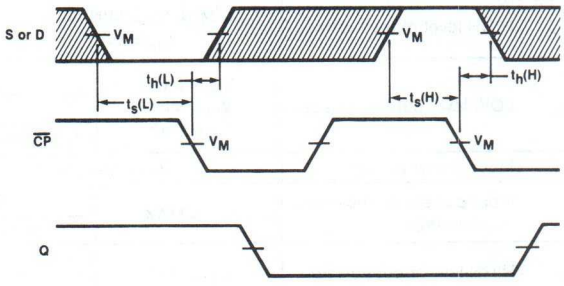
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA SETUP AND HOLD TIMES

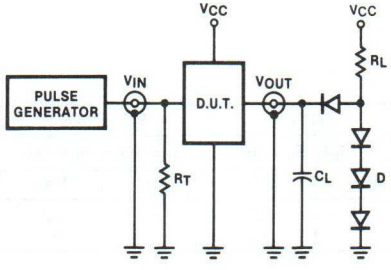


Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded ares indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

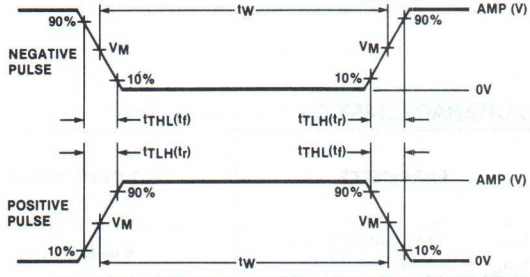
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFTER 54/74S350

4-Bit Shifter With 3-State Outputs

- **Shifts 4 bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**
- **Alternate source AM25S10**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S350	7ns	71mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S350N	
Ceramic DIP	N74S350F	S54S350F
Flatpack		S54S350W

DESCRIPTION

The '350 is a combination logic circuit that shifts a 4-bit word from 0 to 3 places. No clocking is required as with shift registers.

The '350 can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical — with logic zeros filled in at either end of the shifting field.
2. Arithmetic — where the sign bit is extended during a shift down.
3. End around — where the data word forms a continuous loop.

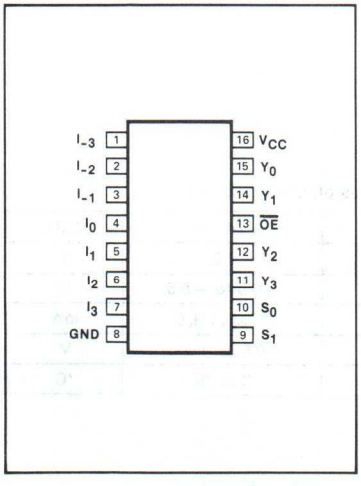
The 3-State outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the HIGH impedance "off" state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

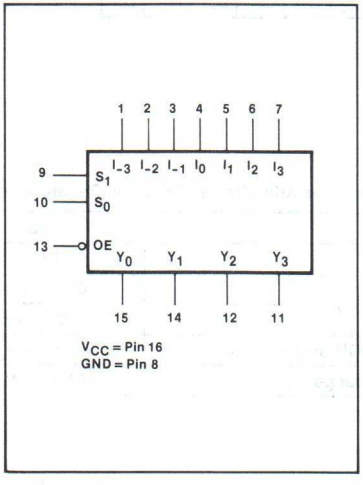
PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
A 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

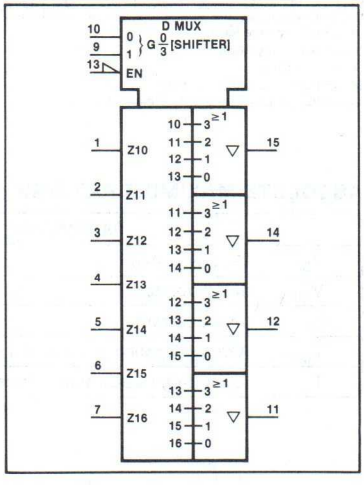
PIN CONFIGURATION



LOGIC SYMBOL

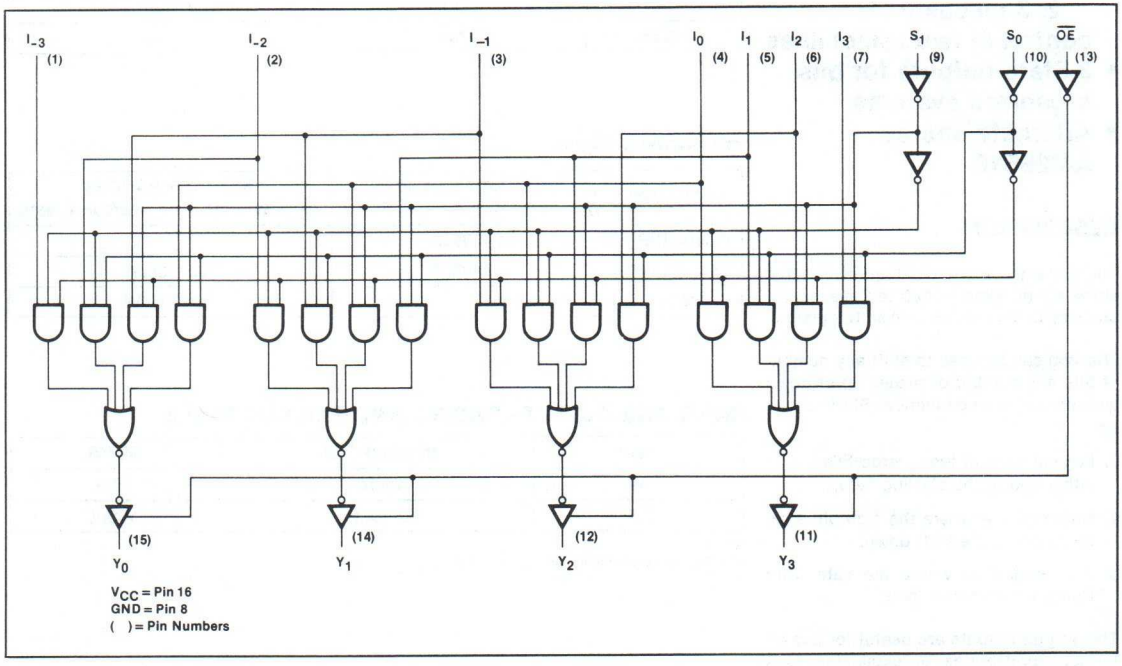


LOGIC SYMBOL (IEEE/IEC)



SHIFTER 54/74S350

LOGIC DIAGRAM



FUNCTION TABLE

OE	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance (off) state
D_n = HIGH or LOW state of referenced I_n input

LOGIC EQUATIONS

$$Y_0 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_0 + S_0 \cdot \overline{S}_1 \cdot I_{-1} + \overline{S}_0 \cdot S_1 \cdot I_{-2} + S_0 \cdot S_1 \cdot I_{-3}$$
$$Y_1 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_1 + S_0 \cdot \overline{S}_1 \cdot I_0 + \overline{S}_0 \cdot S_1 \cdot I_{-1} + S_0 \cdot S_1 \cdot I_{-2}$$
$$Y_2 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_2 + S_0 \cdot \overline{S}_1 \cdot I_1 + \overline{S}_0 \cdot S_1 \cdot I_0 + S_0 \cdot S_1 \cdot I_{-1}$$
$$Y_3 = \overline{S}_0 \cdot \overline{S}_1 \cdot I_3 + S_0 \cdot \overline{S}_1 \cdot I_2 + \overline{S}_0 \cdot S_1 \cdot I_1 + S_0 \cdot S_1 \cdot I_0$$

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	− 0.5 to + 5.5	− 0.5 to + 5.5	V
I_{IN}	Input current	− 30 to + 5	− 30 to + 5	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IH}	Input clamp current				– 18	mA
I_{OH}	HIGH-level output current	Mil			– 2.0	mA
		Com'l			– 6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	– 55		+ 125	°C
		Com'l	0		70	°C

V_{IL} = + 0.7V MAX for 54S at T_A = + 125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74S350			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Mil	2.4			V
			Com'l	2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OL} = MAX	Mil			0.5[4]	V
			Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}				–1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V				–50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				–2.0	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX		–40		–100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, V_{IN} = 0V			71	85	mA

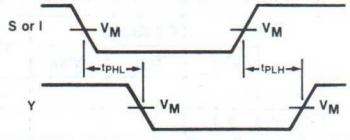
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54S/74S $C_L = 15pF$, $R_L = 280\Omega$ Min	54S/74S $C_L = 15pF$, $R_L = 280\Omega$ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 1		17 20	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		19.5	ns
t_{PZL}	Enable time to LOW level	Waveform 3		21	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5pF$		8.0	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5pF$		15	ns

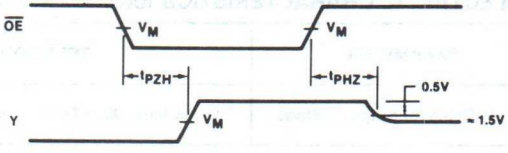
AC WAVEFORMS

PROPAGATION DELAY DATA (I) OR SELECT (S) TO OUTPUT



Waveform 1

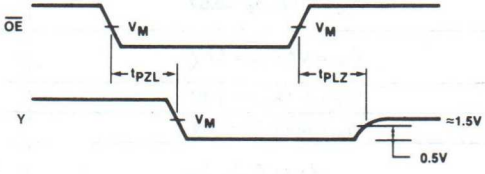
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

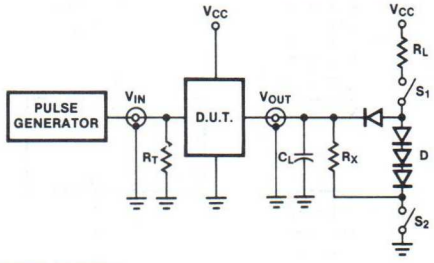
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



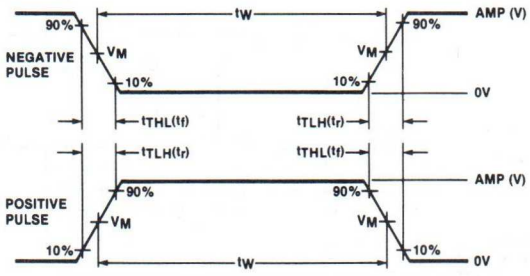
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



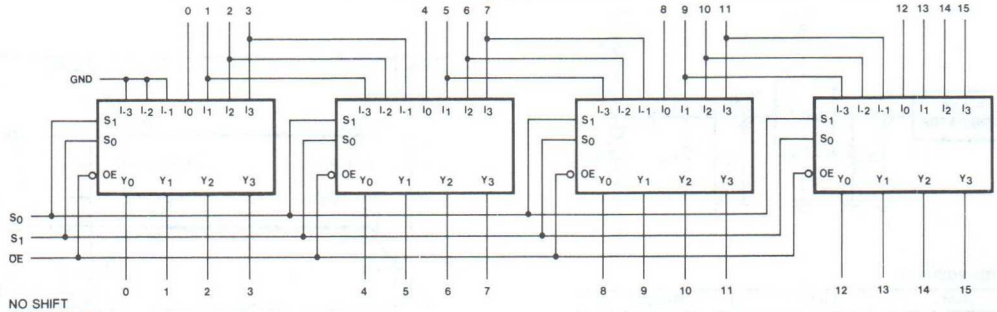
V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

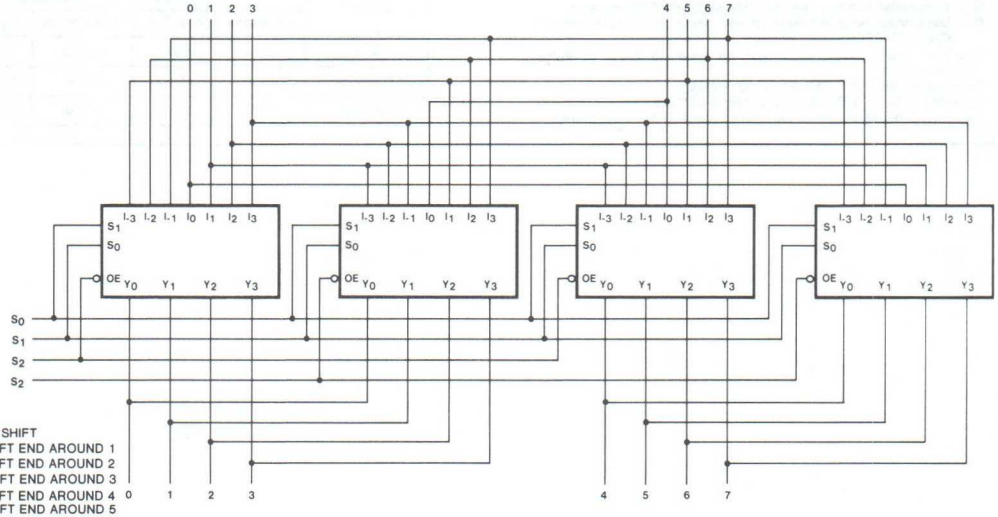
APPLICATIONS

16-BIT SHIFT-UP 0, 1, 2, OR 3 PLACES



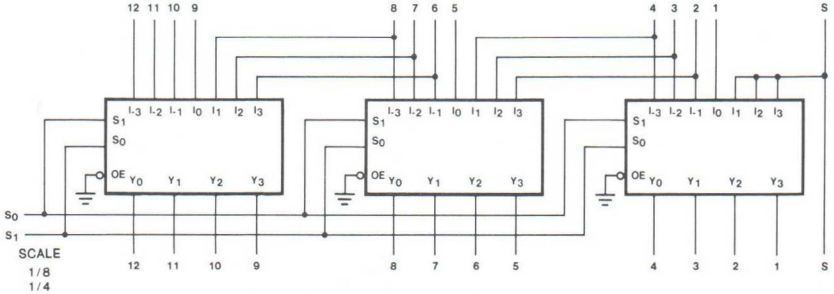
S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

8-BIT END AROUND SHIFT 0, 1, 2, 3, 4, 5, 6, 7 PLACES



S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-BIT 2's COMPLEMENT SCALER



S_1	S_0	SCALE
L	L	÷8
L	H	÷4
H	L	÷2
H	H	NO CHANGE

SCALE
1/8
1/4
1/2
1

LATCH 54/74LS363

Octal Transparent Latch With 3-State Outputs

- 8-bit transparent latch
- 3-State MOS compatible output buffers
- Common Latch Enable input with hysteresis
- Common 3-state Output Enable control
- Independent latch and 3-state buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS363	19ns	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS363N	
Ceramic DIP	N74LS363F	S54LS363F

3

DESCRIPTION

The '363 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs is transferred to the Latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the Data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC}, or to over 3.5V at minimum V_{CC}. This feature makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V.

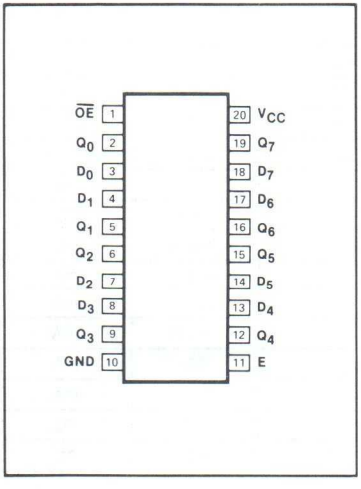
The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

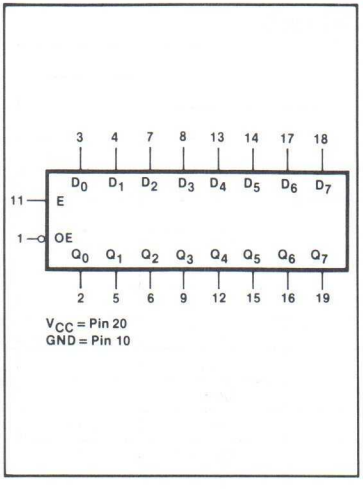
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

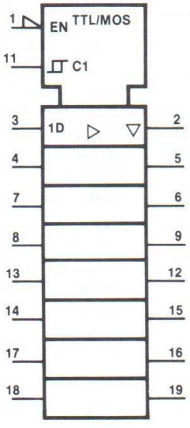
PIN CONFIGURATION



LOGIC SYMBOL

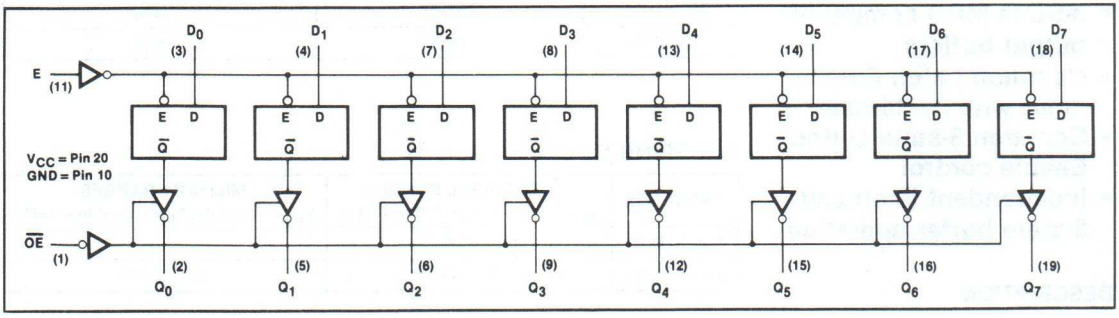


LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74LS363

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0–Q_7
Enable and read register	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = HIGH impedance "off" state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0	mA
		Com'l			−2.6	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS363			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	3.45			V
				Com'l	3.65			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IL} = MAX, V_O = 3.65V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					− 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 30		− 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{OE}$ = 4.5V				42	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

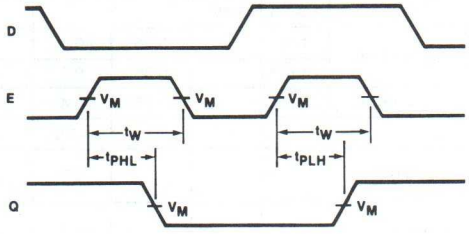
PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			C_L = 45pF, R_L = 667Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1		30 36	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		23 27	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t_{PZL}	Enable time to LOW level	Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		20	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		25	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Latch Enable pulse width	Waveform 1	15		ns
t_s	Setup time, Data to Latch Enable	Waveform 5	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5	10		ns

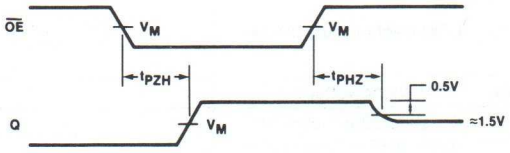
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



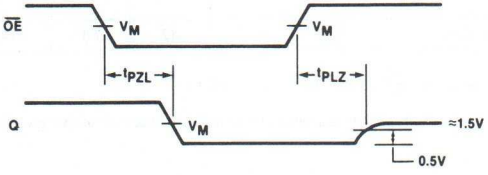
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



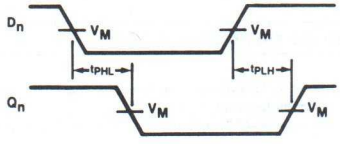
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



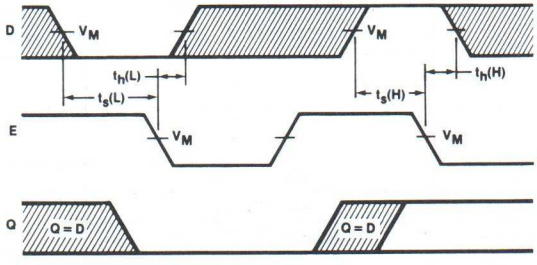
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES



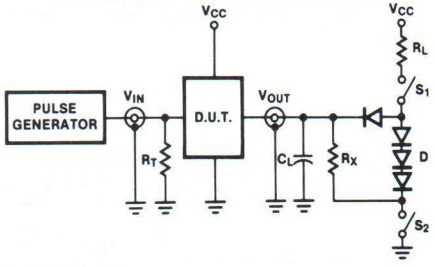
Waveform 5

V_M= 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



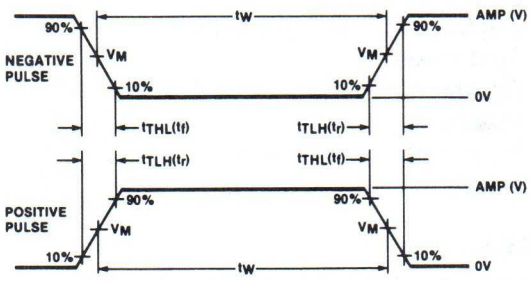
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

FLIP-FLOP 54/74LS364

Octal D Flip-Flop With 3-State Outputs

- 8-bit positive edge-triggered register
- 3-State MOS compatible output buffers
- Common Clock input with hysteresis
- Common 3-state Output Enable control
- Independent register and 3-state buffer operation

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS364	50MHz	42mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS364N	
Ceramic DIP	N74LS364F	S54LS364F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

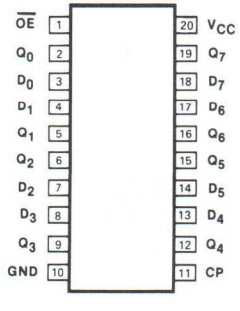
DESCRIPTION

The '364 is an 8-bit edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

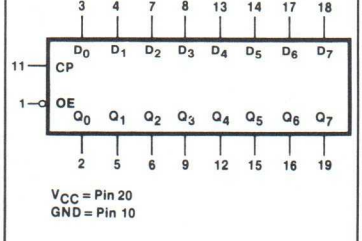
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-state buses, MOS memories, or MOS microprocessors. The output HIGH level differs from the normal 3-state buffer by driving the output about 1V closer to V_{CC}, or to over 3.5V at minimum V_{CC}. This feaure makes these devices ideal for driving MOS memories or microprocessors with thresholds of 2.4V to 3.5V. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-state buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

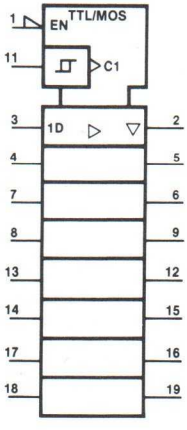
PIN CONFIGURATION



LOGIC SYMBOL

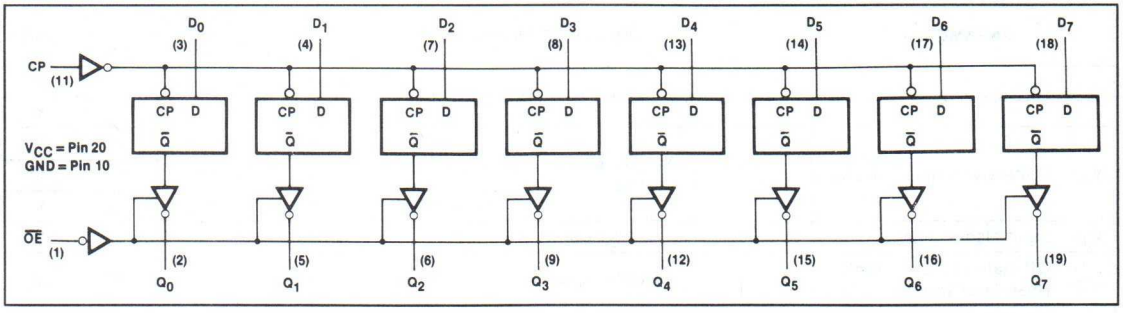


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP 54/74LS364

LOGIC DIAGRAM



3

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Latch register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0	mA
		Com'l			−2.6	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS364			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	3.45			V
				Com'l	3.65			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IL} = MAX, V_O = 3.65V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX, $\overline{OE}$ = 4.5V				42	70	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			C_L = 45pF, R_L = 667Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		33 34	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28	ns
t_{PZL}	Enable time to LOW level	Waveform 3		36	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		18	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		24	ns

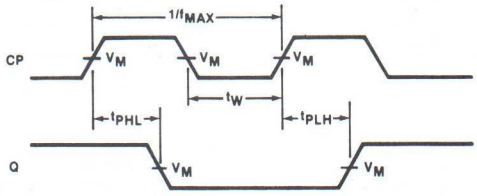
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	15		ns
t_s	Setup time, Data to clock	Waveform 4	20		ns
t_h	Hold time, Data to clock	Waveform 4	0		ns

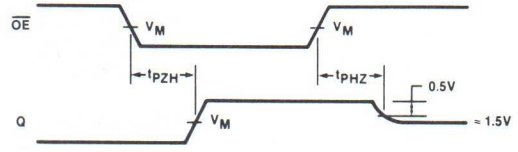
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



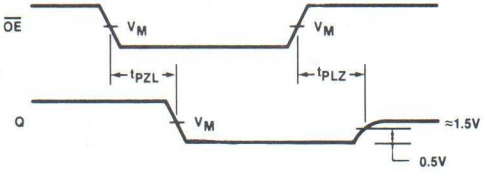
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



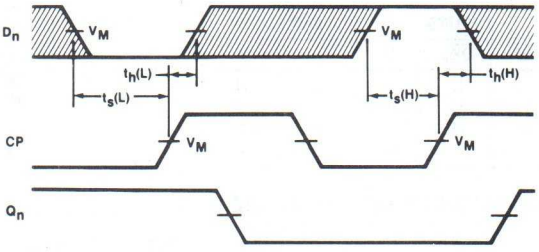
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

DATA SETUP AND HOLD TIMES



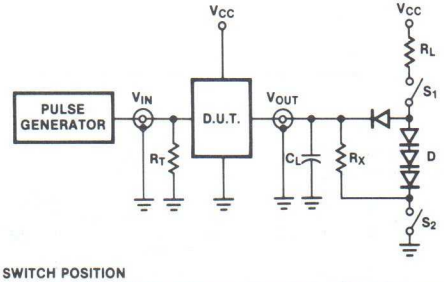
Waveform 4

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



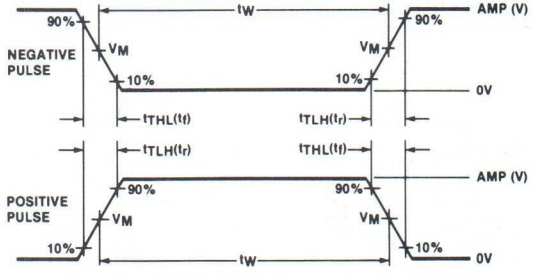
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

'365A, '367A Hex Buffer/Driver (3-State)
'366A, '368A Hex Inverter Buffer (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74365A, 367A	10ns	65mA
74LS365A, 367A	10ns	14mA
74366A, 368A	9ns	59mA
74LS366A, 368A	10ns	12mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74365AN • N74LS365AN N74366AN • N74LS366AN N74367AN • N74LS367AN N74368AN • N74LS368AN	
Ceramic DIP	N74365AF • N74LS365AF N74366AF • N74LS366AF N74367AF • N74LS367AF N74368AF • N74LS368AF	S54365AF • S54LS365AF S54366AF • S54LS366AF S54367AF • S54LS367AF S54368AF • S54LS368AF
Flatpack		S54365AW • S54LS365AW S54366AW • S54LS366AW S54367AW • S54LS367AW S54368AW • S54LS368AW

FUNCTION TABLE, '365A, '366A

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

FUNCTION TABLE, '367A, '368A

INPUTS		OUTPUTS	
$\overline{OE}$	I	Y	$\overline{Y}$
L	L	L	H
L	H	H	L
H	X	(Z)	(Z)

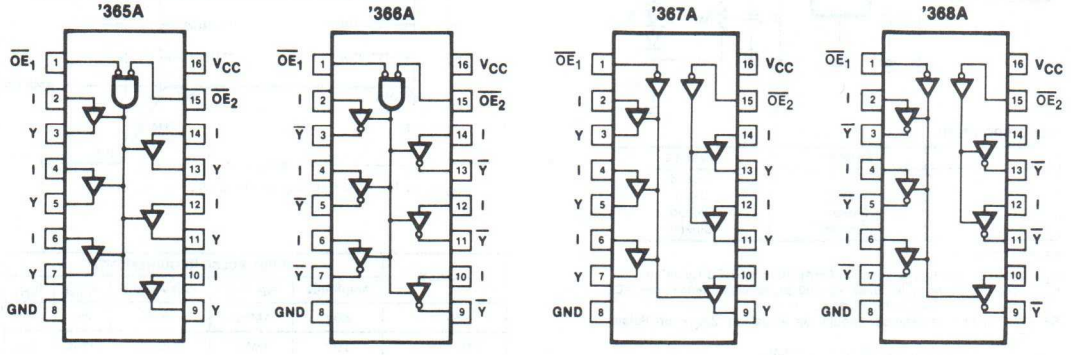
L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

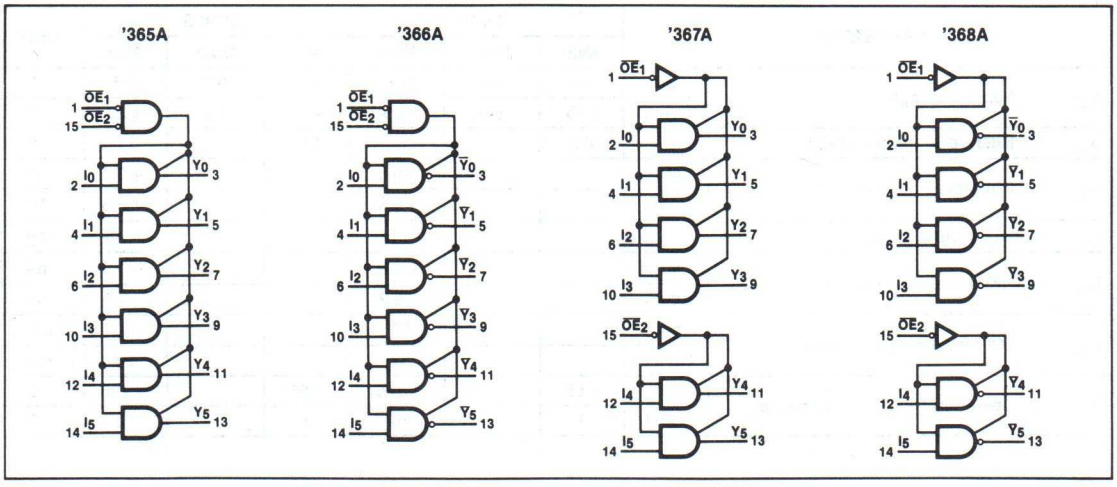
PINS	DESCRIPTION	54/74	54/74LS
All	Inputs	1ul	1LSul
All	Outputs	20ul	30LSul

NOTE
Where a 54/74 unit load (ul) is understood to be 40μA I_{IH} and −1.6mA I_{IL} and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

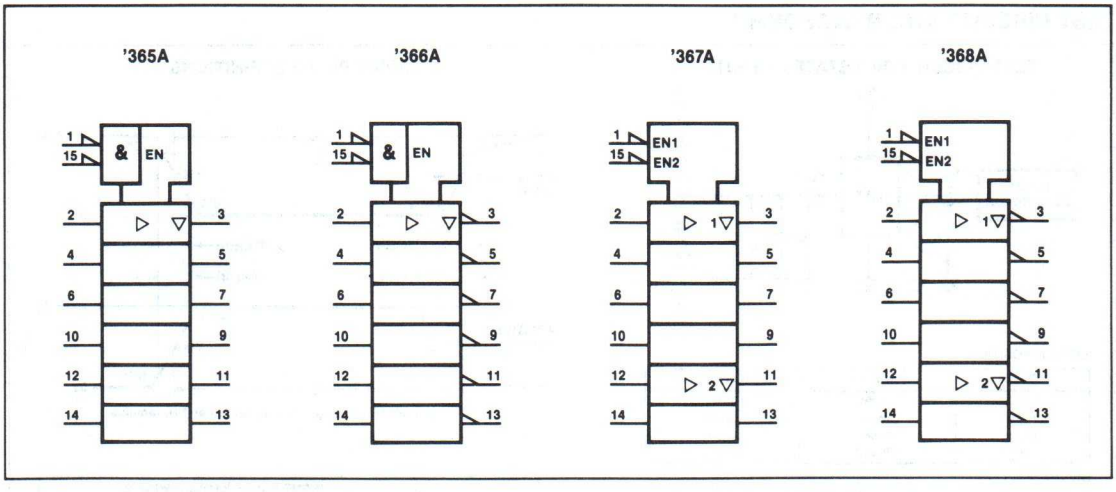
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

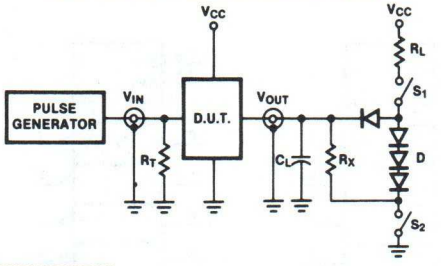
	PARAMETER	54	54LS	74	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +1	−30 to +5	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74			54/74LS			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8			+0.7	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−12			−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0			−1.0	mA
		Com'l			−5.2			−2.6	mA
I_{OL}	LOW-level output current	Mil			32			12	mA
		Com'l			32			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



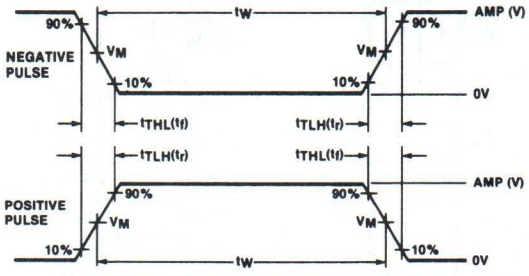
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74365A, '366A, '367A, '368A			54/74LS365A, '366A, '367A, '368A			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.3		2.4	3.3		V
				Com'l	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.4		0.25	0.4	V
				Com'l			0.4		0.35	0.5	V
			I_{OL} = 12mA	74LS					0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 2.4V					40			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					-40			-20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V				1.0				mA
			V_I = 7.0V							0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX	V_I = 2.4V				40				μA
			V_I = 2.7V							20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	I inputs, V_I = 0.5V Either $\overline{OE}$ input at 2.0V Does not apply to 'LS365A or 'LS367A				-40			-20	μA
			I inputs V_I = 0.4V Both $\overline{OE}$ inputs at 0.4V				-1.6			-0.4	mA
			$\overline{OE}$ inputs V_I = 0.4V				-1.6			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-30		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	'365A, '367A			65	85		14	24	mA
			'366A, '368A			59	77		12	21	mA

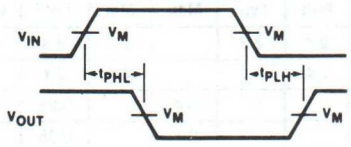
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with Data inputs grounded and Output Enable inputs at 4.5V.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS		54/74 C_L = 50pF, R_L = 400Ω		54LS/74LS C_L = 45pF, R_L = 667Ω		UNIT
				Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveform 1, '366A, '368A			17 16		15 18	ns
t_{PLH} t_{PHL}	Propagation delay	Waveform 2, '365A, '367A			16 22		16 22	ns
t_{PZH}	Enable to HIGH	Waveform 3			35		35	ns
t_{PZL}	Enable to LOW	Waveform 4	'365A, '367A		37		40	ns
			'366A, '368A		37		45	ns
t_{PHZ}	Disable from HIGH	Waveform 3, C_L = 5pF	'365A, '367A		11		30	ns
			'366A, '368A		11		32	ns
t_{PLZ}	Disable from LOW	Waveform 4, C_L = 5pF			27		35	ns

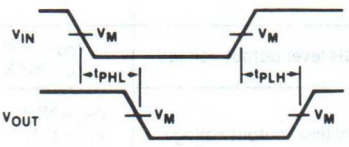
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



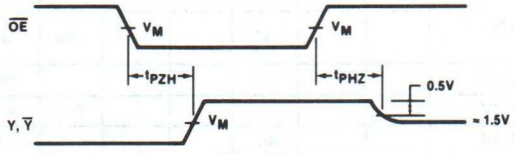
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



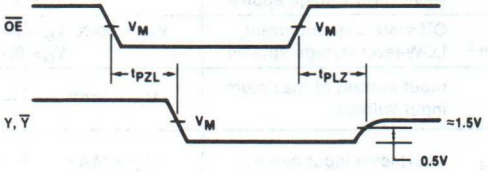
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

'373 Octal Transparent Latch With 3-State Outputs
'374 Octal D Flip-Flop With 3-State Outputs

- 8-bit transparent latch — '373
- 8-bit positive, edge-triggered register — '374
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS373	19ns	24mA
74S373	10ns	105mA
74LS374	19ns	27mA
74S374	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic	N74LS373N • N74S373N N74LS374N • N74S374N	
Ceramic DIP	N74LS373F • N74S373F N74LS374F • N74S374F	S54LS373F • S54S373F S54LS374F • S54S374F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S	54/74LS
All	Inputs	1Sul	1LSul
All	Outputs	10Sul	30LSul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}, and a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

The '373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

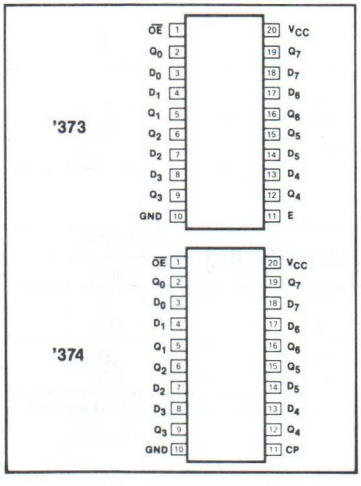
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

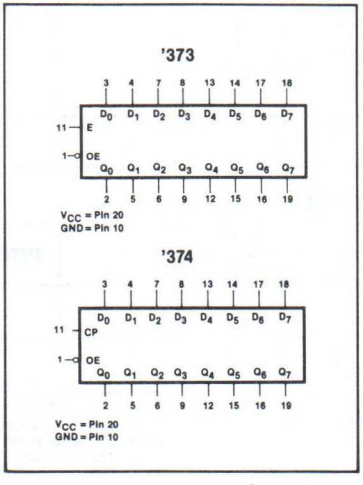
The '374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

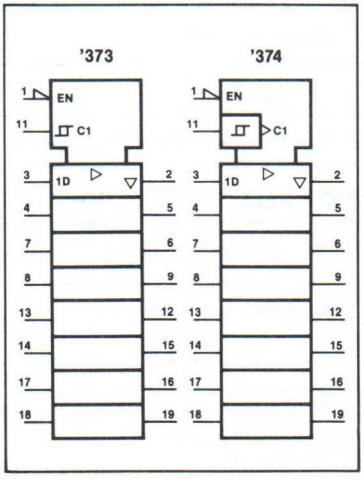
PIN CONFIGURATION



LOGIC SYMBOL

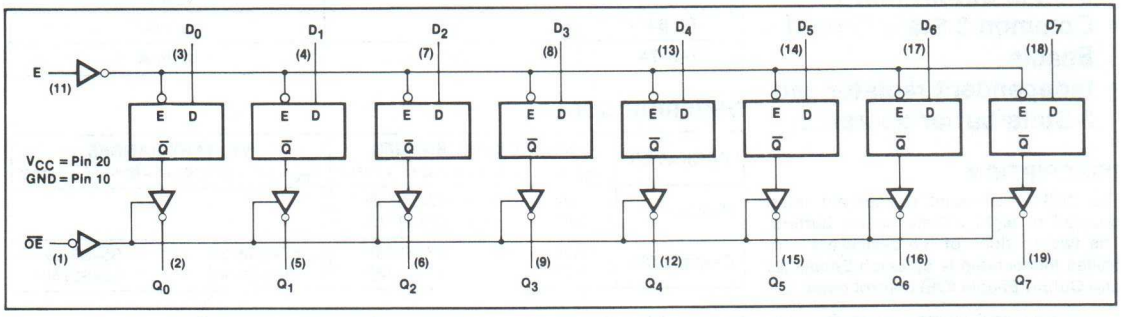


LOGIC SYMBOL (IEEE/IEC)

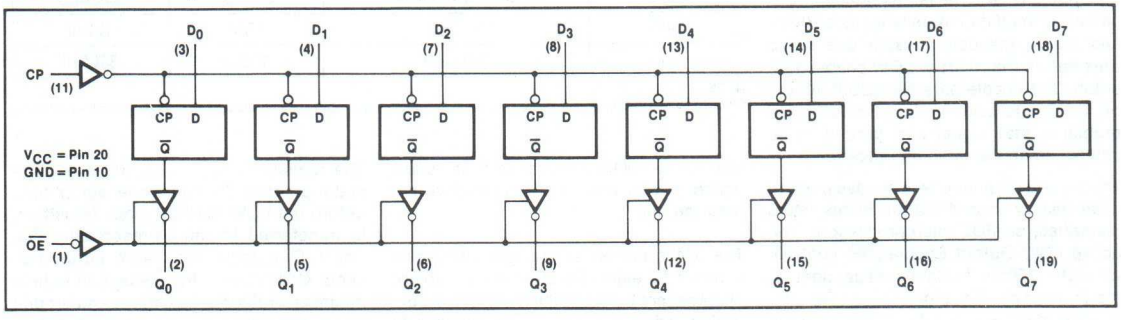


The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, '373



LOGIC DIAGRAM, '374



MODE SELECT—FUNCTION TABLE, '373

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

MODE SELECT—FUNCTION TABLE, '374

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW $\overline{OE}$ transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	54S	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +5.5	−0.5 to +7.0	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +1	−30 to +5	−30 to +1	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125		0 to 70		°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			54/74S			UNIT
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7			+0.8	V
		Com'l			+0.8			+0.8	V
I_{IK}	Input clamp current				−18			−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0			−2.0	mA
		Com'l			−2.6			−6.5	mA
I_{OL}	LOW-level output current	Mil			12			20	mA
		Com'l			24			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	−55		+125	°C
		Com'l	0		70	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS373, 374			54/74S373, 374			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		2.4	3.0		V
				Com'l	2.4	3.1		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4			0.5[4]	V
				Com'l		0.35	0.5			0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4				V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5			– 1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.7V				20				μA
			V_O = 2.4V							50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 0.4V				– 20				μA
			V_O = 0.5V							– 50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V				0.1				mA
			V_I = 5.5V							1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.4V				– 0.4				mA
			V_I = 0.5V							– 0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 30		– 130	– 40		– 100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCZ}	$\overline{OE}$ = 4.5V	'LS373		24	40				mA
			I_{CCL}	$\overline{OE}$ = 0V	'S373				105	160	mA
			I_{CCZ}	$\overline{OE}$ = 4.5V	'LS374		27	40			mA
			I_{CCL}	All inputs grounded	'S374				102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.5V, D inputs = GND	'S374				131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = + 0.45V MAX for 54S at T_A = + 125°C only.

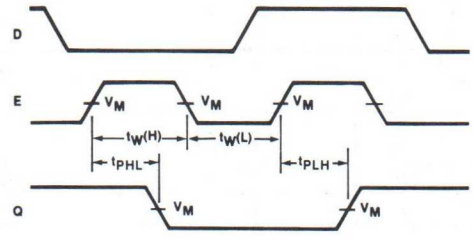
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 15pF, R_L = 280Ω		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 6, '374	35		75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, '373		30 30		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, '373		18 18		12 12	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, '374		28 28		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		28		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3, '373 '374		36 28		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		20		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		25		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

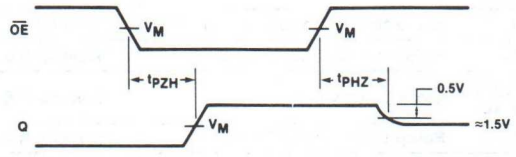
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



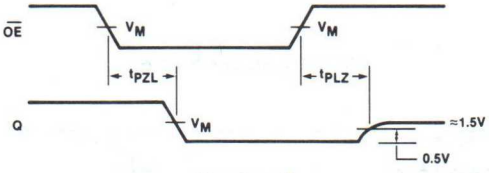
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



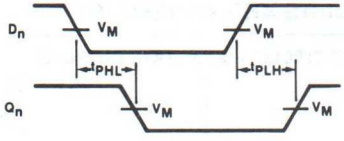
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



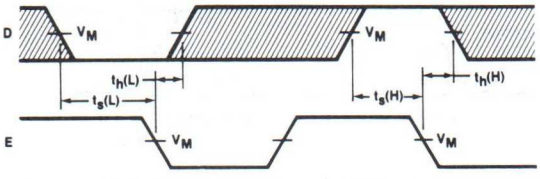
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



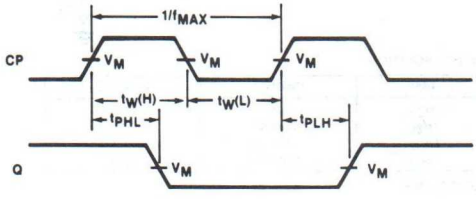
Waveform 4

DATA SETUP AND HOLD TIMES



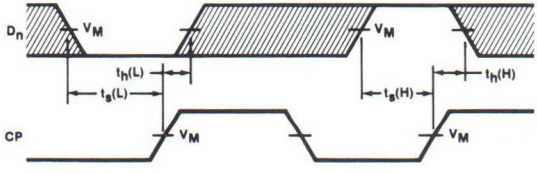
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

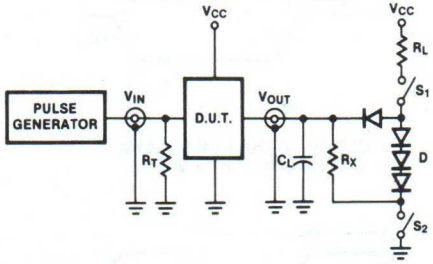
V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54/74LS		54/74S		UNIT
			Min	Max	Min	Max	
$t_W(H)$ $t_W(L)$	Latch Enable pulse width	Waveform 1, '373	15 15		6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, '373	5		0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, '373	20		10		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, '374	15 15		6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, '374	20		5		ns
t_h	Hold time, Data to Clock	Waveform 7, '374	0		2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



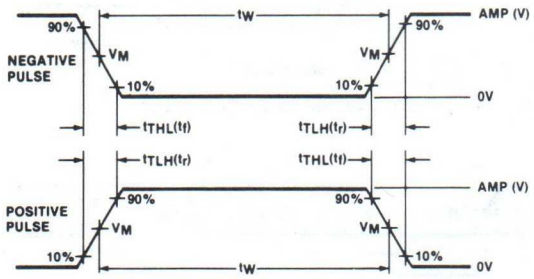
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

LATCH 54/74LS375

Quad Bistable Latch

- **Quad transparent latch**
- **Complementary outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS375	12ns	6.3mA

DESCRIPTION

The '375 has two independent 2-bit transparent latches. Each 2-bit latch is controlled by an active HIGH Enable input (E). When E is HIGH, the data enters the latch and appears at the Q output. The Q outputs follow the Data inputs as long as E is HIGH. The data on the D inputs one setup time before the HIGH-to-LOW transition of the enable will be stored in the latch. The latched output remains stable as long as the enable is LOW.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS375N	
Ceramic DIP	N74LS375F	S54LS375F
Flatpack		S54LS375W

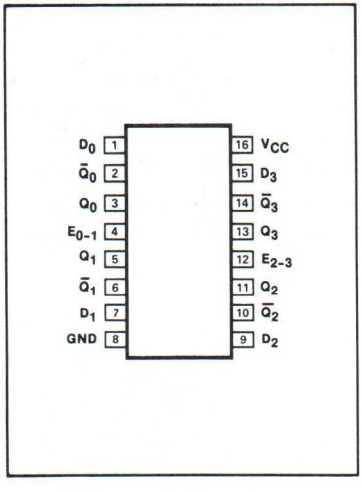
3

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

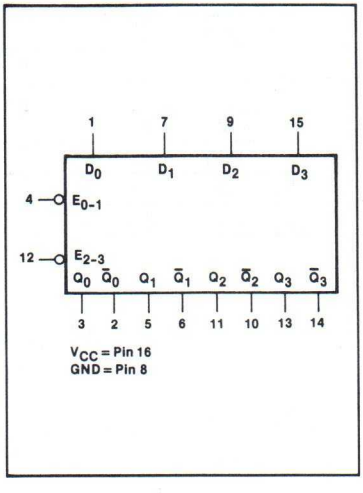
PINS	DESCRIPTION	54/74LS
D_0–D_3	Inputs	1LSul
E_{0-1}, E_{2-3}	Inputs	4LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

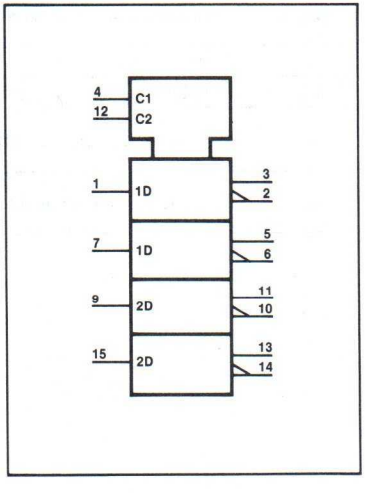
PIN CONFIGURATION



LOGIC SYMBOL

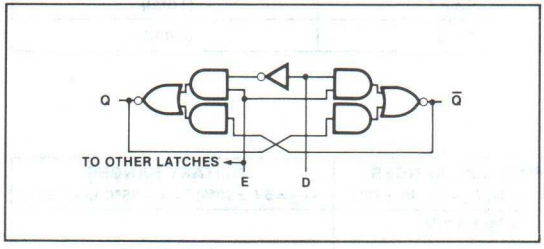


LOGIC SYMBOL (IEEE/IEC)



LATCH 54/74LS375

LOGIC DIAGRAM (Each Latch)



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS		OUTPUTS	
	E	D	Q	$\overline{Q}$
Data Enabled	H H	L H	L H	H L
Data Latched	L	X	q	$\overline{q}$

H = HIGH voltage level
L = LOW voltage level
X = Don't care
q = Lower case letters indicate the state of referenced output one setup time prior to the HIGH-to-LOW Enable transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS375 Min	54/74LS375 Typ[2]	54/74LS375 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.5		V
				Com'l	2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	D_0–D_3 inputs				0.1	mA
			E_{0-1}, E_{2-3} inputs				0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	D_0–D_3 inputs				20	μA
			E_{0-1}, E_{2-3} inputs				80	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	D_0–D_3 inputs				– 0.4	mA
			E_{0-1}, E_{2-3} inputs				– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				6.3	12	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Test I_{CC} with all inputs grounded and all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

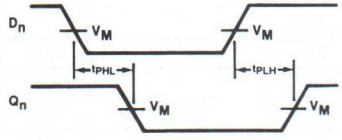
PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ Min	54LS/74LS C_L = 15pF, R_L = 2kΩ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Data to Q output	Waveform 1		27 17	ns
t_{PLH} t_{PHL}	Propagation delay Data to $\overline{Q}$ output	Waveform 2		20 15	ns
t_{PLH} t_{PHL}	Propagation delay Enable to Q output	Waveform 3		27 25	ns
t_{PLH} t_{PHL}	Propagation delay Enable to $\overline{Q}$ output	Waveform 3		30 15	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	Enable pulse width	Waveform 3	20		ns
t_s	Setup time, Data to Enable	Waveform 4	20		ns
t_h	Hold time, Data to Enable	Waveform 4	0		ns

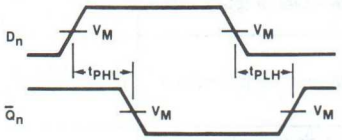
AC WAVEFORMS

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 1

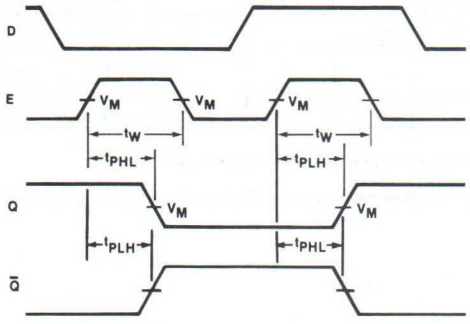
PROPAGATION DELAY DATA TO $\overline{Q}$ OUTPUTS



Waveform 2

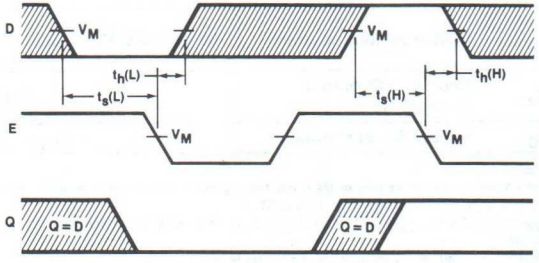
V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



Waveform 3

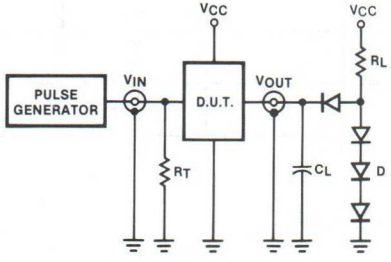
DATA SETUP AND HOLD TIMES



Waveform 4

TEST CIRCUITS AND WAVEFORMS

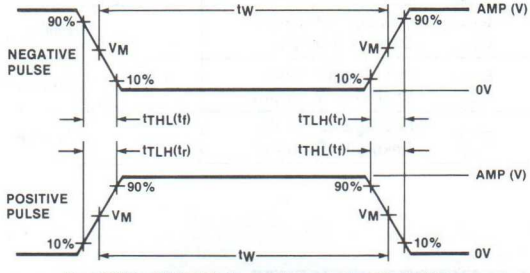
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP 54/74LS377

Octal D Flip-Flop With Clock Enable

- **Ideal for addressable register applications**
- **Clock Enable for address and data synchronization applications**
- **Eight edge-triggered D flip-flops**
- **Buffered common clock**
- **Slim 20-pin plastic and ceramic DIP packages**
- **See '273 for Master Reset version**
- **See '373 for transparent latch version**
- **See '374 for 3-state version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS377	40MHz	20mA

3

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS377N	
Ceramic DIP	N74LS377F	S54LS377F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

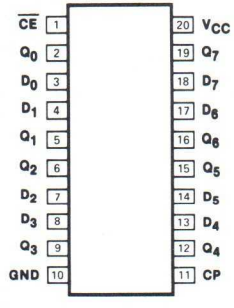
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

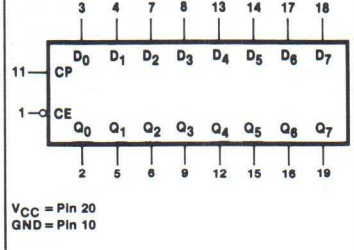
The '377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

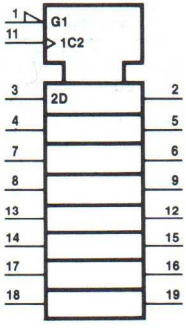
PIN CONFIGURATION



LOGIC SYMBOL

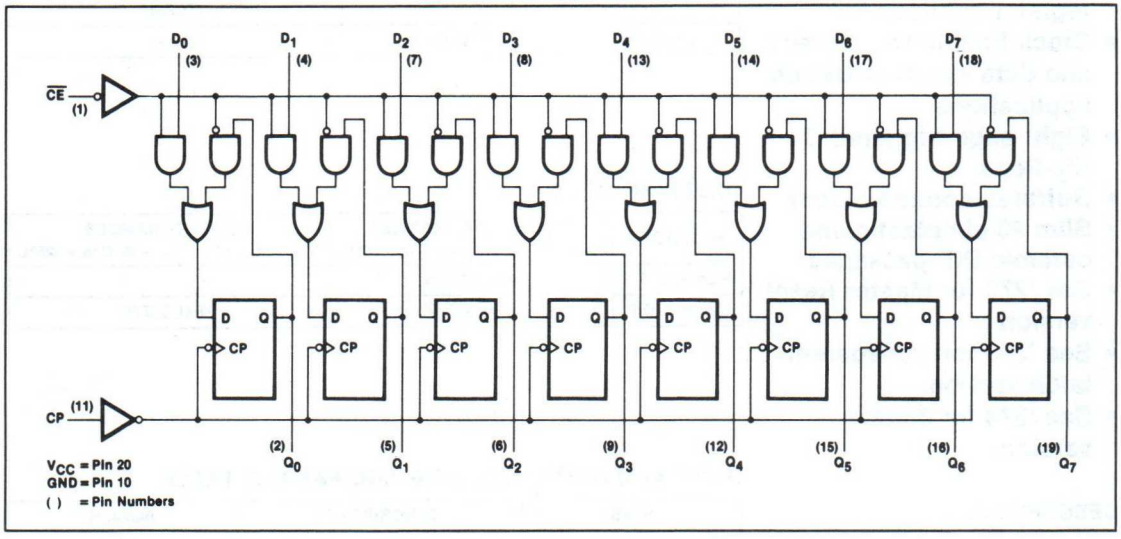


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP 54/74LS377

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS377			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.5		V
				Com'l	2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		18	28	mA
			I_{CCL}	Outputs LOW		22	35	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With all outputs open.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			C_L = 15pF, R_L = 2kΩ		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27	ns

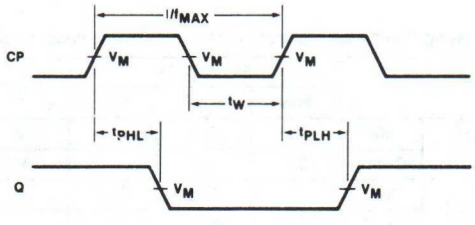
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
$t_W(L)$	Clock pulse width (LOW)	Waveform 1	20		ns
t_s	Setup time, Data to CP	Waveform 2	20		ns
t_h	Hold time, Data to CP	Waveform 2	5		ns
t_s	Setup time, $\overline{CE}$ to CP	Waveform 2	20		ns
t_h	Hold time, $\overline{CE}$ to CP	Waveform 2	5		ns

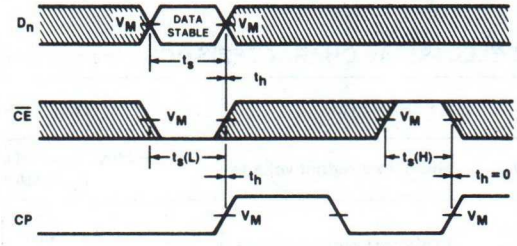
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA AND CLOCK ENABLE SETUP AND HOLD TIMES

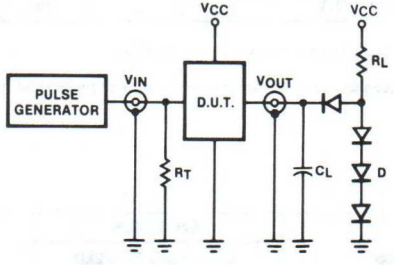


Waveform 2

V_M = 1.5V for 54/74 and 54/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

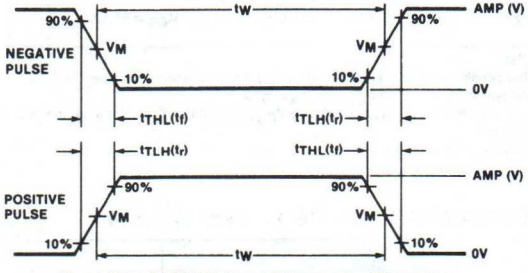
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP 54/74LS378

Hex D Flip-Flop With Clock Enable

- **Ideal for addressable register applications**
- **Six edge-triggered D flip-flops**
- **Buffered common clock**
- **Clock Enable for address and data synchronization applications**
- **See '174 for Master Reset version**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS378	40MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS378N	
Ceramic DIP	N74LS378F	S54LS378F
Flatpack		S54LS378W

DESCRIPTION

The '378 has six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ($\overline{CE}$) is low.

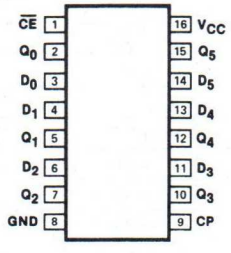
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input is also edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

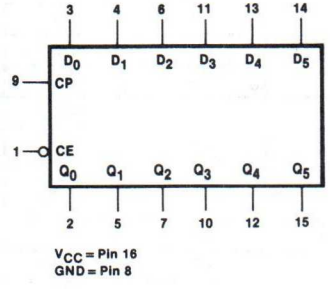
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

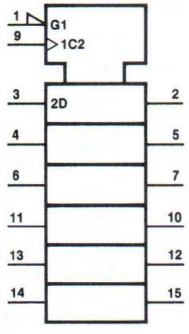
PIN CONFIGURATION



LOGIC SYMBOL

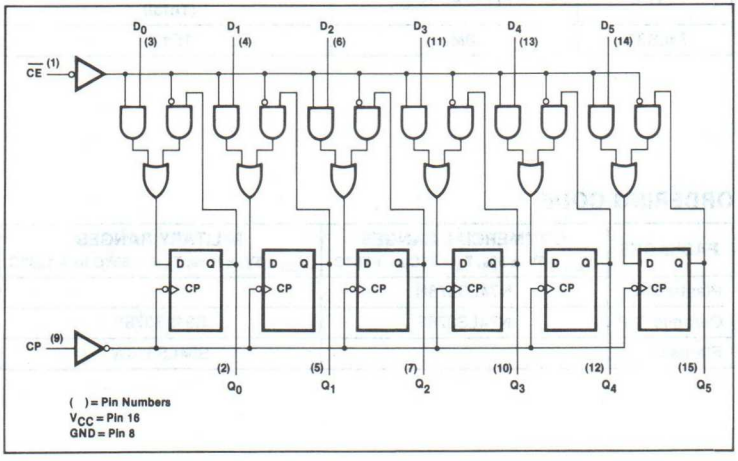


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP 54/74LS378

LOGIC DIAGRAM



MODE SELECT— FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	CP	$\overline{CE}$	D_n	Q_n
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (do nothing)	↑	h	X	no change
	X	H	X	no change

H = HIGH voltage level steady state.
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care.
↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to $+V_{CC}$	−0.5 to $+V_{CC}$	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	mA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

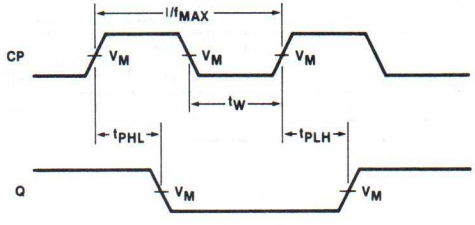
DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS378			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.5		V
				Com'l	2.7	3.5		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				15	24	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. With ground applied to all data inputs and the Clock Enable input and all outputs open, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

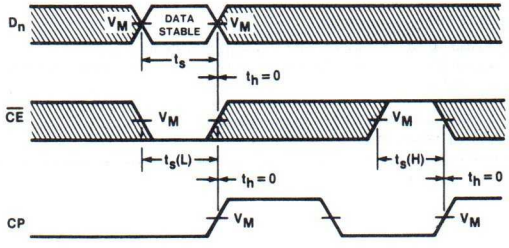
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

DATA AND CLOCK ENABLE SETUP AND HOLD TIMES



Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		27 27	ns

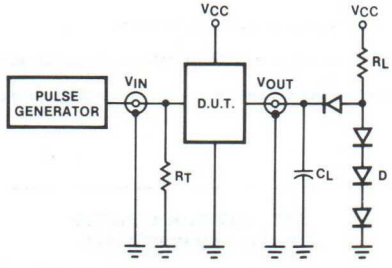
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER			TEST CONDITIONS	54LS/74LS		UNIT
				Min	Max	
$t_W(L)$	Clock pulse width (LOW)		Waveform 1	20		ns
t_s	Setup time, Data to CP		Waveform 2	20		ns
t_h	Hold time, Data to CP		Waveform 2	5		ns
t_s	Setup time, $\overline{CE}$ to CP	Active state	Waveform 2	25		ns
		Inactive state		10		ns
t_h	Hold time, $\overline{CE}$ to CP		Waveform 2	5		ns

TEST CIRCUITS AND WAVEFORMS

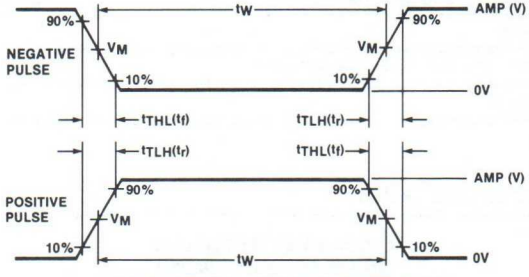
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

COUNTER 54/74LS390

Dual Decade Ripple Counter

- **Two BCD decade or bi-quinary counters**
- **One package can be configured to divide-by-2, 4, 5, 10, 20, 25, 50 or 100**
- **Two Master Resets to clear each decade counter individually**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS390	55MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS390N	
Ceramic DIP	N74LS390F	

DESCRIPTION

The '390 is a dual 4-bit decade ripple counter divided into four separately clocked sections. The counter has two divide-by-two sections and two divide-by-five sections. These sections are normally used in a BCD decade or a bi-quinary configuration, since they share a common Master Reset input. If the two Master Resets can be used to simultaneously clear all 8 bits of the counter, a number of counting configurations are possible within one package. The separate clocks of each section allow ripple counter or frequency division applications of divide-by-2, 4, 5, 10, 20, 25, 50 or 100.

Each section is triggered by the HIGH-to-LOW transition of the Clock ($\overline{CP}$) inputs. For BCD decade operation, the Q_0 output is connected to the $\overline{CP}_1$ input of the divide-by-five section. For bi-quinary decade operation (50% duty cycle output), the Q_3 output is connected to the CP_0 input, and Q_0 becomes the decade output.

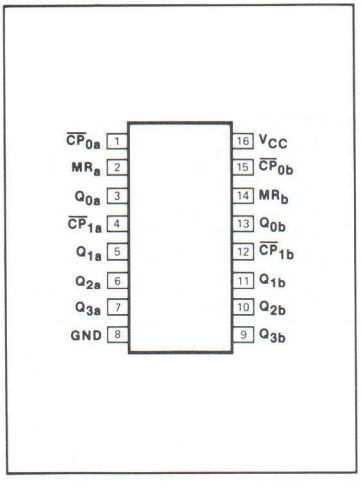
The Master Resets (MR_a and MR_b) are active HIGH asynchronous inputs to each decade counter which operate on the portion of the counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clocks and sets the four outputs LOW.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

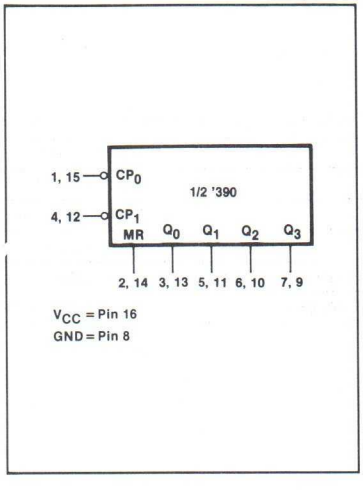
PINS	DESCRIPTION	54/74LS
MR	Inputs	1LSul
CP_0	Inputs	4LSul
CP_1	Inputs	6LSul
All	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

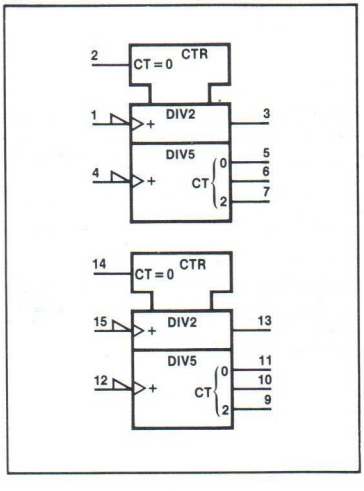
PIN CONFIGURATION



LOGIC SYMBOL

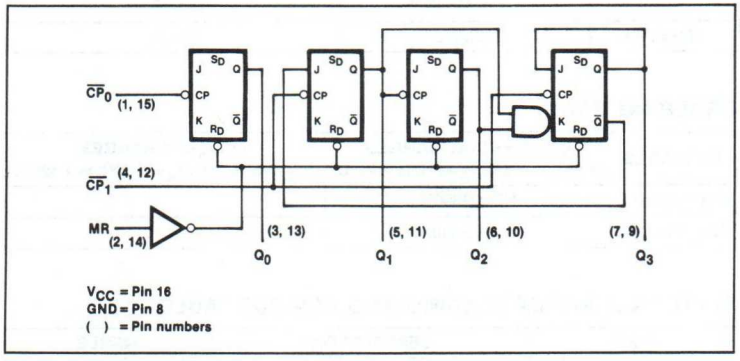


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS390

LOGIC DIAGRAM



BCD COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

H = HIGH voltage level
L = LOW voltage level

NOTE
Output Q_0 is connected to input $\overline{CP}_1$ with Counter input on $\overline{CP}_0$.

BI-QUINARY COUNT SEQUENCE FOR 1/2 THE '390

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	L	H	L	L
2	L	L	H	L
3	L	H	H	L
4	L	L	L	H
5	H	L	L	L
6	H	H	L	L
7	H	L	H	L
8	H	H	H	L
9	H	L	L	H

NOTE
Output Q_3 is connected to input $\overline{CP}_0$ with Counter input on $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on $\overline{CP}_0$ and $\overline{CP}_1$ inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current				− 400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

3

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS390			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					− 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR inputs			0.1	mA
			V_I = 5.5V	$\overline{CP}_0$ inputs			0.2	mA
				$\overline{CP}_1$ inputs			0.4	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR inputs			20	μA
				$\overline{CP}_0$ inputs			100	μA
				$\overline{CP}_1$ inputs			200	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR inputs			− 0.4	mA
				$\overline{CP}_0$ inputs			− 1.6	mA
				$\overline{CP}_1$ inputs			− 2.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			− 20		− 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				15	26	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 15pF$, $R_L = 2k\Omega$		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}_0$ input count frequency	Waveform 1	25		MHz
f_{MAX}	$\overline{CP}_1$ input count frequency	Waveform 1	12.5		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_0	Waveform 1		20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_0$ to Q_2	Waveform 1		60 60	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_1 or Q_3	Waveform 1		21 21	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}_1$ to Q_2	Waveform 1		39 39	ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns

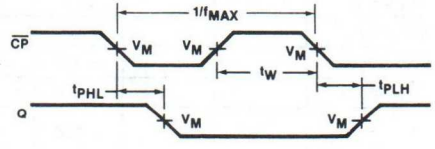
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	$\overline{CP}_0$ pulse width	Waveform 1	20		ns
t_W	$\overline{CP}_1$ pulse width	Waveform 1	40		ns
t_W	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

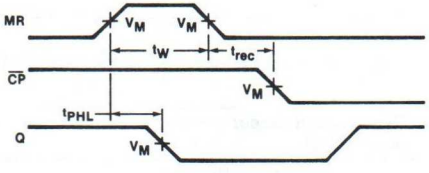
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS

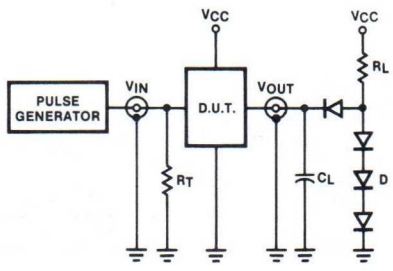


Waveform 2

$V_M = 1.5V$ for 54/74LS and 54S/74S; $V_M = 1.3V$ for 54LS/74LS.
The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Truth Table.

TEST CIRCUITS AND WAVEFORMS

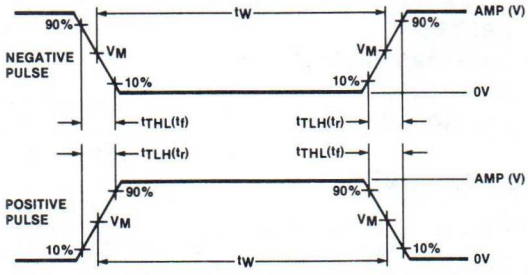
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

COUNTER 54/74LS393

Dual 4-Bit Binary Ripple Counter

- **Two 4-bit binary counters**
- **Divide-by any binary module up to 28 in one package**
- **Two Master Resets to clear each 4-bit counter individually**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS393	35MHz	15mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74LS393N	
Ceramic DIP	N74LS393F	S54LS393F
Flatpack		S54LS393W

DESCRIPTION

The '393 is a Dual 4-Bit Binary Ripple Counter with separate Clock and Master Reset inputs to each counter. The operation of each half of the '393 is the same as the '93 except no external clock connections are required. The counters are triggered by a HIGH-to-LOW transition of the Clock ($\overline{CP}_a$ and $\overline{CP}_b$) inputs. The counter outputs are internally connected to provide Clock inputs to succeeding stages. The outputs of the ripple counter do not change synchronously and should not be used for high speed address decoding.

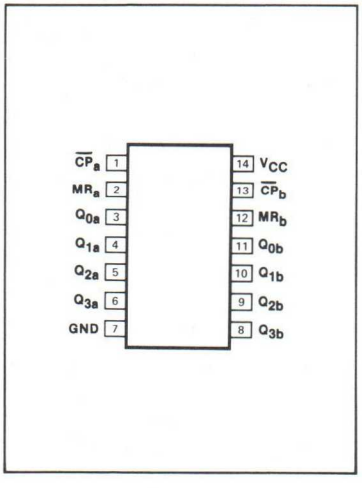
The Master Resets (MR_a and MR_b) are active-HIGH asynchronous inputs to each 4-bit counter identified by the "a" and "b" suffixes in the Pin Configuration. A HIGH level on the MR input overrides the clock and sets the outputs LOW.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

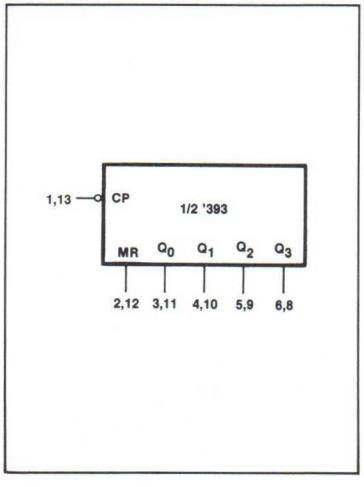
PINS	DESCRIPTION	54/74LS
MR	Master Reset input	1LSul
$\overline{CP}$	Clock input	4LSul
Q	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

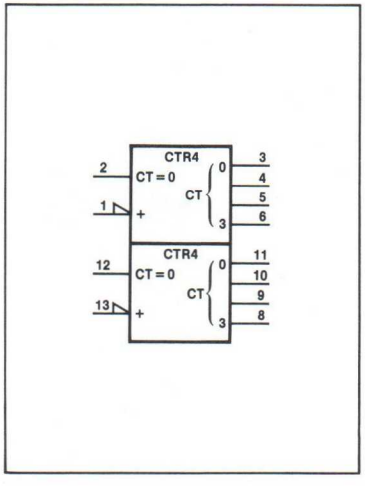
PIN CONFIGURATION



LOGIC SYMBOL

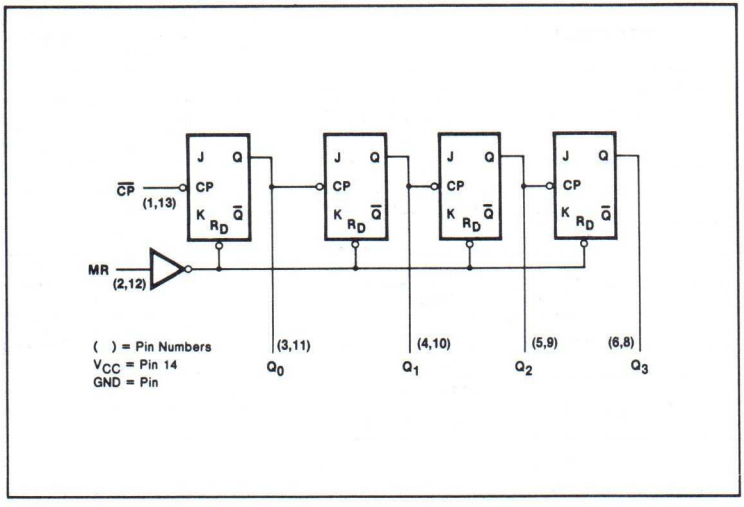


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS393

LOGIC DIAGRAM



COUNT SEQUENCE FOR 1/2 THE '393

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

H = HIGH voltage level
L = LOW voltage level

3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to +5.5V on $\overline{CP}$ input only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	mA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

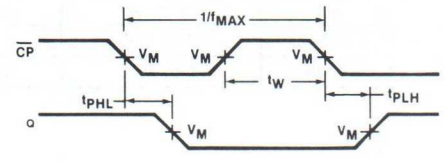
COUNTER 54/74LS393

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

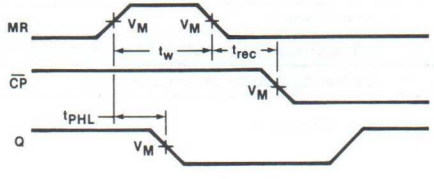
PARAMETER		TEST CONDITIONS[1]			54/74LS393			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR input			0.1	mA
			V_I = 5.5V	$\overline{CP}$ input			0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR input			20	μA
				$\overline{CP}$ input			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR input			– 0.4	mA
				$\overline{CP}$ input			– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				15	26	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with both MR inputs grounded following momentary connection to 4.5V, all other inputs grounded and all outputs open.

AC WAVEFORMS



Waveform 1



Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The number of clock pulses required between the t_{PLH} and t_{PHL} measurements can be determined from the appropriate Function Table.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ		UNIT
			Min	Max	
f_{MAX}	$\overline{CP}$ input count frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1		20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_3	Waveform 1		60 60	ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

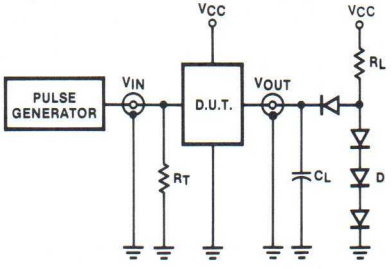
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	$\overline{CP}$ pulse width	Waveform 1	20		ns
t_W	MR pulse width	Waveform 2	20		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns

3

TEST CIRCUITS AND WAVEFORMS

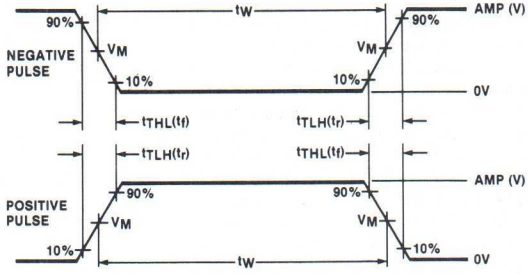
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

SHIFT REGISTER 54/74LS395A

4-Bit Cascadable Shift Register With 3-State Outputs

- 4-bit parallel load shift register
- Independent 3-state buffer outputs
- Separate Q_3 output for serial expansion
- Asynchronous Master Reset

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS395A	45MHz	19mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS395AN	
Ceramic DIP	N74LS395AF	S54LS395AF
Flatpack		S54LS395AW

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
Q_0-Q_3	Outputs	30LSul
Q'_3	Output	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

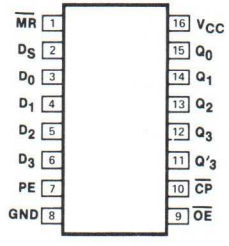
DESCRIPTION

The '395 is a 4-Bit Shift Register with serial and parallel synchronous operating modes and four 3-state buffer outputs. The shifting and loading operations are controlled by the state of the Parallel Enable (PE) input. When PE is HIGH, data is loaded from the Parallel Data inputs (D_0-D_3) into the register synchronous with the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). When PE is LOW, the data at the Serial Data input (D_S) is loaded into the Q_0 flip-flop, and the data in the register is shifted one bit to the right in the direction ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$) synchronous with the negative clock transition. The PE and Data inputs are fully edge-triggered and must be stable only one setup prior to the HIGH-to-LOW transition of the clock.

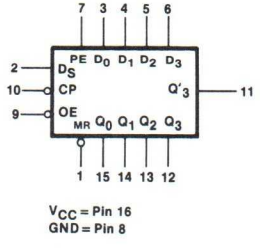
The Master Reset ($\overline{MR}$) is an asynchronous active-LOW input. When LOW, the $\overline{MR}$ overrides the clock and all other inputs and clears the register.

The 3-state output buffers are designed to drive heavily loaded 3-state buses, or large capacitive loads. The active-LOW Output Enable ($\overline{OE}$) controls all four 3-state buffers independent of the register operation. The data in the register appears at the outputs when $\overline{OE}$ is LOW. The outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus when $\overline{OE}$ is HIGH. The output from the last stage is brought out separately. This output (Q'_3) is tied to the Serial Data input (D_S) of the next register for serial expansion applications. The Q'_3 output is not affected by the 3-state buffer operation.

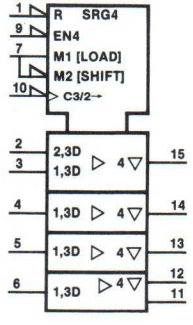
PIN CONFIGURATION



LOGIC SYMBOL

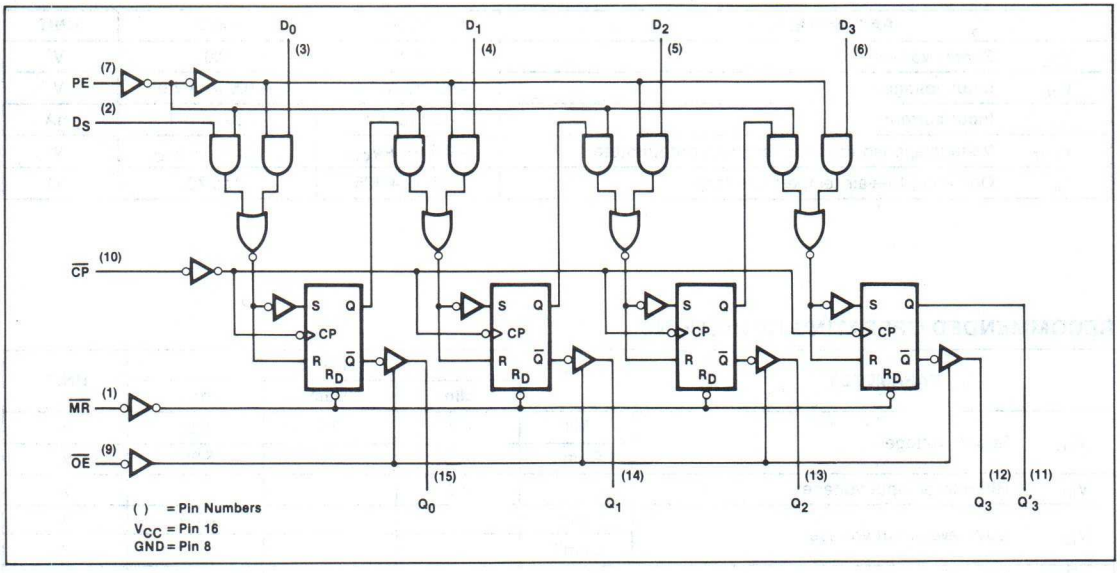


LOGIC SYMBOL (IEEE/IEC)



SHIFT REGISTER 54/74LS395A

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS			
	$\overline{MR}$	$\overline{CP}$	PE	D_S	D_n	Q_0	Q_1	Q_2	Q_3
Reset (clear)	L	X	X	X	X	L	L	L	L
Shift right	H	↓	l	l	X	L	q_0	q_1	q_2
	H	↓	l	h	X	H	q_0	q_1	q_2
Parallel load	H	↓	h	X	l	L	L	L	L
	H	↓	h	X	h	H	H	H	H

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS	
	$\overline{OE}$	Q_n (Register)	Q_0, Q_1, Q_2, Q_3	Q'_3
Read	L	L	L	L
	L	H	H	H
Disable buffers	H	L	(Z)	L
	H	H	(Z)	H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW clock transition
q_n = Lower case letters indicate the state of the referenced output one setup time prior to the HIGH-to-LOW clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↓ = HIGH-to-low transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER				54/74LS			UNIT
				Min	Nom	Max	
V_{CC}	Supply voltage		Mil	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			V
V_{IL}	LOW-level input voltage		Mil			+0.7	V
			Com'l			+0.8	V
I_{IK}	Input clamp current					−18	mA
I_{OH}	HIGH-level output current	Q_3'				−400	μA
		Q_0–Q_3	Mil			−1.0	mA
			Com'l			−2.6	mA
I_{OL}	LOW-level output current	Q_3'	Mil			4	mA
			Com'l			8	mA
		Q_0–Q_3	Mil			12	mA
			Com'l			24	mA
T_A	Operating free-air temperature		Mil	−55		+125	°C
			Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS395A Min	54/74LS395A Typ[2]	54/74LS395A Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX	Q_3'	Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
			Q_0, Q_1, Q_2, Q_3		2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	Q_3'	I_{OL} = MAX, Mil		0.25	0.4	V
				I_{OL} = MAX, Com'l		0.35	0.5	V
				I_{OL} = 4mA, 74LS		0.25	0.4	V
			Q_0, Q_1, Q_2, Q_3	I_{OL} = MAX, Mil		0.25	0.4	V
				I_{OL} = MAX, Com'l		0.35	0.5	V
				I_{OL} = 12mA, 74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MIN, V_{IH} = MIN, V_O = 2.7V	Q_0, Q_1, Q_2, Q_3				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MIN, V_{IH} = MIN, V_O = 0.4V	Q_0, Q_1, Q_2, Q_3				− 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					− 0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Q_3'		− 20		− 100	mA
			Q_0, Q_1, Q_2, Q_3		− 30		− 130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	Condition 1			19	34	mA
			Condition 2			19	31	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with D_S and Master Reset at 4.5V. The Data inputs grounded and outputs open under the following conditions: *Condition 1:* $\overline{OE}$ at 4.5V. A momentary 3V, then ground, applied to $\overline{CP}$. *Condition 2:* Ground $\overline{OE}$ and $\overline{CP}$ inputs.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 45pF, R_L = 667Ω Min	54LS/74LS C_L = 45pF, R_L = 667Ω Max	UNIT
f_{MAX}	Maximum Clock frequency	Waveform 1	30		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to Buffer outputs	Waveform 1		30 30	ns
t_{PLH} t_{PHL}	Propagation delay Clock to Q_3' output	Waveform 1, R_L = 2kΩ, C_L = 15pF		30 30	ns
t_{PHL}	Propagation delay, $\overline{MR}$ to output	Waveform 2		35	ns
t_{PZH}	Enable time to HIGH level	Waveform 3		25	ns
t_{PZL}	Enable time to LOW level	Waveform 4		25	ns
t_{PHZ}	Disable time from HIGH level	Waveform 3, C_L = 5pF		17	ns
t_{PLZ}	Disable time from LOW level	Waveform 4, C_L = 5pF		20	ns

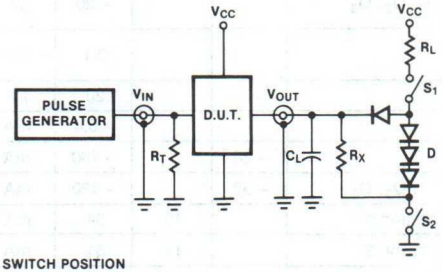
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	16		ns
t_W	Master Reset pulse width	Waveform 2	25		ns
t_s	Setup time, Data to clock	Waveform 5	20		ns
t_h	Hold time, Data to clock	Waveform 5	10		ns
t_s	Setup time, PE to clock	Waveform 5	40		ns
t_h	Hold time, PE to clock	Waveform 5	10		ns
t_{rec}	Recovery time, $\overline{MR}$ to clock	Waveform 2	30		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



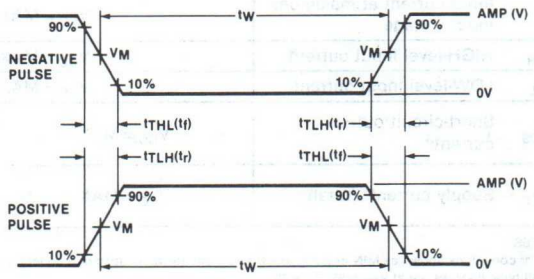
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH} t_{THL} Values should be less than or equal to the table entries.
Q_3' is a standard totem-pole output.

INPUT PULSE DEFINITIONS

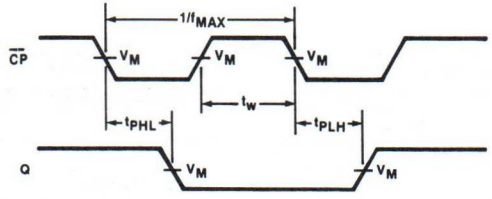


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

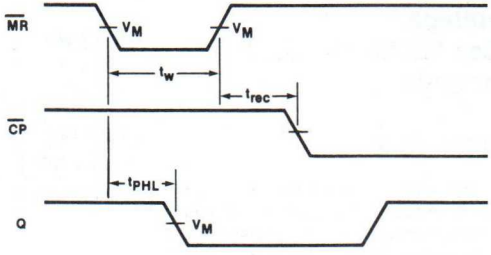
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



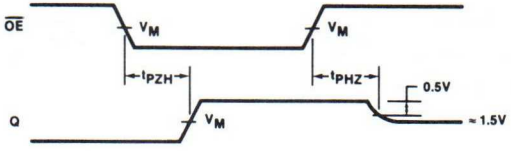
Waveform 1

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



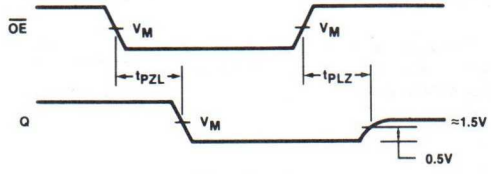
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



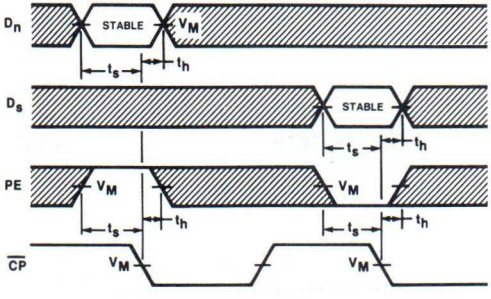
Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

PARALLEL ENABLE AND DATA SETUP AND HOLD TIMES



Waveform 5

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

DECODER/DRIVER 54/74LS445

BCD-To-Decimal Decoder/Driver (Open Collector)

- **80mA output drive capability**
- **7V output breakdown voltage**
- **See '45 for 30V output voltage**
- **See '42 for standard TTL outputs**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS445	39ns	7mA

DESCRIPTION

The '445 is a 1-of-10 decoder with open collector outputs. This decoder accepts BCD inputs on the A_0 to A_3 address lines and generates 10 mutually exclusive active LOW outputs. When an input code greater than "9" is applied, all outputs are HIGH. This device can therefore be used as a 1-of-8 decoder with A_3 used as an active LOW enable.

The '445 features an output breakdown voltage of 7V. This device is ideal as a lamp or solenoid driver.

ORDERING CODE

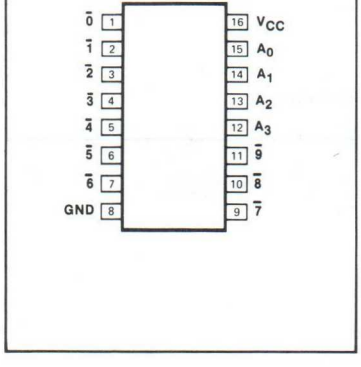
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS445N	
Ceramic DIP	N74LS445F	S54LS445F
Flatpack		S54LS445W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

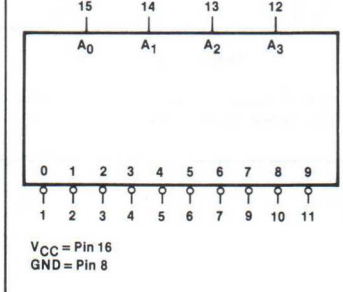
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

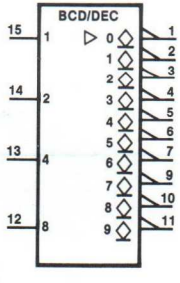
PIN CONFIGURATION



LOGIC SYMBOL

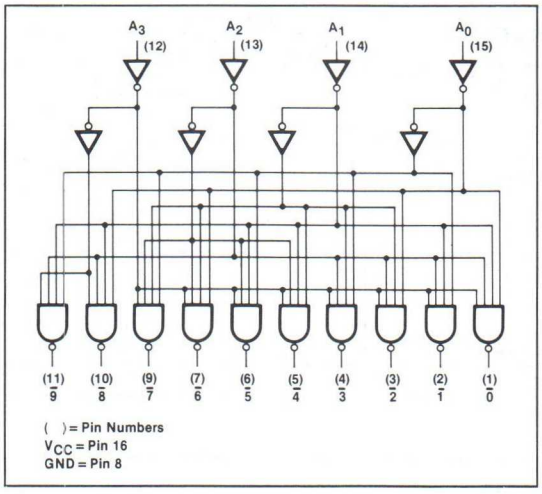


LOGIC SYMBOL (IEEE/IEC)



DECODER/DRIVER 54/74LS445

LOGIC DIAGRAM



FUNCTION TABLE

A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH voltage levels
L = LOW voltage levels

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

	PARAMETER	54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	− 0.5 to + 7.0	− 0.5 to + 7.0	V
I_{IN}	Input current	− 30 to + 1	− 30 to + 1	mA
V_{OUT}	Voltage applied to output in HIGH output state	− 0.5 to + V_{CC}	− 0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	− 55 to + 125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

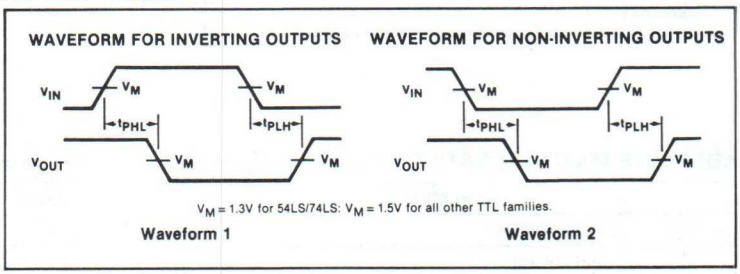
PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.7	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
V_{OH}	HIGH-level output voltage				7.0	V
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS445			UNIT
					Min	Typ[2]	Max	
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 7.0V					250	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
			I_{OL} = 80mA	74LS		1.6	3.0	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					– 0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX				7	13	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Measure I_{CC} with all inputs grounded and all outputs open.

AC WAVEFORMS

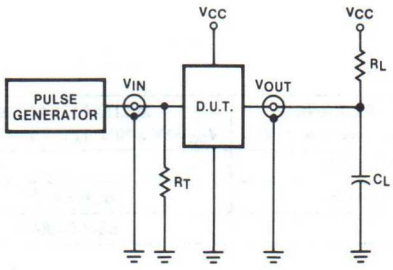


AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 45pF, R_L = 665Ω		UNIT
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveforms 1 & 2		50 50	ns

TEST CIRCUITS AND WAVEFORMS

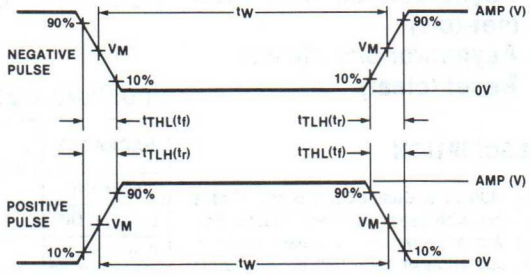
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

3

COUNTER 54/74LS490

Dual BCD Decade Ripple Counter

- **Two BCD decade counters**
- **Asynchronous Master Set (set-to-9)**
- **Asynchronous Master Reset (clear)**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS490	55MHz	15mA

DESCRIPTION

The '490 is a Dual BCD Decade Ripple Counter with separate Clock, Master Set, and Master Reset inputs to each counter. The operation of each half of the '490 is the same as the '90 used in the BCD decade mode.

The counters are triggered by the HIGH-to-LOW transition of the Clock ($\overline{CP}$) inputs. No external connections are required to get the full BCD (8421) decade counting scheme from the counters. The counter outputs are internally connected as clocks or decoded inputs to succeeding stages. Since this is a ripple type counter, the outputs do not change synchronously and should not be used for high speed address decoding.

The Master Set (MS) and Master Reset (MR) are asynchronous active-HIGH inputs. The HIGH MR input overrides the clock and clears the associated 4 bits of the counter. The HIGH MS input overrides the clock and MR inputs and sets the associated 4 bits to nine (HLLH).

ORDERING CODE

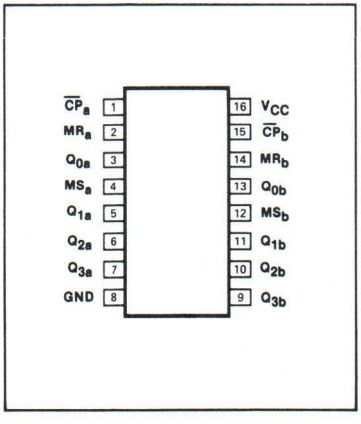
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS490N	
Ceramic DIP	N74LS490F	S54LS490F
Flatpack		S54LS490W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

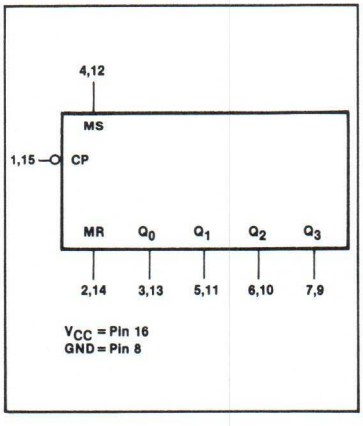
PINS	DESCRIPTION	54/74LS
$\overline{CP}$	Input	4LSul
MR, MS	Inputs	1LSul
Q_0–Q_3	Outputs	10LSul

NOTE
Where a 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

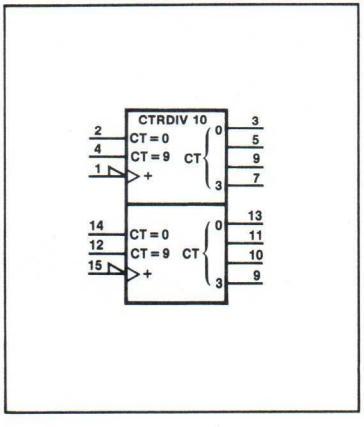
PIN CONFIGURATION



LOGIC SYMBOL

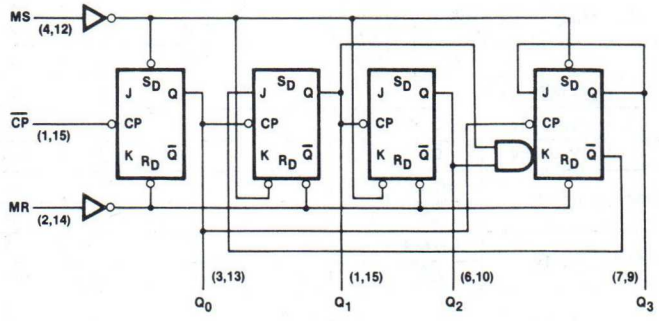


LOGIC SYMBOL (IEEE/IEC)



COUNTER 54/74LS490

LOGIC DIAGRAM



( ) = Pin Numbers
V_{CC} = Pin 16
GND = Pin 8

MODE SELECTION—FUNCTION TABLE FOR 1/2 THE '490

RESET/SET INPUTS		OUTPUTS			
MR	MS	Q_0	Q_1	Q_2	Q_3
H	L	L	L	L	L
L	H	H	L	L	H
L	L	Count			

H = HIGH voltage level
L = LOW voltage level
X = Don't care

BCD COUNT SEQUENCE FOR 1/2 THE '490

COUNT	OUTPUTS			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE
Output Q_0 connected to input $\overline{CP}_1$.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to +5.5V on $\overline{CP}$ input only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−400	μA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS490 Min	54/74LS490 Typ[2]	54/74LS490 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.5	3.4		V
				Com'l	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 7.0V	MR, MS inputs			0.1	mA
			V_I = 5.5V	$\overline{CP}$ input			0.2	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V		MR, MS inputs			20	μA
				$\overline{CP}$ input			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V		MR, MS inputs			– 0.4	mA
				$\overline{CP}$ input			– 1.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				15	26	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with all outputs open, MR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

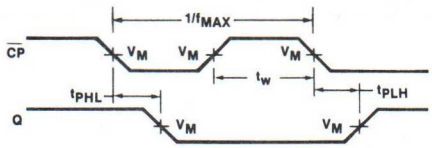
PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ Min	54LS/74LS C_L = 15pF, R_L = 2kΩ Max	UNIT
f_{MAX}	$\overline{CP}$ input count frequency	Waveform 1	35		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_0	Waveform 1		20 20	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_1 or Q_3	Waveform 1		39 39	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to Q_2	Waveform 1		54 54	ns
t_{PHL}	Propagation delay, MR to Q	Waveform 2		39	ns
t_{PLH} t_{PHL}	Propagation delay MS to Q	Waveforms 2 & 3		39 36	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

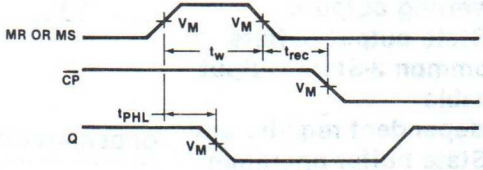
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS Min	54LS/74LS Max	UNIT
t_W	$\overline{CP}$ pulse width	Waveform 1	20		ns
t_W	MR pulse width	Waveform 2	20		ns
t_W	MS pulse width	Waveforms 2 & 3	20		ns
t_{rec}	Recovery time, MR to $\overline{CP}$	Waveform 2	25		ns
t_{rec}	Recovery time, MS to $\overline{CP}$	Waveforms 2 & 3	25		ns

AC WAVEFORMS

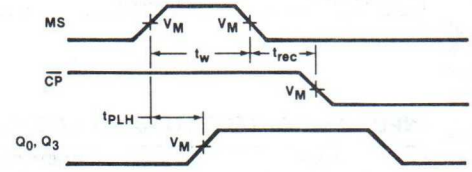


Waveform 1



Waveform 2

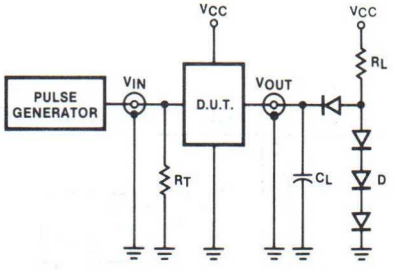
1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.



Waveform 3

TEST CIRCUITS AND WAVEFORMS

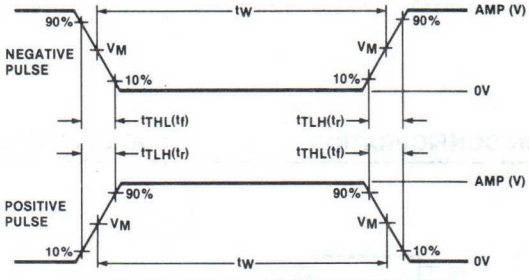
TEST CIRCUIT FOR 54/74 TOTEM-POLE OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

FLIP-FLOP 54/74S534

Octal D Flip-Flop With 3-State Outputs

- 8-bit positive, edge-triggered register
- Inverting outputs
- 3-State output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74S534	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74S534N	
Ceramic DIP	N74S534F	S54S534F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74S
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
Where a 54/74S unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

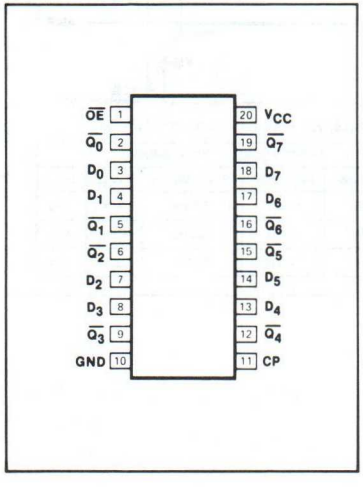
DESCRIPTION

The '534 is an 8-bit, edge-triggered register coupled to eight 3-State inverting output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

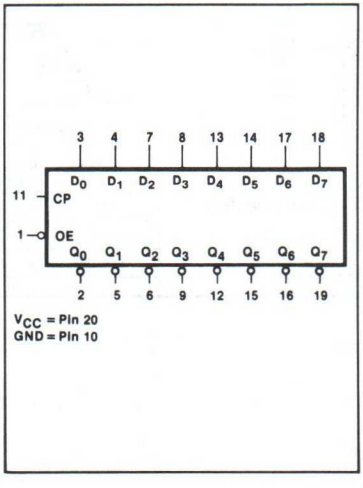
The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's $\overline{Q}$ output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State inverting output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

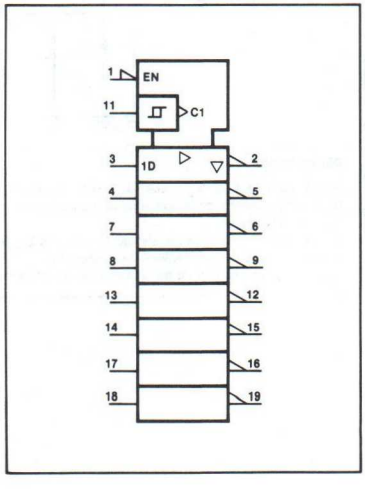
PIN CONFIGURATION



LOGIC SYMBOL

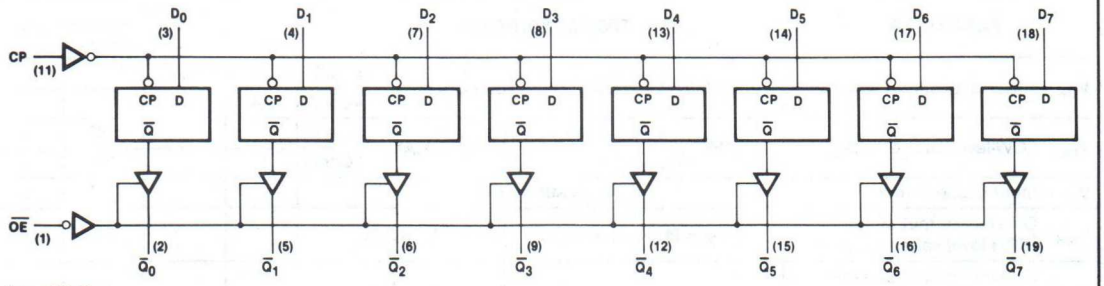


LOGIC SYMBOL (IEEE/IEC)



FLIP-FLOP 54/74S534

LOGIC DIAGRAM



3

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54S	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74S			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for 54S at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74S534			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN	V_O = 2.4V				50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied		V_O = 0.5V				-50	μA
I_I	Input current at maximum input voltage		V_I = 5.5V				1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX	V_I = 0.5V				-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CC}	Supply Current (total)	V_{CC} = MAX	I_{CCL}	All inputs grounded		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.5V, D inputs = GND		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for 54S at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74S		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 3	75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 3		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 1		15	ns
t_{PZL}	Enable time to LOW level	Waveform 2		18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 1, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 2, C_L = 5pF		12	ns

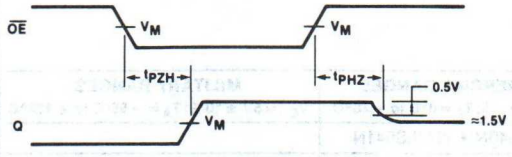
AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54S/74S		UNIT
			Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 3	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 4	5		ns
t_h	Hold time, Data to Clock	Waveform 4	2		ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

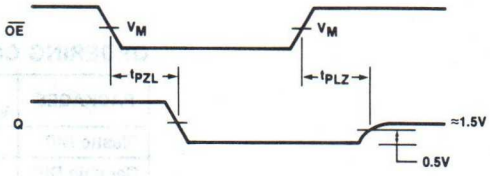
AC WAVEFORMS

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



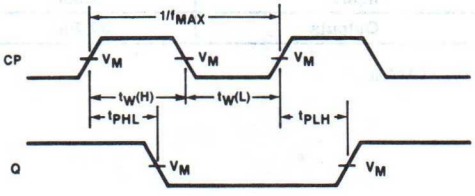
Waveform 1

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



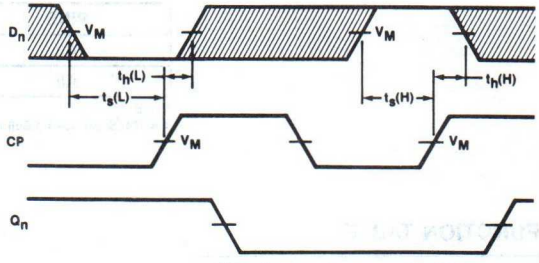
Waveform 2

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 3

DATA SETUP AND HOLD TIMES

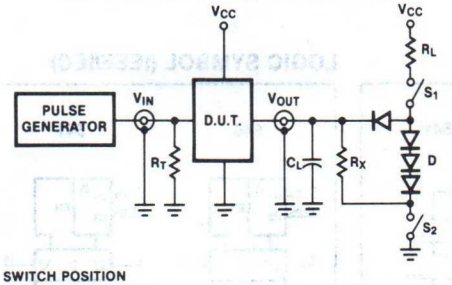


Waveform 4

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



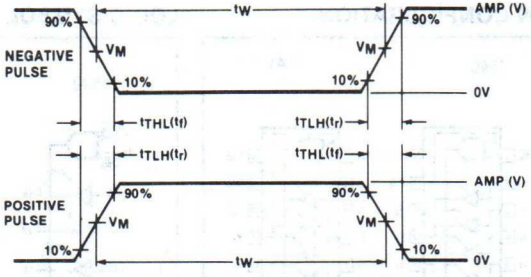
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal Buffer/Line Driver (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS540	9ns	22mA
74LS541	10ns	23mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS540N • N74LS541N	
Ceramic DIP	N74LS540F • N74LS541F	S54LS540F • S54LS541F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

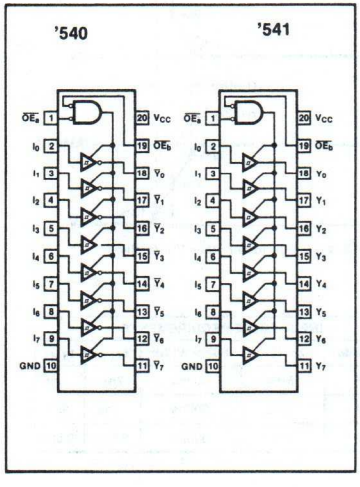
PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

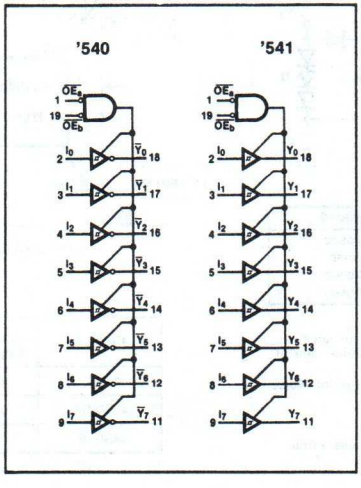
FUNCTION TABLE

INPUTS			OUTPUTS	
$\overline{OE}_1$	$\overline{OE}_2$	I	Y	$\overline{Y}$
L	L	L	L	H
L	L	H	H	L
X	H	X	(Z)	(Z)
H	X	X	(Z)	(Z)

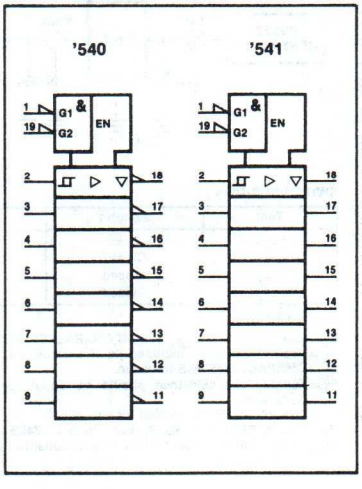
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

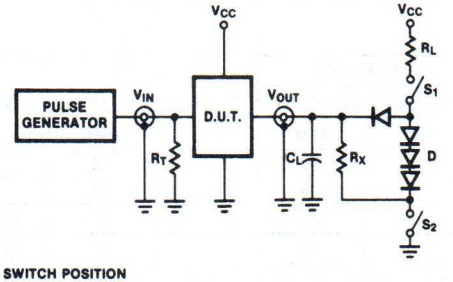
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



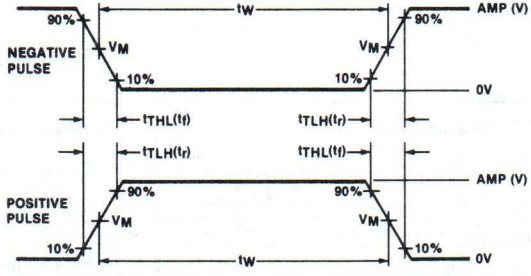
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS540, 541			UNIT
					Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = MIN			0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = MAX			2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = −3mA			2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 12mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_H = MIN, V_{IL} = MAX, V_O = 2.7V					20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_{IL} = MAX, V_O = 0.4V					−20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V					0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		16	25	mA
			I_{CCL}	Outputs LOW		27	45	mA
			I_{CCZ}	Outputs OFF		31	52	mA

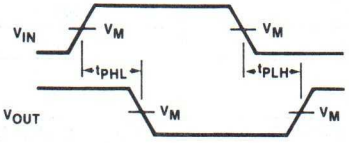
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS540		54/74LS541		UNIT
			C_L = 45pF, R_L = 667Ω		C_L = 45pF, R_L = 667Ω		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay	Waveforms 1 & 2		15 15		15 18	ns
t_{PZH}	Output enable time to HIGH level	Waveform 3		25		32	ns
t_{PZL}	Output enable time to LOW level	Waveform 4		38		38	ns
t_{PHZ}	Output disable time from HIGH level	Waveform 3, C_L = 5pF		18		18	ns
t_{PLZ}	Output disable time from LOW level	Waveform 4, C_L = 5pF		25		29	ns

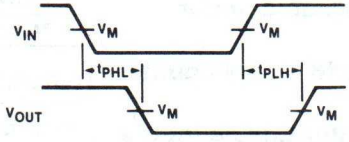
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



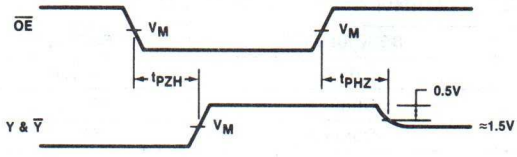
Waveform 1

WAVEFORM FOR NON-INVERTING OUTPUTS



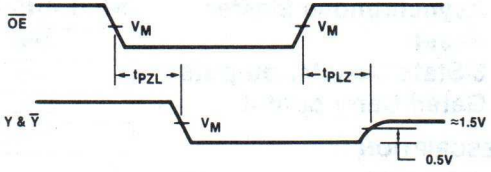
Waveform 2

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.

3

'568 BCD Decade Up/Down Synchronous Counter (3-State)
'569 4-Bit Binary Up/Down Synchronous Counter (3-State)

- Synchronous counting and loading
- UP/DOWN counting
- BCD decade counter — '568
- Modulo 16 binary counter — '569
- Two Count Enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset
- 3-State Counter outputs
- Gated Carry output

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (Total)
74LS568	35MHz	28mA
74LS569	35MHz	28mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS568N • N74LS569N	
Ceramic DIP	N74LS568F • N74LS569F	S54LS568F • S54LS569F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
All	Inputs	1LSul
Q_0–Q_3	Outputs	30LSul
$\overline{TC}$, GC	Outputs	10LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

DESCRIPTION

The '568 and '569 are synchronous presettable UP/DOWN counters featuring an internal carry look-ahead for applications in high speed counting designs.

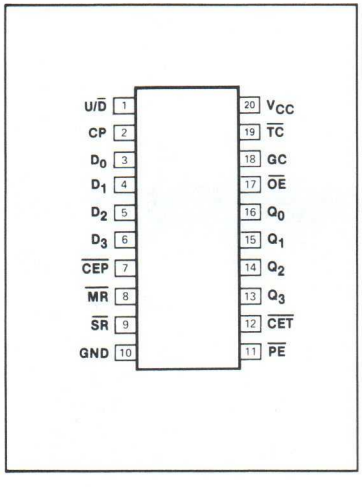
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count-Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered Clock input triggers the flip-flops on the LOW-to-HIGH transition of the Clock.

The counter is fully programmable; that is, the outputs may be preset to either level. Presetting is synchronous with the Clock, and takes place regardless of the levels of the Count Enable inputs. A LOW level on the Parallel Enable ($\overline{PE}$) input disables the counter and causes the data at the D_n inputs to be loaded into the counter on the next LOW-to-HIGH transition of the Clock. The Synchronous Reset ($\overline{SR}$), when LOW one setup time before the LOW-to-HIGH transition of the Clock, overrides the $\overline{CEP}$, $\overline{CET}$ and $\overline{PE}$ inputs, and causes the flip-flops to go LOW coincident with the positive Clock transition.

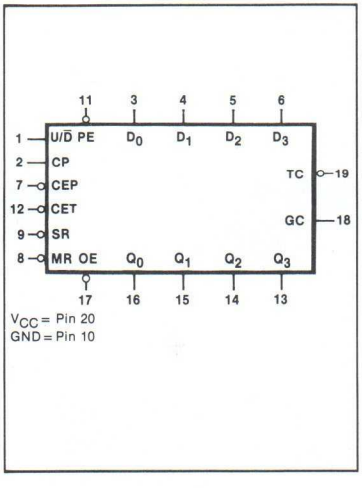
The Master Reset ($\overline{MR}$) is an asynchronous overriding clear function which forces all stages to a LOW state while the $\overline{MR}$ input is LOW without regard to the Clock.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enable inputs ($\overline{CET}$•$\overline{CEP}$) and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be LOW to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus

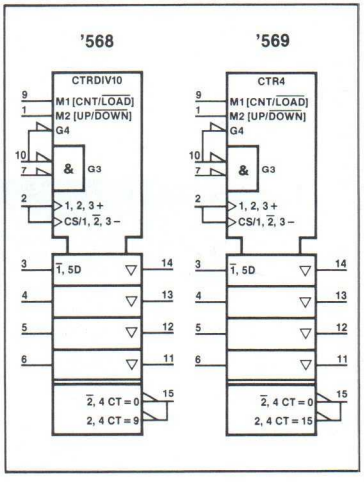
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



enabled will produce a LOW output pulse with a duration approximately equal to the HIGH level portion of the Q_0 output. This LOW level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure A in '168/'169 data sheet for the fast synchronous multistage counting connections.

The Gated Clock output (GC) is a Terminal Count output which provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the Clock pulse when $\overline{TC}$ is LOW. The GC output can be used as a Clock input for the next stage in a simple ripple expansion scheme.

The direction of counting is controlled by the UP/DOWN ($U/\overline{D}$) input; a HIGH will cause the count to increase, a LOW will cause the count to decrease.

The active LOW Output Enable ($\overline{OE}$) input controls the 3-State buffer outputs independent of the counter operation. When $\overline{OE}$ is LOW, the count appears at the buffer outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

3

MODE SELECT—FUNCTION TABLE

COUNTER OPERATING MODES	INPUTS								COUNTER STATES			
	$\overline{MR}$	CP	$\overline{SR}$	$U/\overline{D}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	D_n	Q_0	Q_1	Q_2	Q_3
Asynchronous Reset	L	X	X	X	X	X	X	X	L	L	L	L
Synchronous Reset	H	↑	l	X	X	L	L	X	L	L	L	L
Parallel load	H	↑	h	X	l	X	X	l	L	L	L	L
	H	↑	h	X	l	X	X	h	H	H	H	H
Count up	H	↑	h	h	h	l	l	X	count up			
Count down	H	↑	h	l	h	l	l	X	count down			
Hold (do nothing)	H	↑	h	X	h	h	X	X	no change			
	H	↑	h	X	h	X	h	X	no change			

3-STATE BUFFER OPERATING MODES	INPUTS		OUTPUTS
	$\overline{OE}$	Q_n-Counter	Q_0, Q_1, Q_2, Q_3
Read counter	L	L	L
	L	H	H
Disable outputs	H	L	(Z)
	H	H	(Z)

TERMINAL COUNT FUNCTION TABLE, '568

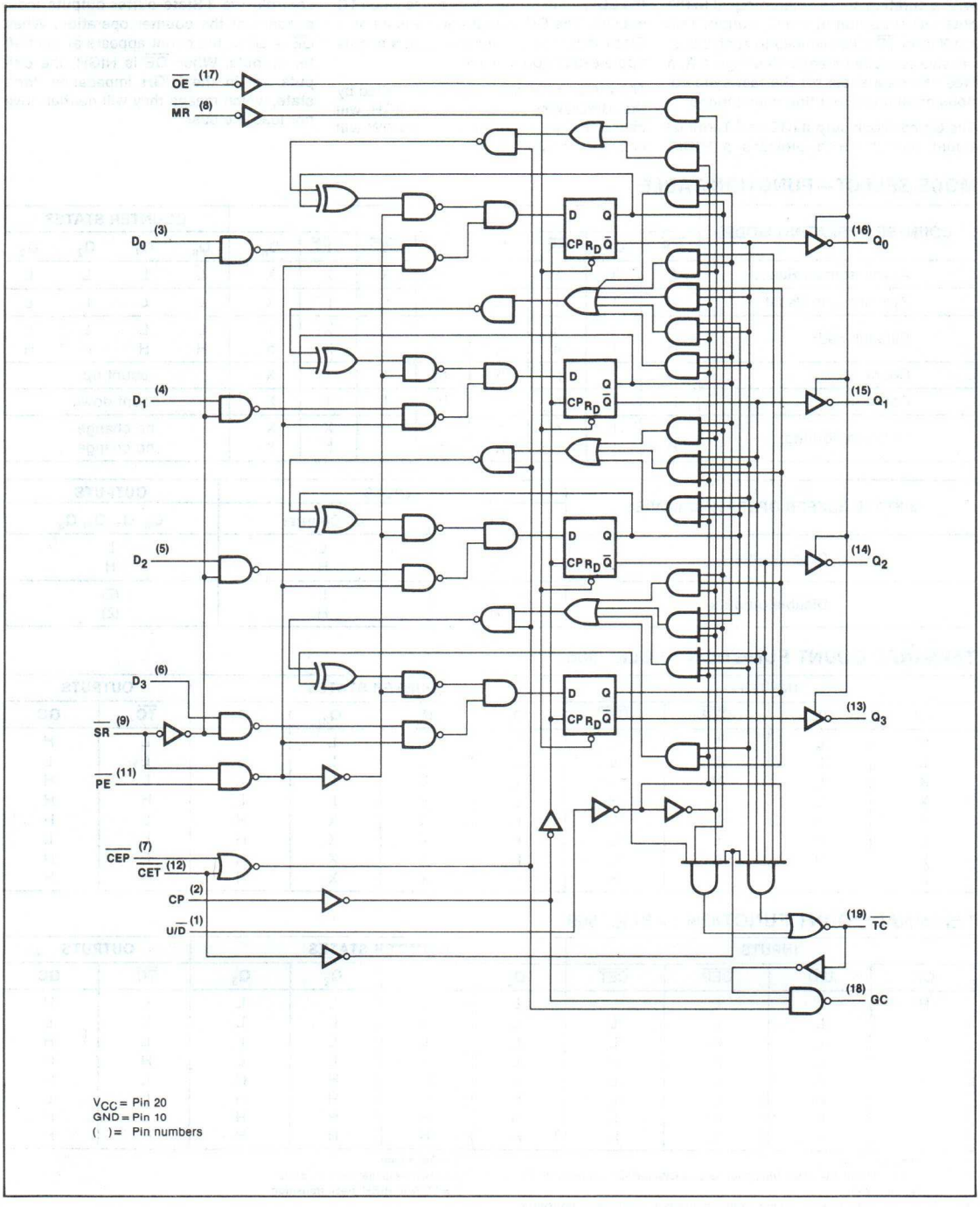
INPUTS				COUNTER STATES				OUTPUTS	
CP	$U/\overline{D}$	$\overline{CEP}$	$\overline{CET}$	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	X	X	H	L	H
L	H	L	L	H	X	X	H	L	L
X	H	H	L	H	X	X	H	L	H
X	H	X	H	H	X	X	H	H	H

TERMINAL COUNT FUNCTION TABLE, '569

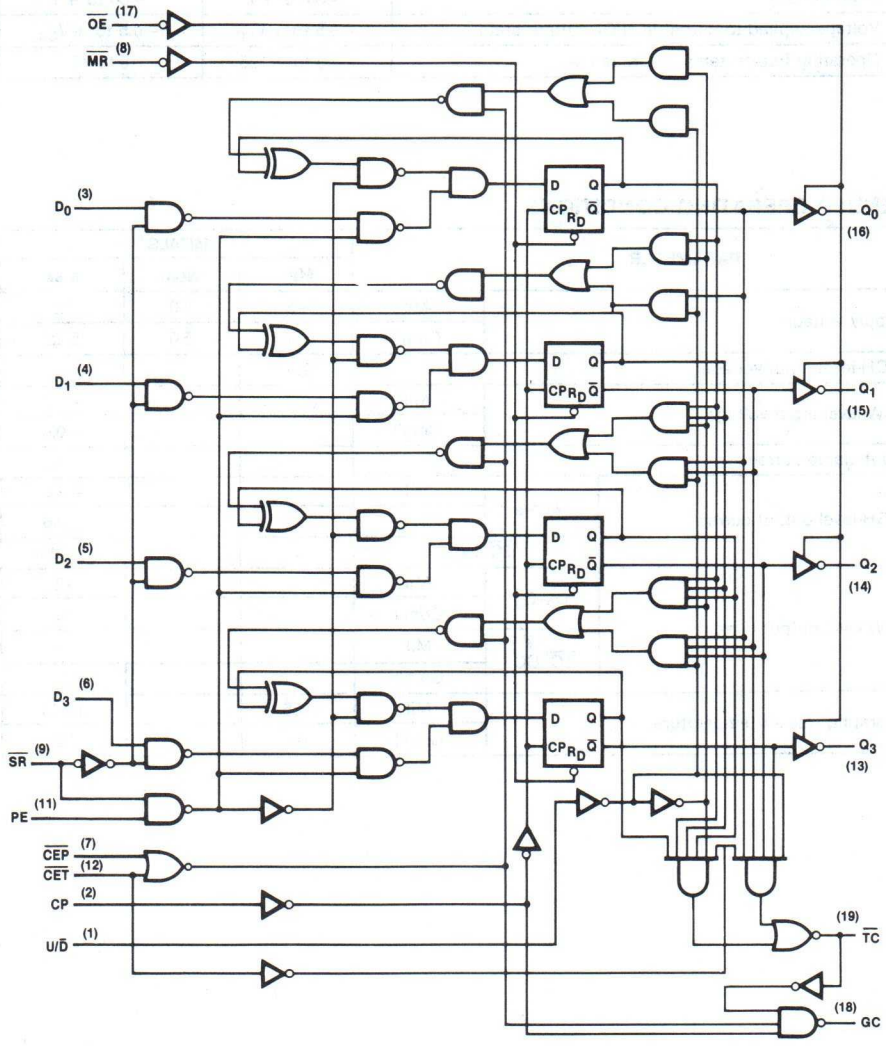
INPUTS				COUNTER STATES				OUTPUTS	
CP	$U/\overline{D}$	$\overline{CEP}$	$\overline{CET}$	Q_0	Q_1	Q_2	Q_3	$\overline{TC}$	GC
H	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L
X	L	H	L	L	L	L	L	L	H
X	L	X	H	L	L	L	L	H	H
H	H	L	L	H	H	H	H	L	H
L	H	L	L	H	H	H	H	L	L
X	H	H	L	H	H	H	H	L	H
X	H	X	H	H	H	H	H	H	H

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

LOGIC DIAGRAM, '568



LOGIC DIAGRAM, '569



V_{CC} = Pin 20
GND = Pin 10
( ) = Pin numbers

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER				54/74LS			UNIT
				Min	Nom	Max	
V_{CC}	Supply voltage		Mil	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			V
V_{IL}	LOW-level input voltage		Mil			+0.7	V
			Com'l			+0.8	V
I_{IK}	Input clamp current					−18	mA
I_{OH}	HIGH-level output current	Q_0–Q_3	Mil			−1.0	mA
			Com'l			−2.6	mA
		$\overline{TC}$, GC				−400	μA
I_{OL}	LOW-level output current	Q_0–Q_3	Mil			12	mA
			Com'l			24	mA
		$\overline{TC}$, GC	Mil			4	mA
			Com'l			8	mA
T_A	Operating free-air temperature		Mil	−55		+125	°C
			Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]				54/74LS568, 569			UNIT
						Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	Q_0-Q_3	I_{OH} = MAX	Mil	2.4			V
					Com'l	2.4			V
			$\overline{TC}$, GC	I_{OH} = MAX	Mil	2.4			V
					Com'l	2.4			V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	Q_0-Q_3	I_{OL} = MAX	Mil			0.4	V
					Com'l			0.5	V
				I_{OL} = 12mA	74LS			0.4	V
			$\overline{TC}$, GC	I_{OL} = MAX	Mil			0.4	V
					Com'l			0.5	V
				I_{OL} = 4mA	74LS			0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}						-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.7V						20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V						-20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V						0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V						20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V						-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			Q_0-Q_3	-30		-100	mA
					$\overline{TC}$, GC	-15		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX					28	43	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS $C_L = 45pF$, $R_L = 667\Omega$		UNIT
			Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	25		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		20 23	ns
t_{PLH} t_{PHL}	Propagation delay Clock to $\overline{TC}$	Waveform 2		35 35	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$	Waveform 3		14 14	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ control to $\overline{TC}$	Waveform 4		25 29	ns
t_{PLH} t_{PHL}	Propagation delay Clock to GC	Waveform 2		20 20	ns
t_{PHL}	Propagation delay $\overline{MR}$ to output	Waveform 5		35	ns
t_{PZH}	Output enable to HIGH level	Waveform 6			ns
t_{PZL}	Output enable to LOW level	Waveform 7			ns
t_{PHZ}	Output disable from HIGH level	Waveform 6, $C_L = 5pF$			ns
t_{PLZ}	Output disable from LOW level	Waveform 7, $C_L = 5pF$			ns

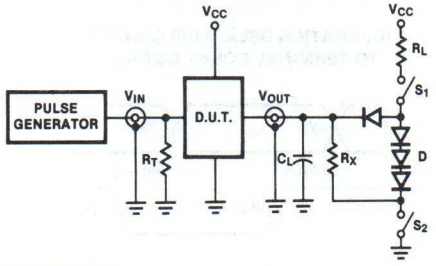
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Clock pulse width	Waveform 1	20		ns
t_s	Setup time data to clock	Waveform 8	20		ns
t_h	Hold time data to clock	Waveform 8	0		ns
t_s	Setup time $\overline{PE}$ to clock	Waveform 8	25		ns
t_h	Hold time $\overline{PE}$ to clock	Waveform 8	0		ns
t_s	Setup time $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 9	20		ns
t_h	Hold time $\overline{CEP}$ & $\overline{CET}$ to clock	Waveform 9	0		ns
t_s	Setup time U/$\overline{D}$ to clock	Waveform 10	30		ns
t_h	Hold time U/$\overline{D}$ to clock	Waveform 10	0		ns
t_s	Setup time $\overline{SR}$ to clock	Waveform 11	30		ns
t_h	Hold time $\overline{SR}$ to clock	Waveform 11	0		ns
t_{rec}	Recovery time $\overline{MR}$ to clock	Waveform 5	20		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



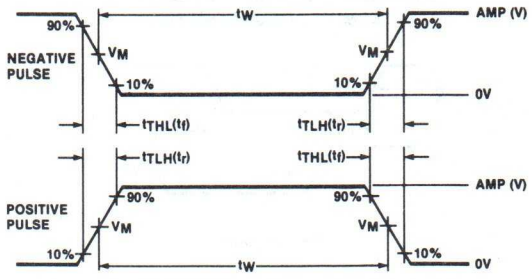
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

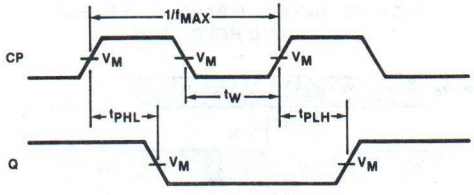


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

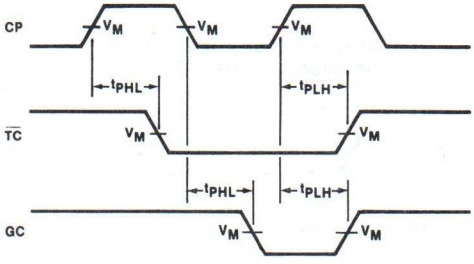
AC WAVEFORMS

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 1

CLOCK TO TERMINAL COUNT DELAYS

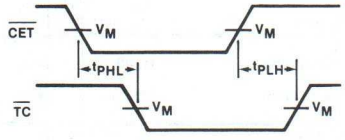


Waveform 2

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

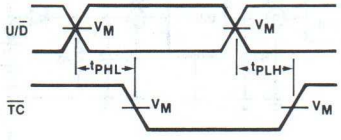
AC WAVEFORMS (Continued)

PROPAGATION DELAYS $\overline{CET}$ INPUT TO TERMINAL COUNT OUTPUT



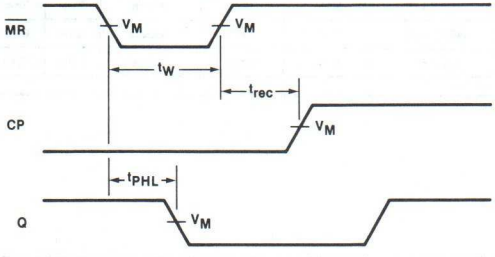
Waveform 3

PROPAGATION DELAYS U/$\overline{D}$ CONTROL TO TERMINAL COUNT OUTPUT



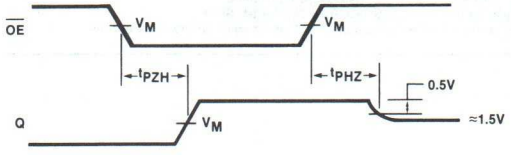
Waveform 4

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME



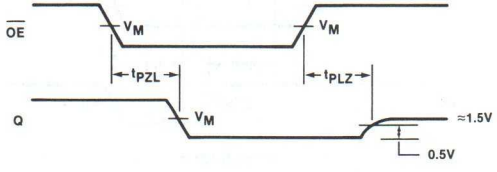
Waveform 5

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



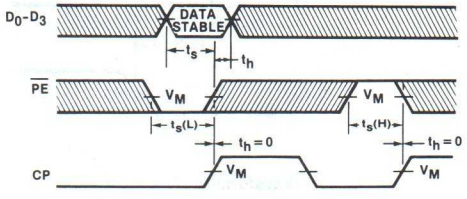
Waveform 6

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 7

PARALLEL DATA AND PARALLEL ENABLE SETUP AND HOLD TIMES

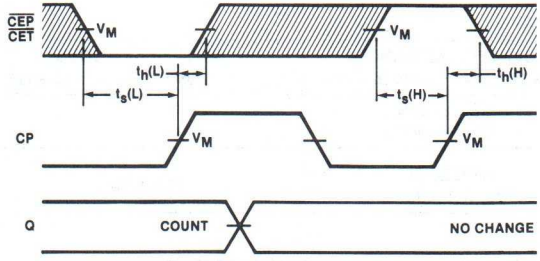


Waveform 8

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

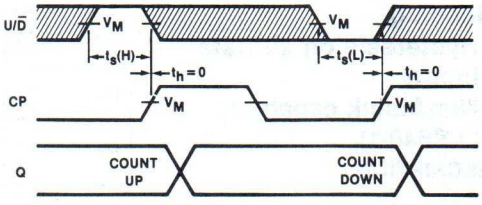
AC WAVEFORMS (Continued)

COUNT ENABLE SETUP AND HOLD TIMES



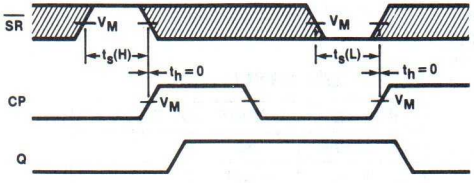
Waveform 9

UP/DOWN CONTROL SETUP AND HOLD TIMES



Waveform 10

SYNCHRONOUS RESET SETUP AND HOLD TIMES



Waveform 11

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

TRANSCEIVER 54/74LS640, 74LS640-1

Inverting Octal Bus Transceiver (3-State)

- **Octal bidirectional bus interface**
- **Inverting 3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**
- **48mA sink capability ('LS640-1)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS640 & -1	7ns	58mA

DESCRIPTION

The 'LS640 is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS640-1 features a 48mA sink current capability. The device features a Chip Enable ($\overline{CE}$) input for easy cascading and a Send/Receive (S/$\overline{R}$) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS640N N74LS640-1N	
Ceramic DIP	N74LS640F N74LS640-1F	S54LS640F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

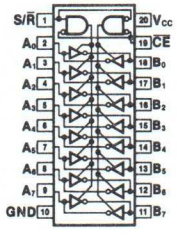
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

FUNCTION TABLE

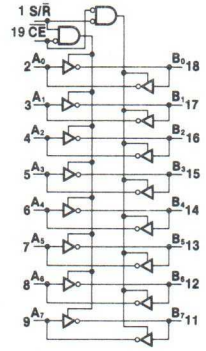
INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

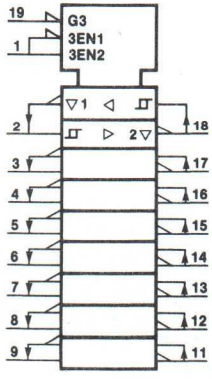
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on A and B inputs only.

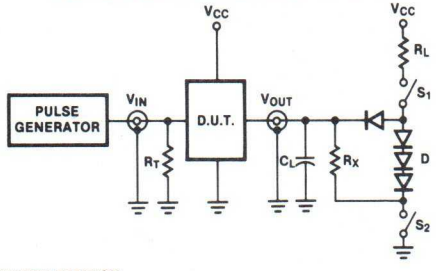
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

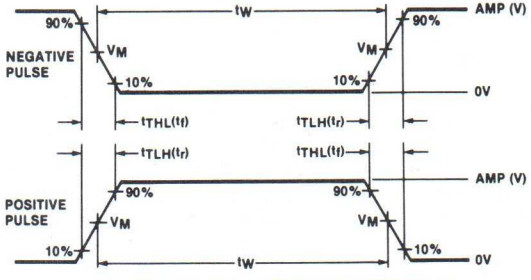


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS640			74LS640-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			2.0			V
			I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.5			−1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 2.7V					20			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 0.4V					−400			−400	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					−0.4			−0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−130	−40		−130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

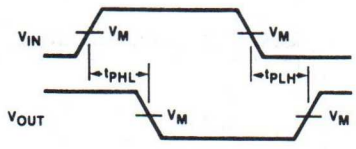
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74LS & -1 $C_L = 45pF$, $R_L = 667\Omega$ Min	54/74LS & -1 $C_L = 45pF$, $R_L = 667\Omega$ Max	UNIT
t_{PLH} t_{PHL} Propagation delay A input to B output	Waveform 1		10 15	ns
t_{PLH} t_{PHL} Propagation delay B input to A output	Waveform 1		10 15	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2, $C_L = 5pF$		25	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3, $C_L = 5pF$		25	ns

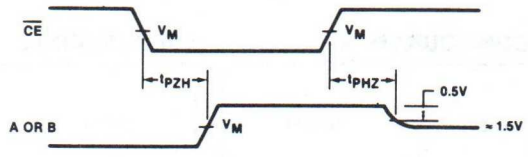
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

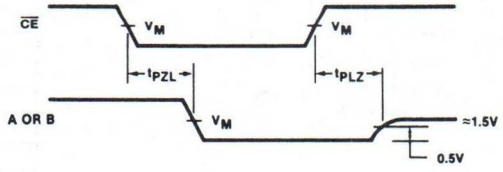
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families.

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

TRANSCEIVERS 54/74LS641, LS642, 74LS641-1, LS642-1

Octal Bus Transceiver (Open Collector)

- Octal bidirectional bus interface
- Open Collector Outputs
  - — 'LS641, non-inverting
  - — 'LS642, inverting
- PNP inputs for reduced loading
- Hysteresis on all Data inputs
- 48mA sink capability ('LS641-1, LS642-1)

TYPE	TYPICAL PROPAGATION DELAY (A to B)	TYPICAL SUPPLY CURRENT (Total)
74LS641 & -1	17ns	58mA
74LS642 & -1	17ns	58mA

FUNCTION TABLE, 'LS641

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

FUNCTION TABLE, 'LS642

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUTS	B = $\overline{A}$
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

ORDERING CODE

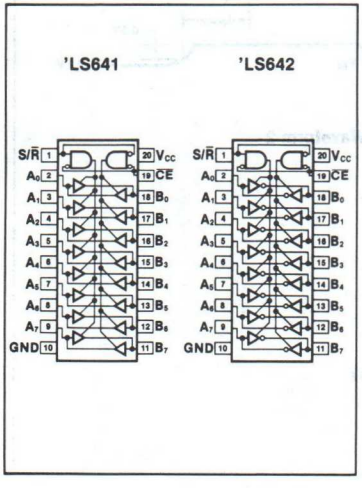
PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N74LS641N N74LS641-1N N74LS642N N74LS642-1N	
Ceramic DIP	N74LS641F N74LS641-1F N74LS642F N74LS642-1F	S54LS641F S54LS642F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

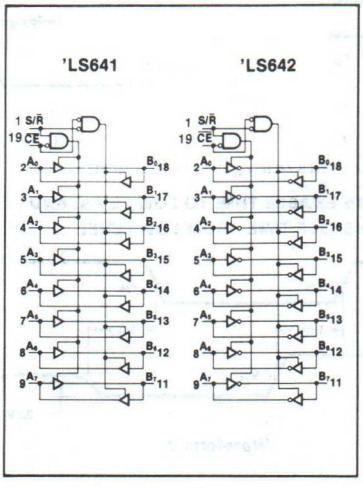
PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

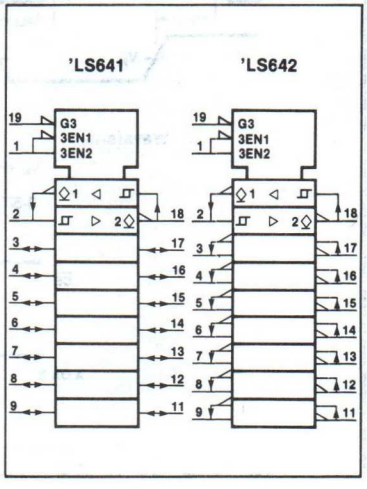
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

NOTE
V_{IN} limited to 5.5V on A and B inputs only.

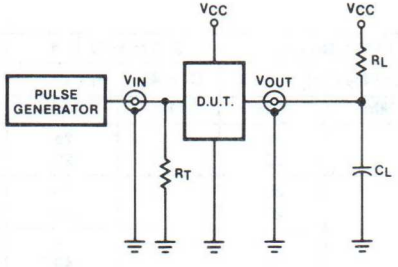
3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
V_{OH}	HIGH-level output voltage				5.5	V
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

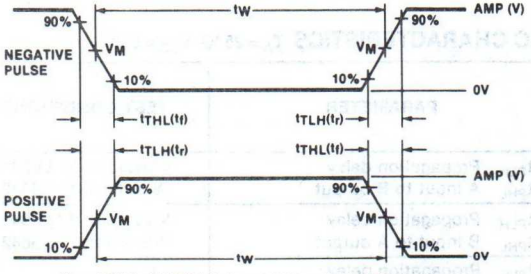
TEST CIRCUIT FOR 54/74 OPEN COLLECTOR OUTPUTS



DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

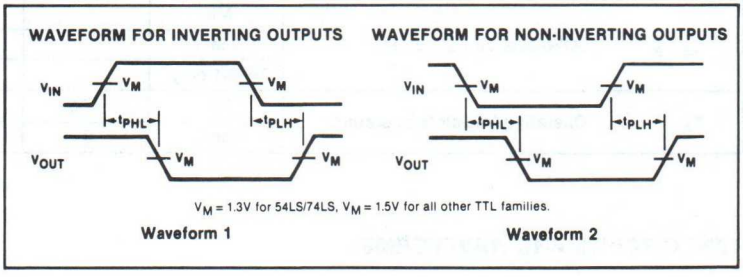
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS641 54/74LS642			74LS641-1 74LS642-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
I_{OH}	HIGH-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, V_{OH} = 5.5V					100			100	μA
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{CC}	Supply current[3] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C
3. Measure I_{CC} with outputs open.

AC WAVEFORMS



AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54/74LS641 & -1 C_L = 45pF, R_L = 667Ω		54/74LS642 & -1 C_L = 45pF, R_L = 667Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A input to B output	Waveform 2, 'LS641 Waveform 1, 'LS642		25 25		25 25	ns
t_{PLH} t_{PHL}	Propagation delay B input to A output	Waveform 2, 'LS641 Waveform 1, 'LS642		25 25		25 25	ns
t_{PLH}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 1 Waveform 1 Waveform 2		 40 40 40		 40 40 40	ns
t_{PHL}	Propagation delay $\overline{CE}$, S/$\overline{R}$ inputs to A output $\overline{CE}$ input to B output S/$\overline{R}$ input to B output	 Waveform 2 Waveform 2 Waveform 1		 50 50 50		 60 60 60	ns

TRANSCEIVER 54/74LS645, 74LS645-1

Octal Bus Transceiver (3-State)

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**
- **48mA sink capability ('LS645-1)**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS645 & -1	10ns	58mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS645N N74LS645-1N	
Ceramic DIP	N74LS645F N74LS645-1F	S54LS645F

3

DESCRIPTION

The 'LS645 is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. In addition, the 74LS645-1 features a 48mA sink current capability. The device features a Chip Enable ($\overline{CE}$) input for easy cascading and a Send/Receive (S/R) input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS & -1
All	Inputs	1LSul
All	Outputs	30LSul

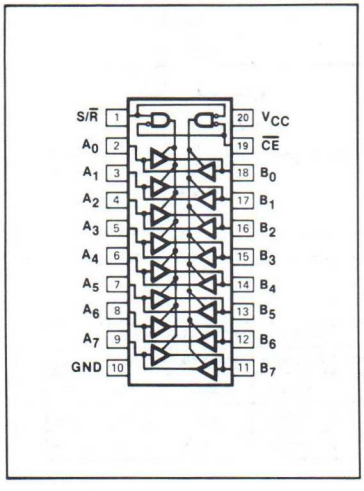
NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

FUNCTION TABLE

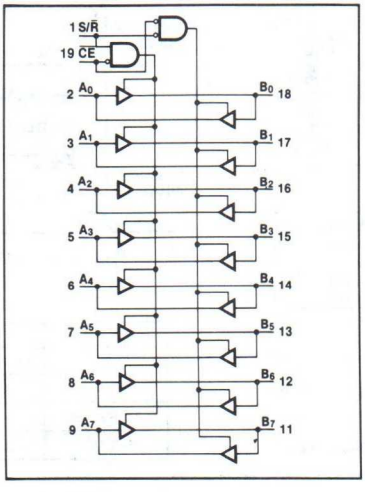
INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = B	INPUTS
L	H	INPUTS	B = A
H	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

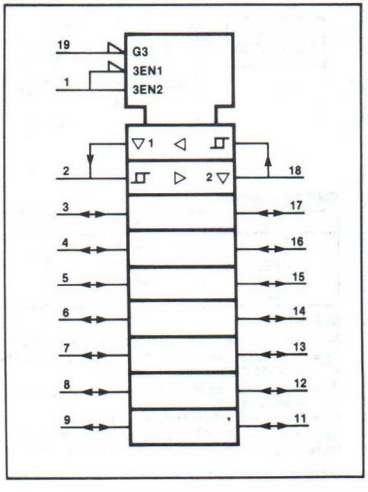
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS & -1	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

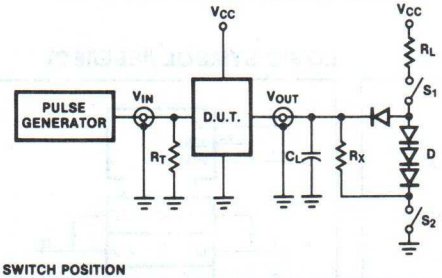
NOTE
V_{IN} limited to 5.5V on A and B inputs only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS & -1			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.5	V
		Com'l			+0.6	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
		74LS-1 only			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

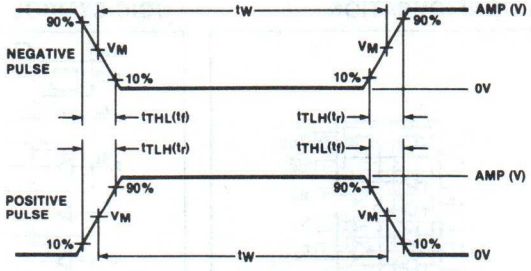


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature unless range otherwise noted)

PARAMETER		TEST CONDITIONS[1]			54/74LS645			74LS645-1			UNIT
					Min	Typ[2]	Max	Min	Typ[2]	Max	
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN, A or B input		Mil	0.1	0.4					V
				Com'l	0.2	0.4		0.2	0.4		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OH} = MAX		2.0			2.0			V
			I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = 12mA	Mil		0.25	0.4				V
				Com'l		0.25	0.4		0.25	0.4	V
			I_{OL} = 24mA	74LS		0.35	0.5		0.35	0.5	V
			I_{OL} = 48mA						0.4	0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.5			-1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 2.7V					20			20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, $\overline{CE}$ input = 2.0V, V_O = 0.4V					-400			-400	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V	A or B input			0.1			0.1	mA
			V_I = 7.0V	S/$\overline{R}$ or $\overline{CE}$ input			0.1			0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					20			20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V					-0.4			-0.4	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-130	-40		-130	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX	I_{CCH}	Outputs HIGH		48	70		48	70	mA
			I_{CCL}	Outputs LOW		62	90		62	90	mA
			I_{CCZ}	Outputs OFF		64	95		64	95	mA

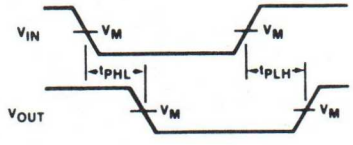
NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with outputs open.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	54/74LS & -1 $C_L = 45pF$, $R_L = 667\Omega$		UNIT
		Min	Max	
t_{PLH} t_{PHL} Propagation delay A input to B output	Waveform 1		15 15	ns
t_{PLH} t_{PHL} Propagation delay B input to A output	Waveform 1		15 15	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2		40	ns
t_{PZH} Enable to HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3		40	ns
t_{PZL} Enable to LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3		40	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 2, $C_L = 5pF$		25	ns
t_{PHZ} Disable from HIGH $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 2, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to A output	Waveform 3, $C_L = 5pF$		25	ns
t_{PLZ} Disable from LOW $\overline{CE}$, S/$\overline{R}$ inputs to B output	Waveform 3, $C_L = 5pF$		25	ns

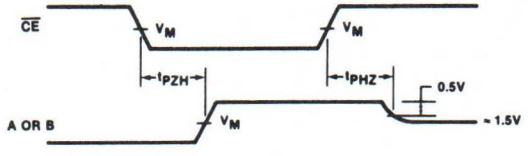
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

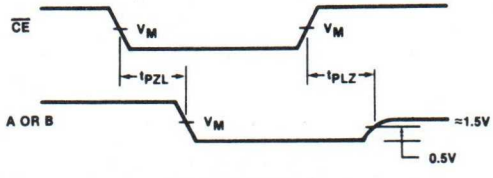
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

V_M = 1.3V for 54LS/74LS, V_M = 1.5V for all other TTL families

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

REGISTER FILE 54/74LS670

4 x 4 Register File (3-State)

- **Simultaneous and independent Read and Write operations**
- **Expandable to almost any word size and bit length**
- **3-State outputs**
- **See '170 for open collector version**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
74LS670	25ns	30mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N74LS670N	
Ceramic DIP	N74LS670F	S54LS670F
Flatpack		S54LS670W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54/74LS
D_0-D_3, W_A, W_B, R_A, R_B	Inputs	1LSul
$\overline{WE}$	Input	2LSul
$\overline{RE}$	Input	3LSul
Q_0-Q_3	Outputs	10LSUl

NOTE
A 54/74LS unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

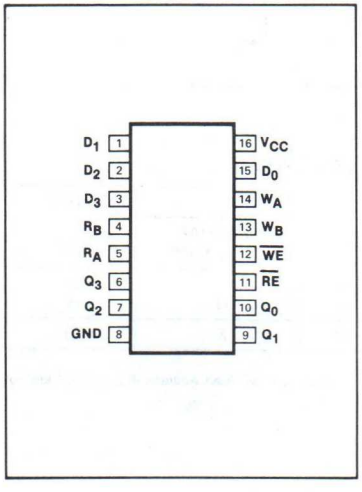
DESCRIPTION

The '670 is a 16-bit 3-State Register File organized as 4 words of 4 bits each. Separate Read and Write Address and Enable inputs are available, permitting simultaneous writing into one word location and reading from another location. The 4-bit word to be stored is presented to four Data inputs. The Write Address inputs (W_A and W_B) determine the location of the stored word. When the Write Enable ($\overline{WE}$) input is LOW, the data is entered into the addressed location. The addressed location remains transparent to the data while the $\overline{WE}$ is LOW. Data supplied at the inputs will be read out in true (non-inverting) form from the 3-State outputs. Data and Write Address inputs are inhibited when $\overline{WE}$ is HIGH.

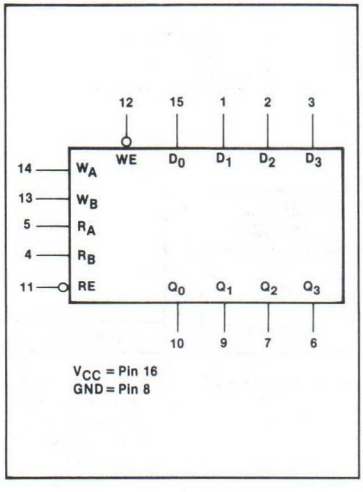
Direct acquisition of data stored in any of the four registers is made possible by individual Read Address inputs (R_A and R_B). The addressed word appears at the four outputs when the Read Enable ($\overline{RE}$) is LOW. Data outputs are in the HIGH impedance "off" state when the Read Enable input is HIGH. This permits outputs to be tied together to increase the word capacity to very large numbers.

Up to 128 devices can be stacked to increase the word size to 512 locations by tying the 3-State outputs together. Since the limiting factor for expansion is the output HIGH current, further stacking is possible by tying pull-up resistors to the outputs to increase the I_{OH} current available. Design of the Read Enable signals for the stacked devices must ensure that there is no overlap in the LOW levels which would cause more than one output to be active at the same time. Parallel expansion to generate n-bit words is accomplished by driving the Enable and Address inputs of each device in parallel.

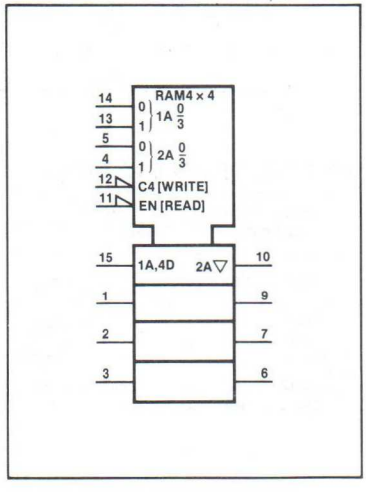
PIN CONFIGURATION



LOGIC SYMBOL

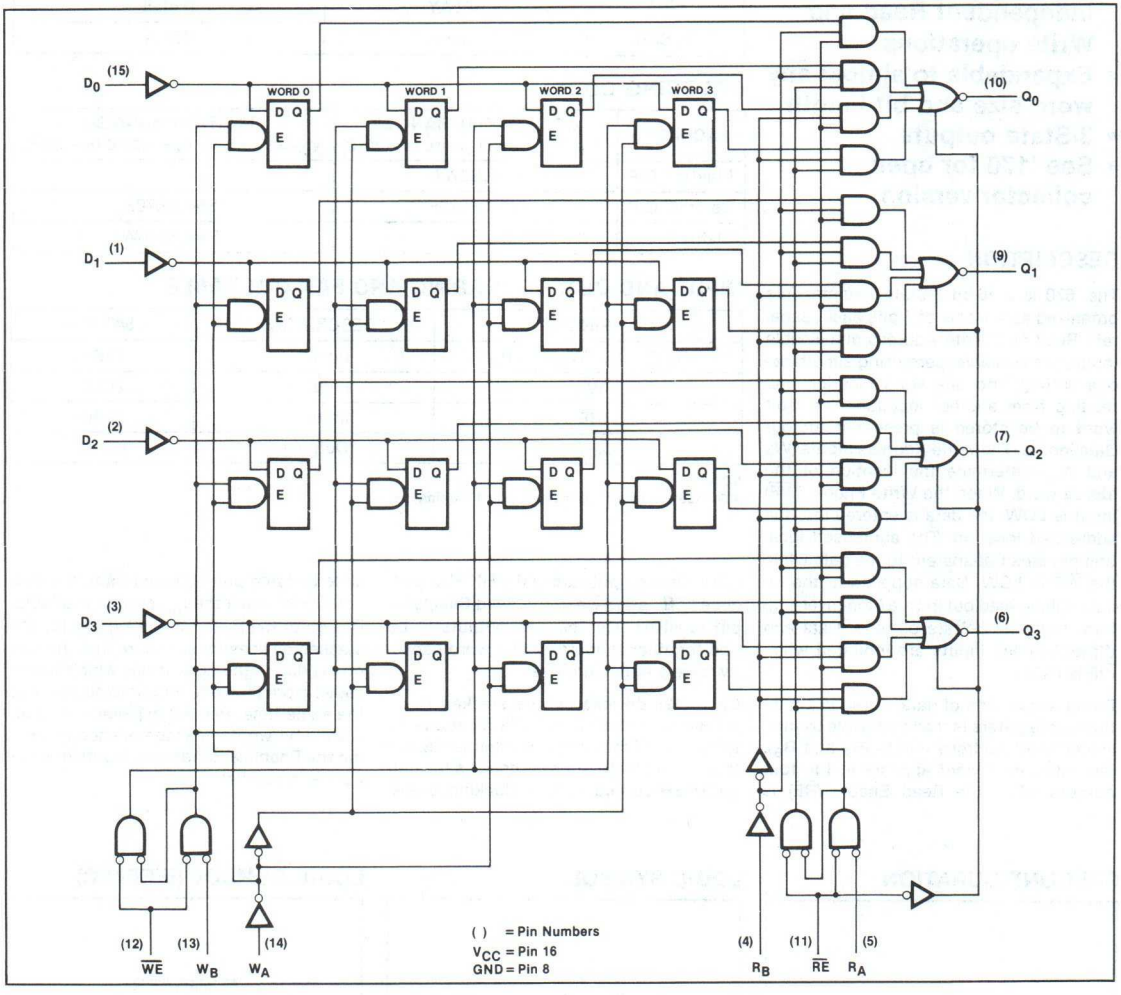


LOGIC SYMBOL (IEEE/IEC)



REGISTER FILE 54/74LS670

LOGIC DIAGRAM



WRITE MODE SELECT TABLE

OPERATING MODE	INPUTS		INTERNAL LATCHES[a]
	$\overline{WE}$	D_n	
Write Data	L	L	L
	L	H	H
Data Latched	H	X	no change

NOTE

a. The Write Address (W_A and W_B) to the "internal latches" must be stable while $\overline{WE}$ is LOW for conventional operation.

READ MODE SELECT TABLE

OPERATING MODE	INPUTS		OUTPUT
	$\overline{RE}$	INTERNAL LATCHES[b]	Q_n
Read	L	L	L
	L	H	H
Disabled	H	X	(Z)

NOTE

b. The selection of the "internal latches" by Read Address (R_A and R_B) are not constrained by $\overline{WE}$ or $\overline{RE}$ operation.

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54LS	74LS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

3

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74LS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−1.0	mA
		Com'l			−2.6	mA
I_{OL}	LOW-level output current	Mil			4	mA
		Com'l			8	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			54/74LS670 Min	54/74LS670 Typ[2]	54/74LS670 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.4		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil		0.25	0.4	V
				Com'l		0.35	0.5	V
			I_{OL} = 4mA	74LS		0.25	0.4	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					– 1.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.7V					20	μA
I_{OZL}	Off-state outut current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.4V					– 20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V	D_0-D_3, W_A, W_B, R_A, R_B inputs				0.1	mA
			$\overline{WE}$ input				0.2	mA
			$\overline{RE}$ input				0.3	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V	D_0-D_3, W_A, W_B, R_A, R_B inputs				20	μA
			$\overline{WE}$ input				40	μA
			$\overline{RE}$ input				60	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V	D_0-D_3, W_A, W_B, R_A, R_B inputs				– 0.4	mA
			$\overline{WE}$ input				– 0.8	mA
			$\overline{RE}$ input				– 1.2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			– 20		– 100	mA
I_{CC}	Supply current[4] (total)	V_{CC} = MAX				30	50	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = + 0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. Measure I_{CC} with 4.5V applied to all Data inputs and Read Enable and Write Enable inputs, ground Read Address and Write Address inputs and leave all outputs open. This is a worse-case condition.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	54LS/74LS C_L = 15pF, R_L = 2kΩ Min	54LS/74LS C_L = 15pF, R_L = 2kΩ Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Read Address to output	Waveform 2		40 45	ns
t_{PLH} t_{PHL}	Propagation delay Write Enable to output	Waveform 1		45 50	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 1		45 40	ns
t_{PZH}	Enable time to HIGH level	Waveform 4		35	ns
t_{PZL}	Enable time to LOW level	Waveform 5		40	ns
t_{PHZ}	Disable time from HIGH level	Waveform 4, C_L = 5pF		50	ns
t_{PLZ}	Disable time from LOW level	Waveform 5, C_L = 5pF		35	ns

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	54LS/74LS		UNIT
			Min	Max	
t_W	Read Enable pulse width	Waveform 6	25		ns
t_W	Write Enable pulse width	Waveform 3, $\overline{RE}$ = ≤0.8V	25		ns
t_s	Setup time, Data to positive-going $\overline{WE}$[c]	Waveform 3	10		ns
t_h	Hold time, Data to positive-going $\overline{WE}$[c]	Waveform 3	15		ns
t_s	Setup time, Read Address to negative-going $\overline{WE}$[c]	Waveform 3	15		ns
t_h	Hold time, Read Address to positive-going $\overline{WE}$[d]	Waveform 3	5.0		ns
t_{latch}	Latch time for new data[d]	Waveform 3	25		ns

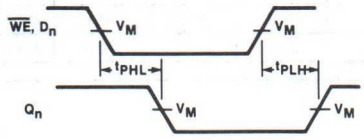
NOTES

c. Write address setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_s (write address to $\overline{WE}$) can be ignored, as any address selection sustained for the final 30ns of the $\overline{WE}$ pulse and during t_h (write address to $\overline{WE}$) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

d. Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data. This parameter is measured from the falling edge of $\overline{WE}$ to the rising edge of R_A or R_B. $\overline{RE}$ must be LOW.

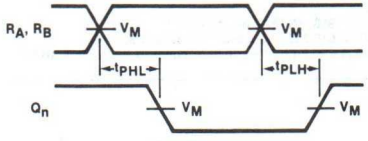
AC WAVEFORMS

PROPAGATION DELAY, WRITE ENABLE AND DATA TO OUTPUTS



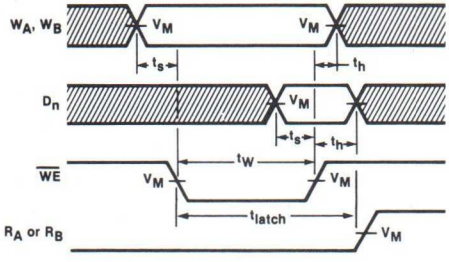
Waveform 1

PROPAGATION DELAY READ ADDRESS TO OUTPUTS



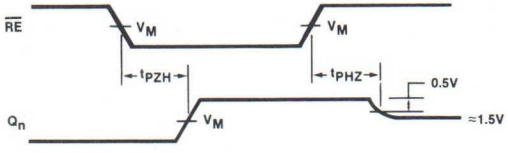
Waveform 2

SETUP AND HOLD TIMES WRITE ADDRESS AND DATA TO WRITE ENABLE



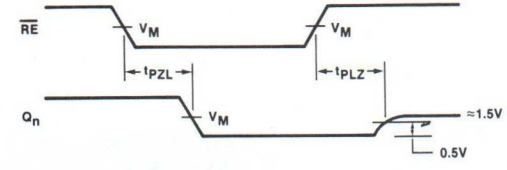
Waveform 3

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



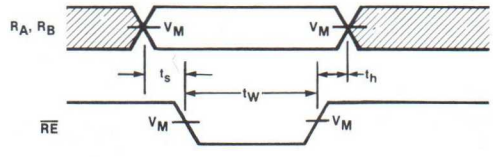
Waveform 4

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 5

SETUP AND HOLD TIMES READ ADDRESS TO READ ENABLE



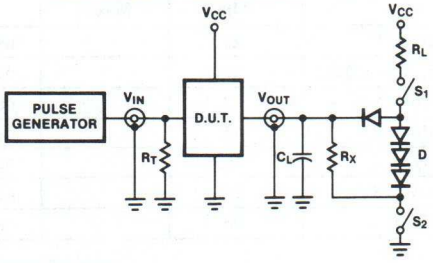
Waveform 6

V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



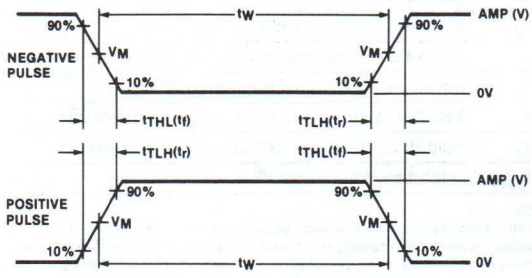
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
54/74	3.0V	1MHz	500ns	7ns	7ns
54LS/74LS	3.0V	1MHz	500ns	15ns	6ns
54S/74S	3.0V	1MHz	500ns	2.5ns	2.5ns

Section 4
8T Series Data Sheets

BUS TRANSCEIVERS 8T26A, 28

3-State Quad Bus Transceiver

- **High speed Schottky quad transceivers**
- **48mA LOW-state drive**
- **200μA bus loading**
- **Ideal for:**
  - **Half-duplex data transmission**
  - **Memory interface buffers**
  - **Data routing in bus oriented systems**
  - **High current drivers**
  - **MOS/CMOS-to-TTL interface**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T26A	7ns	48mA
N8T28	10ns	67mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N8T26AN • N8T28N	
Ceramic DIP	N8T26AF • N8T28F	S8T26AF • S8T28F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	N8T	S8T
I_N	Input	0.5SuI	0.5SuI
D/E, R/E	Inputs	0.5SuI	0.5SuI
D_{OUT}	Output	24SuI	16SuI
R_{OUT}	Output	10SuI	6SuI

NOTE
A unit load (ul) is 50μA I_{IH} and −2.0mA I_{IL}.

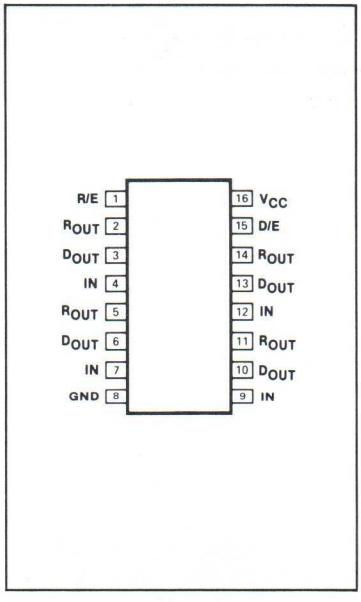
4

DESCRIPTION

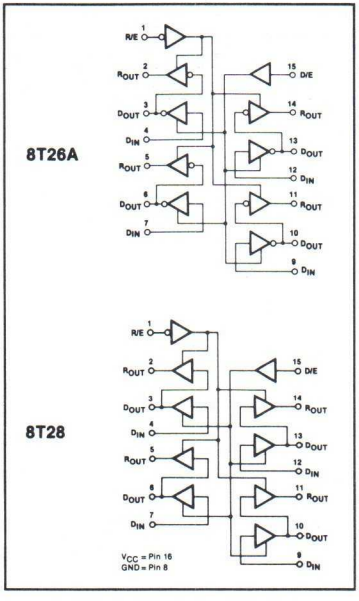
The 8T26A/28 consists of four pairs of 3-state logic elements configured as quad bus drivers/receivers, along with separate buffered receiver enable and driver enable lines. This single IC quad transceiver design distinguishes the 8T26A/28 from conventional multi-IC implementations. In addition, the 8T26/28's ultra high speed while driving heavy bus capacitance (300pF) makes these devices particularly suitable for memory systems and bidirectional data buses.

Both the driver and receiver gates have 3-State outputs and low-current PNP inputs. 3-State outputs provide the high switching speeds of totem-pole TTL circuits while offering the bus capability of open collector gates. PNP inputs reduce input loading to 200μA maximum.

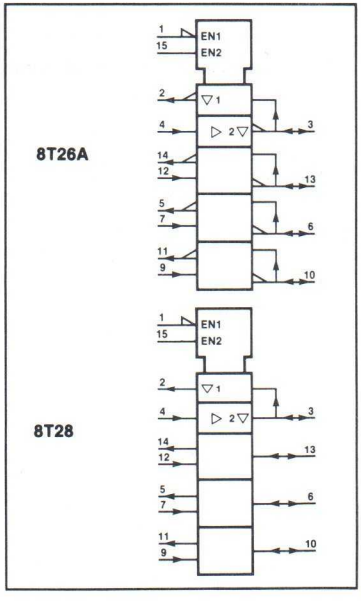
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8T	N8T	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
I_{OL}	Continuous	100	100	m A
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER				8T			UNIT
				Min	Nom	Max	
V_{CC}	Supply Voltage		Mil	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			V
V_{IL}	LOW-level input voltage		Mil			+0.8	V
			Com'l			+0.8	V
I_{IK}	Input clamp current					−18	mA
I_{OH}	HIGH-level output current	Driver	Mil			−2	mA
			Com'l			−10	mA
I_{OL}	LOW-level output current	Driver	Mil			32	mA
			Com'l			48	mA
		Receiver	Mil			12	mA
			Com'l			20	mA
T_A	Operating free-air temperature		Mil	−55		+125	°C
			Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		N8T26A, N8T28		S8T26A, S8T28		UNIT
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA			−1.2		−1.2	V
V_{BD}	Input breakdown voltage	V_{CC} = MAX, I_I = 1mA		5.5		5.5		V
V_{OH}	HIGH-level output voltage, Driver outputs	V_{CC} = MIN	I_{OH} = −10mA	2.4				V
			I_{OH} = −2mA			2.4		V
V_{OH}	HIGH-level output voltage, Receiver outputs	V_{CC} = MIN, I_{OH} = −100μA		3.25				V
		V_{CC} = 5.0V, I_{OH} = −100μA				3.0		V
V_{OL}	LOW-level output voltage, Driver outputs	V_{CC} = MIN	I_{OL} = 48mA		0.5			V
			I_{OL} = 32mA				0.5	V
V_{OL}	LOW-level output voltage, Receiver outputs	V_{CC} = MIN	I_{OL} = 20mA		0.5			V
			I_{OL} = 12mA				0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V			100		100	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V			−100		−100	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 4.5V			25		25	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	Driver, Receiver		−200		−200	μA
			Disabled		−25		−25	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX	Driver	−50	−150	−50	−150	mA
			Receiver	−30	−100	−30	−100	mA
I_{CC}	Supply current	V_{CC} = MAX	8T26A		87		87	mA
			8T28		110		110	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

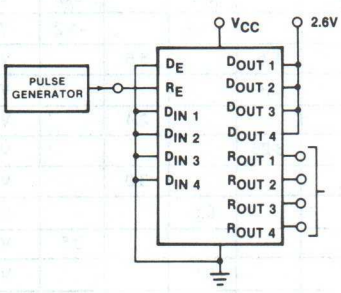
AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

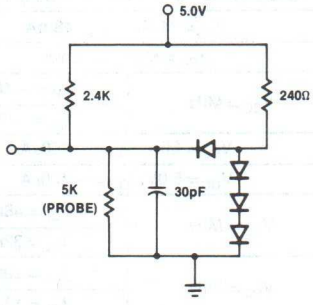
PARAMETER		TEST CONDITIONS	8T26A		8T28		UNIT
			Min	Max	Min	Max	
t_{PHL}	Propagation delay, D_{OUT} to R_{OUT}	C_L = 30pF		14		17	ns
t_{PHL}	Propagation delay, D_{IN} to D_{OUT}	C_L = 300pF		14		17	ns
t_{PLH}	Propagation delay, D_{OUT} to R_{OUT}	C_L = 30pF		14		17	ns
t_{PLH}	Propagation delay, D_{IN} to D_{OUT}	C_L = 300pF		14		17	ns
t_{PZL}	Data enable to Data output, High Z to 0	C_L = 300pF		25		28	ns
t_{PLZ}	Data enable to Data output, 0 to High Z	C_L = 300pF		20		23	ns
t_{PZL}	Receive enable to Receive output, High Z to 0	C_L = 30pF		20		23	ns
t_{PLZ}	Receive enable to Receive output, 0 to High Z	C_L = 30pF		15		18	ns

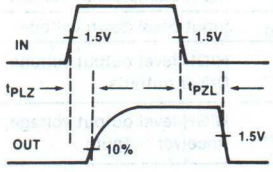
TEST CIRCUITS AND WAVEFORMS

DISABLE AND ENABLE TIME
RECEIVE ENABLE TO RECEIVE OUTPUT

8T26A

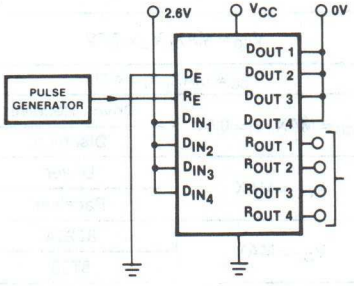




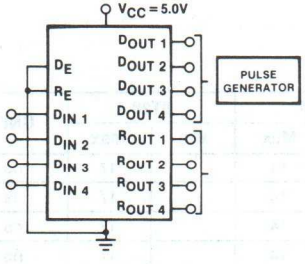


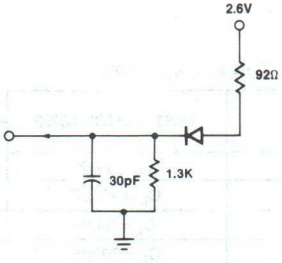
Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 5MHz$ (50% duty cycle)
Amplitude = 2.6V

8T28

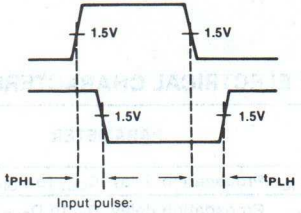


PROPAGATION DELAY
D_{OUT} TO R_{OUT}



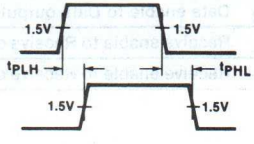


8T26A



Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 10MHz$ (50% duty cycle)
Amplitude = 2.6V

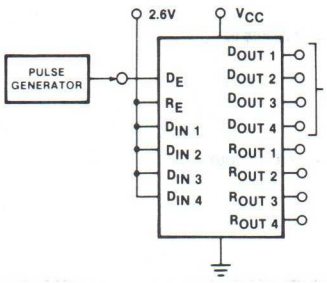
8T28

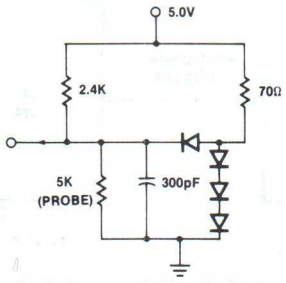


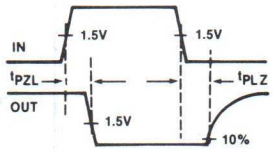
TEST CIRCUITS AND WAVEFORMS (Continued)

DISABLE AND ENABLE TIME
DATA ENABLE TO DATA OUTPUT

8T26A

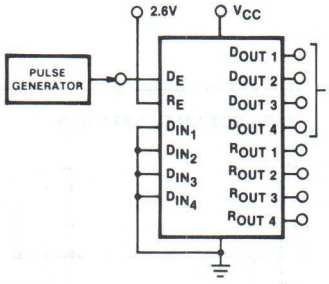




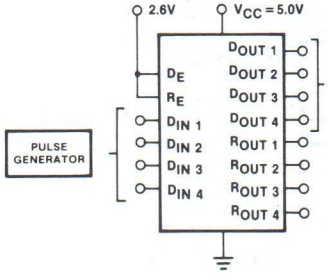


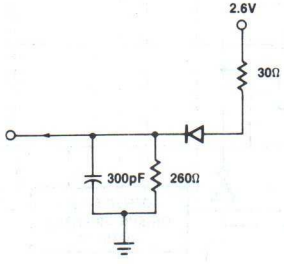
Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
freq = 5MHz (50% duty cycle)
Amplitude = 2.6V

8T28

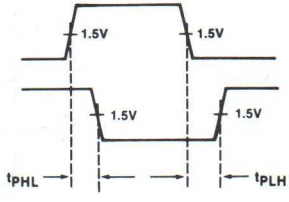


PROPAGATION DELAY
D_{IN} TO D_{OUT}

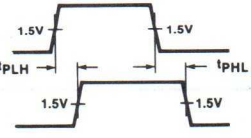




8T26A



8T28

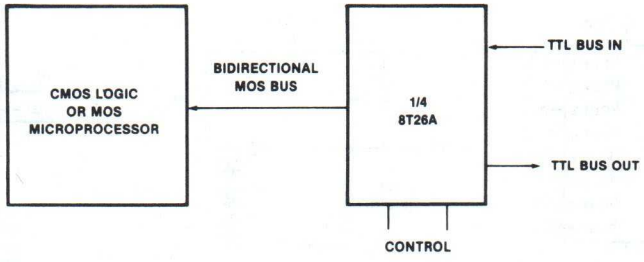


Input pulse:
$t_r = t_f = 5ns$ (10% to 90%)
$f_{req} = 10MHz$ (50% duty cycle)
Amplitude = 2.6V

4

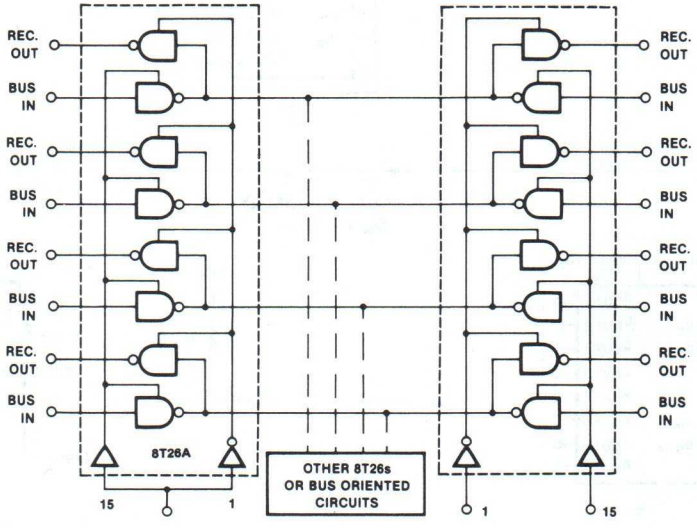
TYPICAL APPLICATION

BIDIRECTIONAL MOS
CMOS to TTL Interface



TYPICAL APPLICATION

BIDIRECTIONAL DATA BUS



Control lines may be tied together, such that logical "1" transmit, logical "0" receive.

Logical "0" = active
Logical "11" = Hi-z

Logical "1" = active
Logical "0" = Hi-z

High Speed Hex 3-State Buffers
High Speed Hex 3-State Inverters

DESCRIPTION

Each of the 3-state bus interface elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL bus levels. For maximum systems flexibility, the 8T95 and 8T97 do so without logic inversion, whereas the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T95	8ns	65mA
N8T96	6.5ns	59mA
N8T97	8ns	65mA
N8T98	6.5ns	59mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8T95N • N8T96N N8T97N • N8T98N	
Ceramic DIP	N8T95F • N8T96F N8T97F • N8T98F	S8T95F • S8T98F S8T97F •

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FUNCTION TABLE—8T95

INPUTS			OUTPUT
DIS_1	DIS_2	I	Y
L	L	L	L
L	L	H	H
X	H	X	(Z)
H	X	X	(Z)

L = LOW voltage level
H = HIGH voltage level
X = Don't care
(Z) = HIGH impedance (off) state

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8T
DIS	Input	1Sul
I	Input	1Sul
Y	Output	24Sul

NOTE
A unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

FUNCTION TABLE—8T96

INPUTS			OUTPUT
DIS_1	DIS_2	I	$\overline{Y}$
L	L	L	H
L	L	H	L
X	H	X	(Z)
H	X	X	(Z)

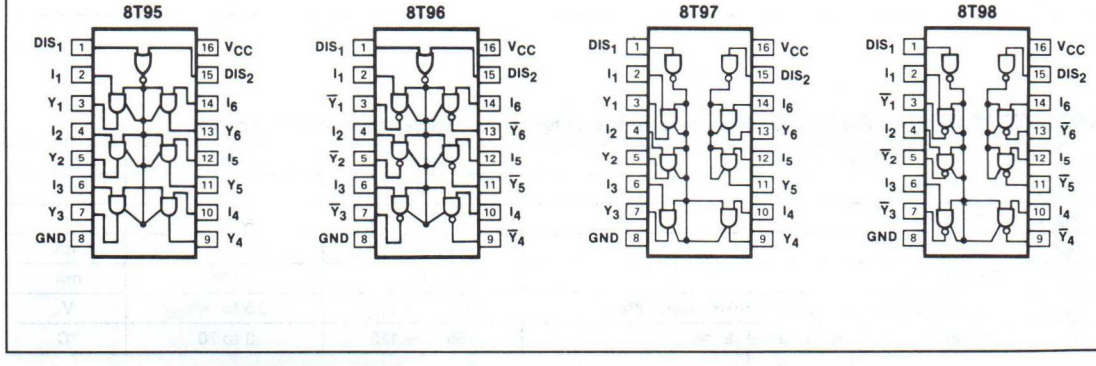
FUNCTION TABLE—8T97

INPUTS		OUTPUT
DIS	I	Y
L	L	L
L	H	H
H	X	(Z)

FUNCTION TABLE—8T98

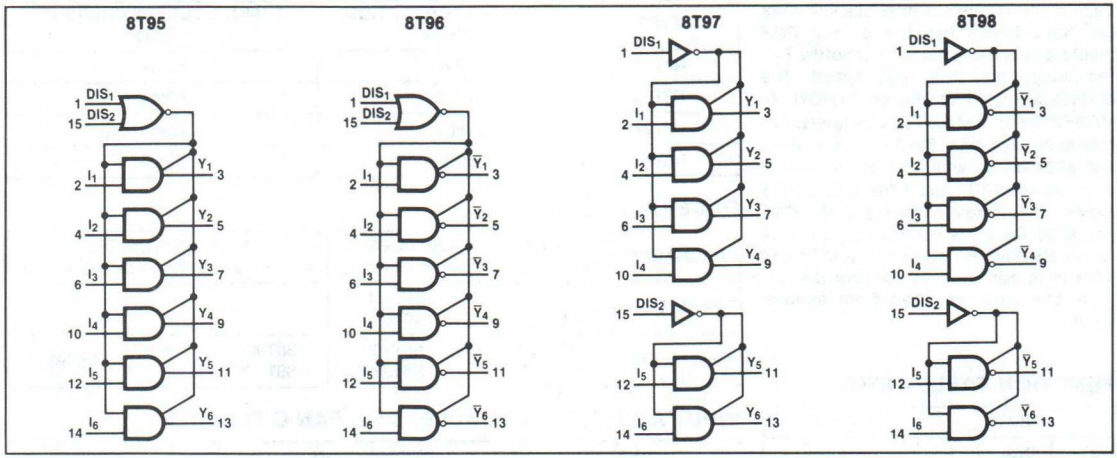
INPUTS		OUTPUT
DIS	I	$\overline{Y}$
L	L	H
L	H	L
H	X	(Z)

PIN CONFIGURATION

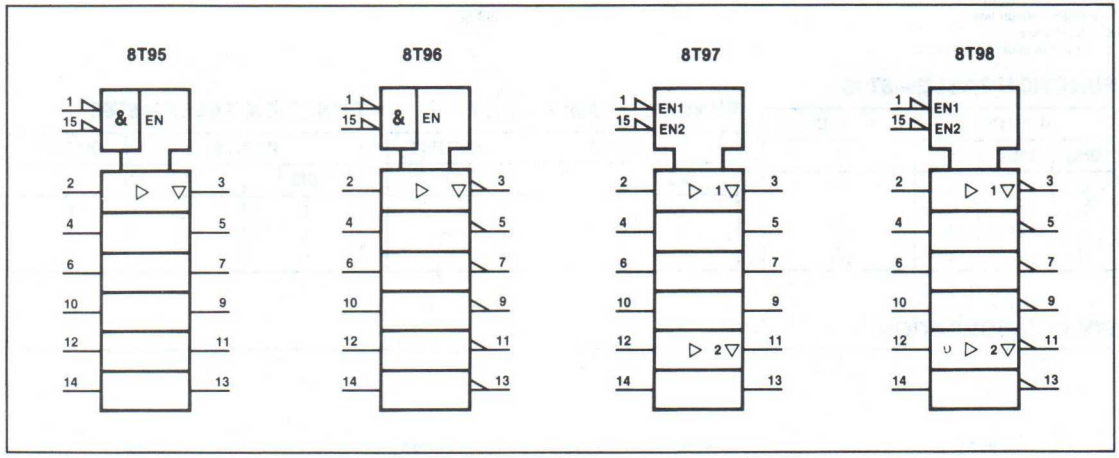


HEX BUFFERS/INVERTERS 8T95, 96, 97, 98

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

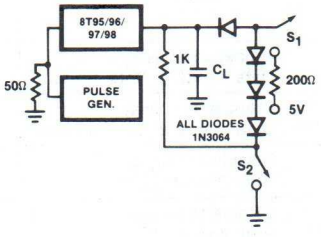
PARAMETER		S8T	N8T	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
I_{OL}	Continuous	100	100	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8T			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IH}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current				−5.2	mA
I_{OL}	LOW-level output current	Mil			48	mA
		Com'l			48	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V for S8T only.

TEST CIRCUIT



Input Characteristics
PA = 3V, = 1MHz $t_r = t_f \leq 10$ns (10% to 90%)
C_L includes probe and jig capacitance.

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted.)

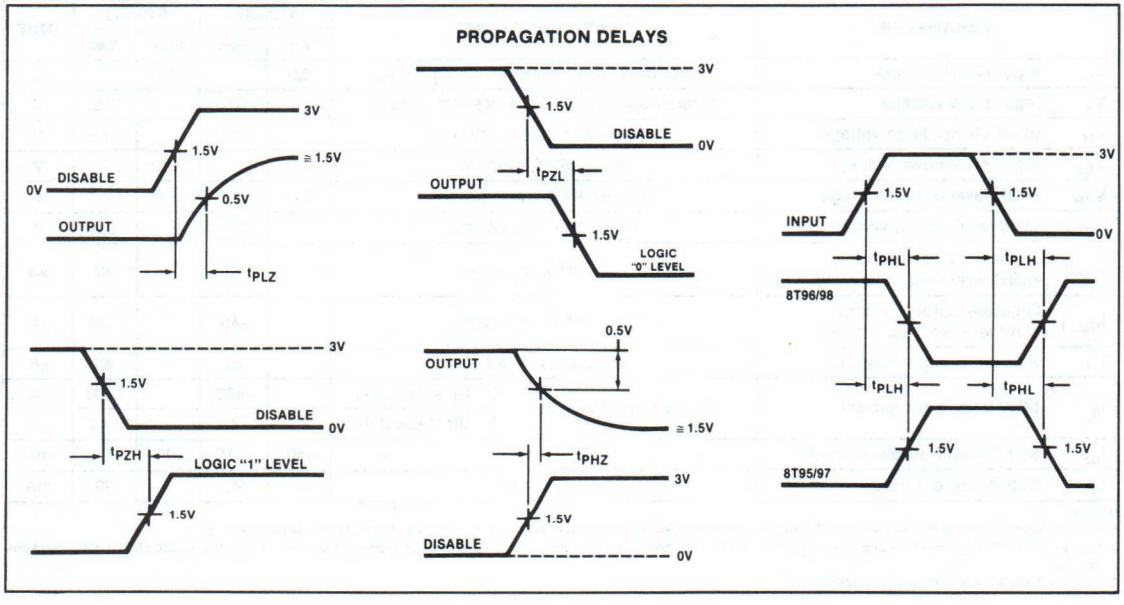
PARAMETER		TEST CONDITIONS[1]		8T95/97		8T96/98		UNIT
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage			0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −12mA			−1.5		−1.5	V
V_{BD}	Input breakdown voltage	V_{CC} = MAX, I_I = 1mA		5.5		5.5		V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = −5.2mA		2.4		2.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = 48mA			0.5[3]		0.5[3]	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V			40		40	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.5V			−40		−40	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V			40		40	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V	Disable = 0.5V		−400		−400	μA
			Disable = 2.0V		−40		−40	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX		−40	−115	−40	−115	mA
I_{CC}	Supply current (total)	V_{CC} = MAX			98		89	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
3. V_{OL} = +0.45V MAX for S8T at T_A = +125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8T95/97 $R_L = 200\Omega$		8T96/98 $R_L = 200\Omega$		UNIT
			Min	Max	Min	Max	
t_{PLH}	Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50pF$	3	12	4	11	ns
t_{PHL}	Propagation delay Data inputs to Data outputs	S_1, S_2 are closed, $C_L = 50pF$	3	13	3	10	ns
t_{PZH}	Disable to outputs High Z to Logic "1"	S_1 is open, S_2 is closed, $C_L = 50pF$	8	25	7	22	ns
t_{PZL}	Disable to outputs High Z to Logic "0"	S_1 is closed, S_2 is open, $C_L = 50pF$	12	25	11	24	ns
t_{PHZ}	Disable to outputs Logic "1" to High Z	S_1, S_2 are closed, $C_L = 5pF$	3	10	3	10	ns
t_{PLZ}	Disable to outputs Logic "0" to High Z	S_1, S_1 are closed, $C_L = 5pF$	3	12	5	16	ns

AC WAVEFORMS



TRANSCEIVER 8T125

Octal 3-State Transceiver

- **Octal bidirectional bus interface**
- **3-State buffer outputs**
- **PNP inputs for reduced loading**
- **Hysteresis on all Data inputs**
- **Pin compatible with 54LS/74LS245**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T125	7.5ns	50mA

DESCRIPTION

The 8T125 is an octal transceiver featuring inverting 3-State bus-compatible outputs in both send and receive directions. The outputs are all capable of sinking 24mA and sourcing up to 15mA, producing very good capacitive drive characteristics. The device features a Chip Enable input for easy cascading and a Send/Receive input for direction control. All Data inputs have hysteresis built in to minimize ac noise effects.

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8T125N	
Ceramic DIP	N8T125F	S8T125F

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{CE}$	S/$\overline{R}$	A_n	B_n
L	L	A = $\overline{B}$	INPUTS
L	H	INPUT	B = $\overline{A}$
H	X	(Z)	(Z)

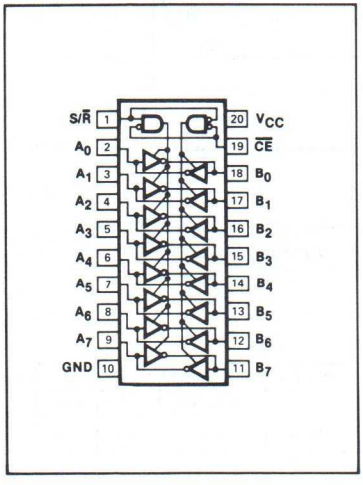
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = HIGH impedance "off" state

INPUT AND OUTUT LOADING AND FAN-OUT TABLE

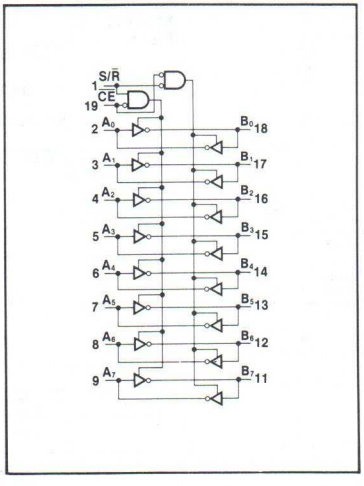
PINS	DESCRIPTION	8T125
All	Inputs	1LSul
All	Outputs	30LSul

NOTE
A unit load (LSul) is 20μA I_{IH} and −0.4mA I_{IL}.

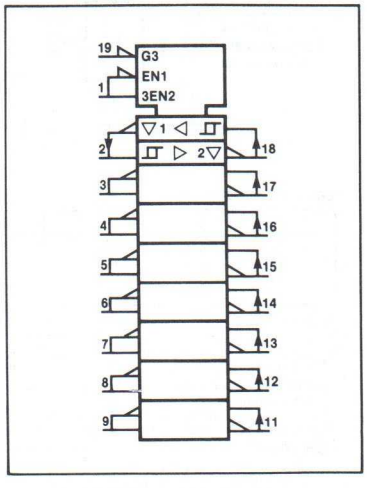
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



TRANSCEIVER 8T125

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

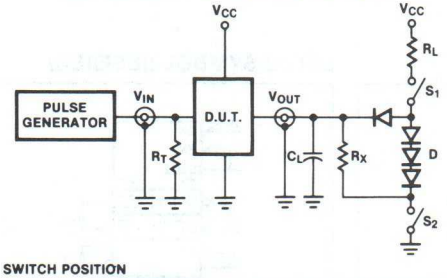
PARAMETER			S8T	N8T	UNIT
V_{CC}	Supply voltage		7.0	7.0	V
V_{IN}	Input voltage	Transceiver inputs	−0.5 to +5.5	−0.5 to +5.5	V
		Non-Transceiver inputs	−0.5 to +7.0	−0.5 to +7.0	V
I_{OL}	Continuous		50	50	m A
I_{IN}	Input current		−30 to +1	−30 to +1	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8T			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.7	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−12	mA
		Com'l			−15	mA
I_{OL}	LOW-level output current	Mil			12	mA
		Com'l			24	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



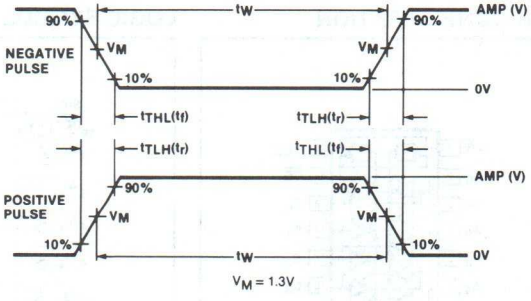
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

TRANSCEIVER 8T125

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8T125 Min	8T125 Max	UNIT
ΔV_T	Hysteresis ($V_{T+}-V_{T-}$)	V_{CC} = MIN			0.2		V
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage			2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage				0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA				−1.5	V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN	I_{OH} = −2.0mA	Mil	2.4		V
			I_{OH} = −3.0mA	Com'l	2.4		V
			I_{OH} = −12mA	Mil	2.0		V
			I_{OH} = −15mA	Com'l	2.0		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN	I_{OL} = 12mA	Mil		0.4	V
				Com'l		0.4	V
			I_{OL} = 24mA	Com'l		0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V				20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_O = 0.4V				−200	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.4V				20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	V_I = 5.5V Transceiver inputs			100	μA
			V_I = 7.0V Non-Transceiver inputs			100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−200	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX			−40	−120	mA
I_{CCH}	Supply current HIGH	V_{CC} = MAX, outputs HIGH				70	mA
I_{CCL}	Supply current LOW	V_{CC} = MAX, outputs LOW				90	mA
I_{CCZ}	Supply current "off"	V_{CC} = MAX, outputs "off"				95	mA

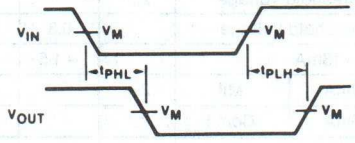
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8T R_L = 667Ω Min	8T R_L = 667Ω Max	UNIT
t_{PLH} t_{PHL}	Propagation delay Input to output	Waveform 1, C_L = 45pF		12 12	ns
t_{PZH}	Enable to HIGH	Waveform 2, C_L = 45pF		40	ns
t_{PZL}	Enable to LOW	Waveform 3, C_L = 45pF		40	ns
t_{PHZ}	Disable from HIGH	Waveform 2, C_L = 5pF		25	ns
t_{PLZ}	Disable from LOW	Waveform 3, C_L = 5pF		25	ns

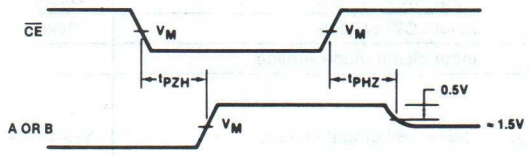
AC WAVEFORMS

WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 1

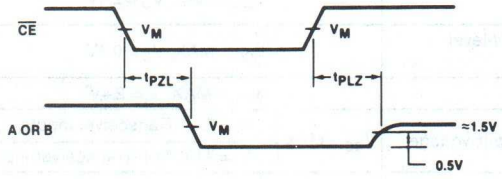
3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 2

$V_M = 1.3V$

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 3

Quad, 3-State Transceivers

DESCRIPTION

The 8T126 through 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-State outputs on both send and receive buffers, and pnp transistors on all inputs to reduce input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS interface applications. The send and receive buffers have separate Enable inputs for independent control.

The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading and a Send/Receive input for direction control.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T126	10ns (Data)	17mA
N8T127	9ns (Data)	21mA
N8T128	10ns (Data)	17mA
N8T129	9ns (Data)	21mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic	N8T126N • N8T127N N8T128N • N8T129N	
Ceramic DIP	N8T126F • N8T127F N8T128F • N8T129F	S8T126F • S8T127F S8T128F • S8T129F
Flatpack		S8T126W • S8T127W S8T128W • S8T129W

FUNCTION TABLES

8T126

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	$A = \overline{B}$	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(X) = HIGH imedance "off" state

8T127

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	$A = \overline{B}$	INPUTS
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

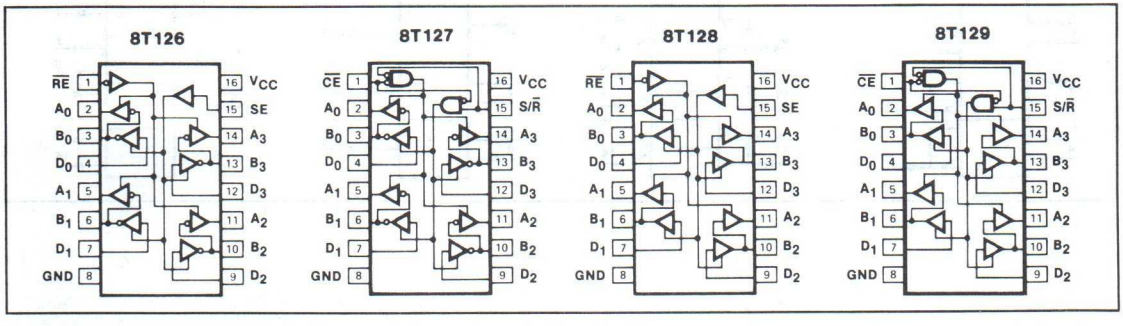
8T128

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

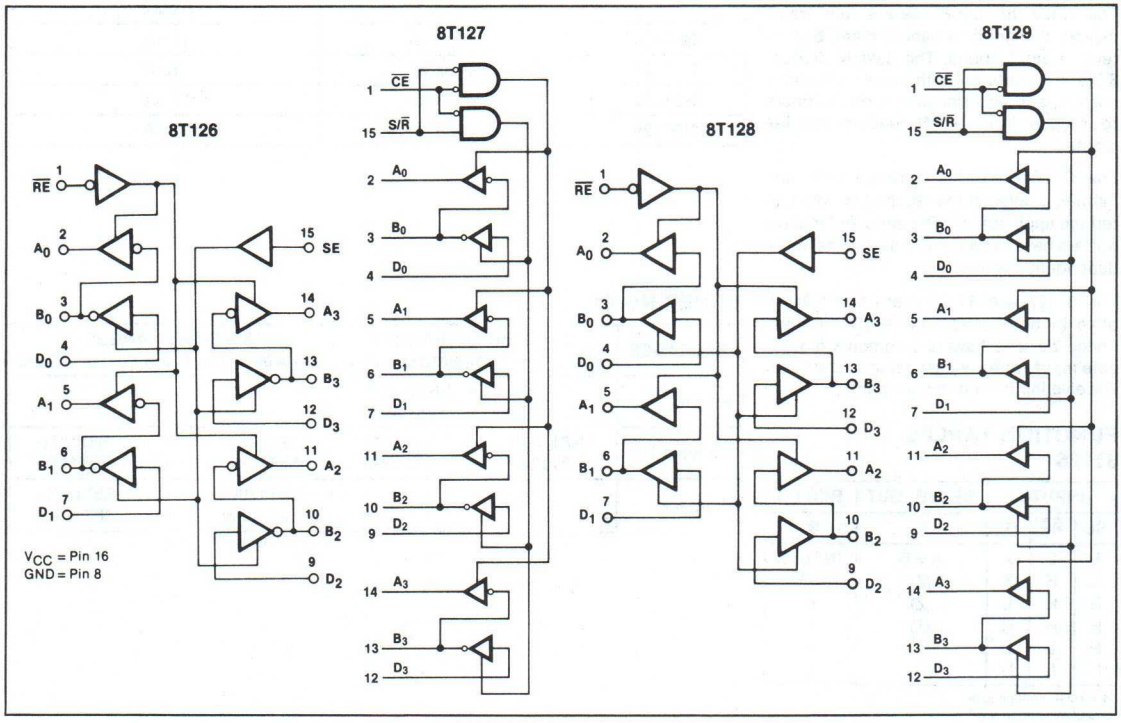
8T129

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

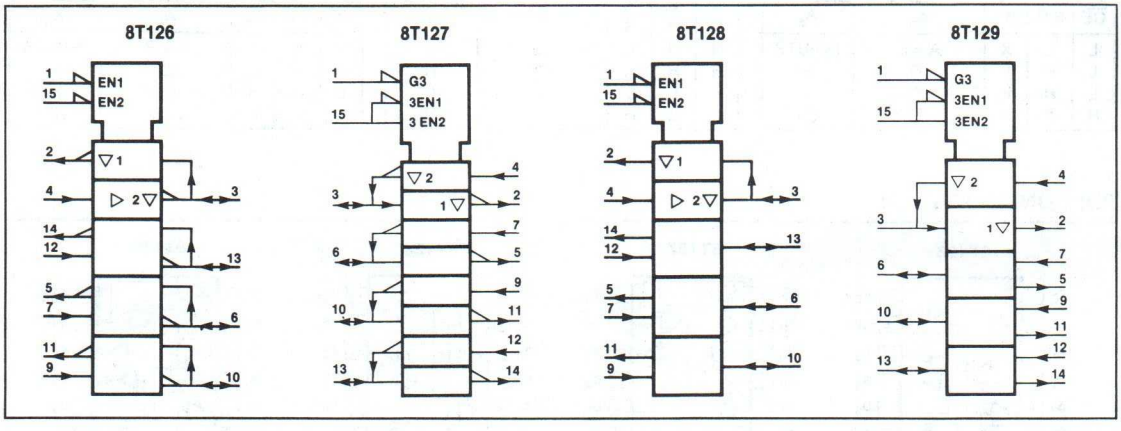
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER			S8T	N8T	UNIT
V_{CC}	Supply voltage		7.0	7.0	V
V_{IN}	Input voltage	Transceiver inputs	−0.5 to +5.5	−0.5 to +5.5	V
		Non-Transceiver inputs	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current		−30 to +1	−30 to +1	mA
I_{OL}	Continuous		50	50	mA
V_{OUT}	Voltage applied to output in HIGH output state		−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range		−55 to +125	0 to 70	°C

4

RECOMMENDED OPERATING CONDITIONS

PARAMETERS				8T126/8T128			8T127/8T129			UNIT
				Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage		Mil	4.5	5.0	5.5	4.5	5.0	5.5	V
			Com'l	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage			2.0			2.0			V
V_{IL}	LOW-level input voltage		Mil			0.7			0.7	V
			Com'l			0.8			0.8	V
I_{IK}	Input clamp current					−18			−18	mA
I_{OH}	HIGH-level output current	Bus	Mil			−2.0			−2.0	mA
			Com'l			−5.2			−5.2	mA
		Receiver	Mil			−1.0			−2.0	mA
			Com'l			−2.6			−5.2	mA
I_{OL}	LOW-level output current	Bus	Mil, Com'l			12			12	mA
			Com'l			24			24	mA
		Receiver	Mil, Com'l			6			12	mA
			Com'l			12			24	mA
T_A	Operating free-air temperature		Mil	−55		+125	−55		+125	°C
			Com'l	0		70	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8T126/8T128		8T127/8T129		UNIT
					Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage			2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage		Mil		0.7		0.7	V
				Com'l		0.8		0.8	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −18mA				−1.5		−1.5	V
V_{OH}	HIGH-level output voltage, Bus outputs	V_{CC} = MIN	I_{OH} = −2.0mA	Mil	2.4		2.4		V
			I_{OH} = −5.2mA	Com'l	2.4		2.4		V
V_{OH}	HIGH-level output voltage, Receiver outputs	V_{CC} = MIN, V_{IN} = V_{IL}, or V_{IH} per Function Table	I_{OH} = −100μA	Mil	3.1				V
			I_{OH} = −100μA	Com'l	3.4				V
			I_{OH} = −1.0mA	Mil	2.4				V
			I_{OH} = −2.0mA	Mil			2.4		V
			I_{OH} = −2.6mA	Com'l	2.4				V
			I_{OH} = −5.2mA	Com'l			2.4		V
V_{OL}	LOW-level output voltage, Bus outputs	V_{CC} = MIN	I_{OL} = 12mA	Mil & Com'l		0.4		0.4	V
			I_{OL} = 24mA	Com'l		0.5		0.5	V
V_{OL}	LOW-level output voltage, Receiver outputs	V_{CC} = MIN	I_{OL} = 6mA	Mil & Com'l		0.4			V
			I_{OL} = 12mA	Mil & Com'l				0.4	V
			I_{OL} = 12mA	Com'l		0.5			V
			I_{OL} = 24mA	Com'l				0.5	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_O = 2.4V				20		20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied, Receiver outputs	V_{CC} = MAX, V_O = 0.4V				−20		−20	μA
I_{OZL}	Off-state output current, LOW-level voltage applied, Bus outputs	V_{CC} = MAX, V_O = 0.4V				−100		−200	μA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20		20	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX	Bus inputs	V_I = 5.5V		100		100	μA
			Others	V_I = 7.0V		100		100	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.4V				−100		−200	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX			−40	−120	−40	−120	mA
I_{CCH}	Supply current HIGH	V_{CC} = MAX, outputs HIGH				26		36	mA
I_{CCL}	Supply current LOW	V_{CC} = MAX, outputs LOW				30		42	mA
I_{CCZ}	Supply current "off"	V_{CC} = MAX, outputs "off"				36		44	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

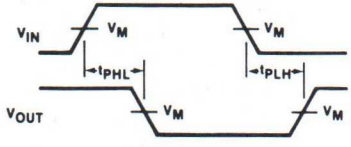
AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to Bus output	Waveforms 1 & 2, $C_L = 100pF$, $R_L = 667\Omega$		20 30		20 30	ns
t_{PLH} t_{PHL}	Propagation delay Bus to Receiver output	Waveforms 1 & 2, $C_L = 50pF$, $R_L = 667\Omega$		20 30		20 25	ns
t_{PZH}	Enable to HIGH for Bus output	Waveform 3, $C_L = 100pF$, $R_L = 667\Omega$		30		35	ns
t_{PZH}	Enable to HIGH for Receiver output	Waveform 3, $C_L = 50pF$, $R_L = 667\Omega$		25		30	ns
t_{PZL}	Enable to LOW for Bus output	Waveform 4, $C_L = 100pF$, $R_L = 667\Omega$		35		35	ns
t_{PZL}	Enable to LOW for Receiver output	Waveform 4, $C_L = 50pF$, $R_L = 667\Omega$		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 3, $C_L = 5pF$, $R_L = 667\Omega$, Com'l		25		25	ns
		Waveform 3, $C_L = 50pF$, $R_L = 667\Omega$, Mil		63		63	ns
		Waveform 3, $C_L = 100pF$, $R_L = 667\Omega$, Mil		102		102	ns
t_{PLZ}	Disable from LOW	Waveform 4, $C_L = 5pF$, $R_L = 667\Omega$, Com'l		25		25	ns
		Waveform 4, $C_L = 50pF$, $R_L = 667\Omega$, Mil		29		29	ns
		Waveform 4, $C_L = 100pF$, $R_L = 667\Omega$, Mil		33		33	ns

4

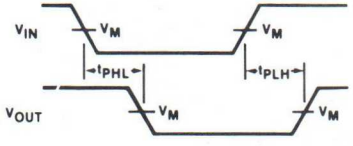
AC WAVEFORMS

WAVEFORM FOR INVERTING OUTPUTS



Waveform 1

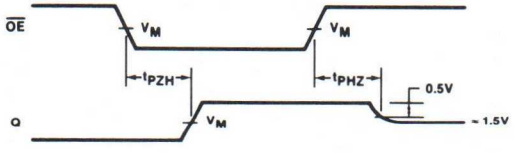
WAVEFORM FOR NON-INVERTING OUTPUTS



Waveform 2

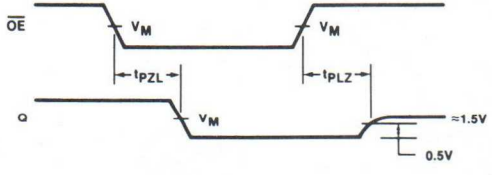
$V_M = 1.3V$

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



Waveform 3

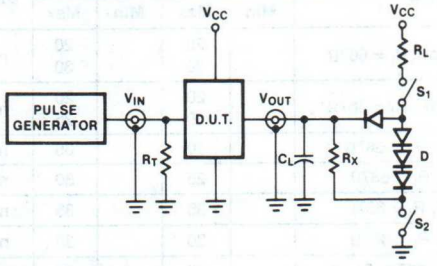
3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



Waveform 4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



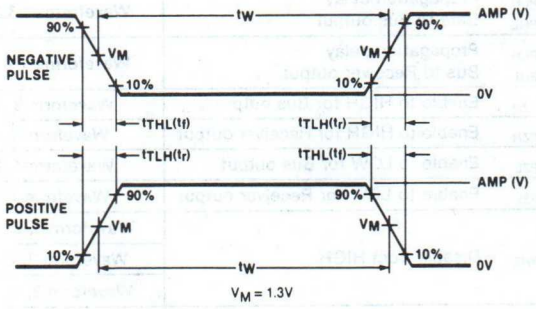
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8T	3.0V	1MHz	500ns	15ns	6ns

BUS RECEIVER 8T380

Quad Bus Receiver with Hysteresis-Schmitt Trigger

DESCRIPTION

The 8T380 is a quad 2-input bus receiver with hysteresis for use in I/O, data, and memory busses. Built-in hysteresis provides maximum noise immunity and a power-up or power-down sequence on the receiver will not affect the bus. LOW input current allows several drivers and receivers to communicate over a common bus in "Party line" fashion. The 8T380 is ideal as a Schmitt Trigger in analog interfaces that cannot tolerate the non-linear input impedance characteristics of standard TTL. Further, the LOW input requirements allow the 8T380 to be used as a CMOS to TTL interface. All inputs have clamping diodes to simplify systems design.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T380	20ns (t_{PLH}) 16ns (t_{PHL})	25mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES $V_{CC} = 5V \pm 5\%$; $T_A = 0°C$ to $+70°C$
Plastic DIP	N8T380N
Ceramic DIP	N8T380F

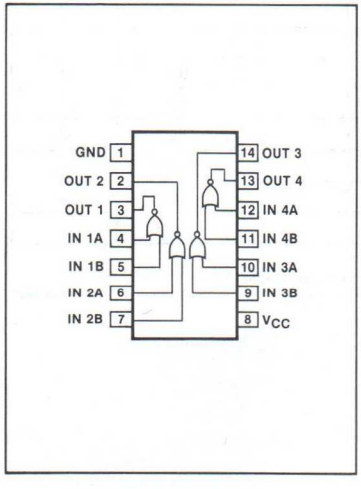
4

FUNCTION TABLE

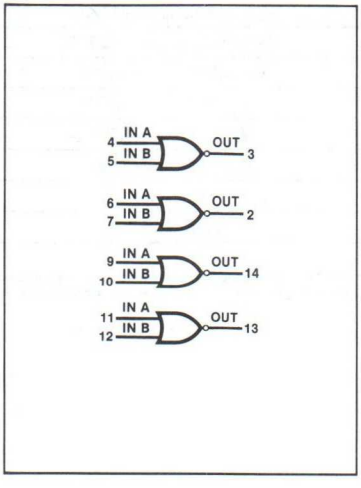
INPUTS		OUTPUT
A	B	OUT
L	L	H
L	H	L
H	L	L
H	H	L

H = HIGH voltage level
L = LOW voltage level

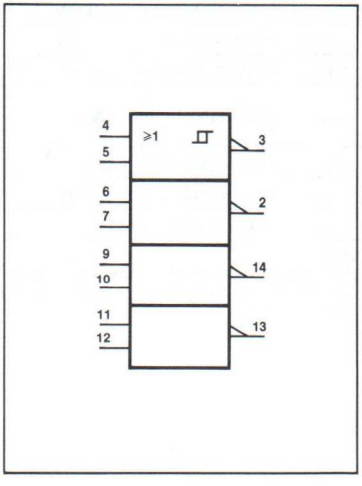
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



BUS RECEIVER 8T380

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

PARAMETER		8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{OL}	Continuous	30	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0		2.5	V
V_{IL}	LOW-level input voltage	1.1		1.5	V
I_{IK}	Input clamp current			−12	mA
I_{OH}	HIGH-level output current			−400	μA
I_{OL}	LOW-level output current			16	mA
T_A	Operating free-air temperature	0		70	°C

DC CHARACTERISTICS (Over recommended operating free-air temperature range, unless otherwise noted).

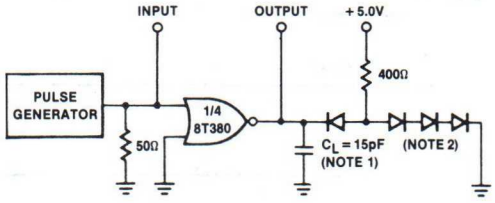
PARAMETER		TEST CONDITIONS[1]	8T380		UNIT
			Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage	2.0	2.5	V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage	1.1	1.5	V
V_{IK}	Input clamp diode voltage	V_{CC} = MIN, I_{IK} = −12mA		−1.5	V
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, I_{OH} = −400μA	2.4		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, I_{OL} = 16mA		0.4	V
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 4.5V		50	μA
		V_{CC} = 0V, V_I = 4.5V		50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0V		−25	μA
I_{OS}	Short-circuit output current[2]	V_{CC} = MAX	−18	−55	mA
I_{CC}	Supply current (total)	V_{CC} = 5.25V		40	mA

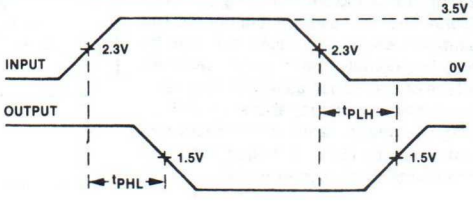
NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER	TEST CONDITIONS	8T $C_L = 15pF$, $R_L = 400\Omega$		UNIT
		Min	Max	
t_{PLH} Propagation delay t_{PHL} Input to output	See Test Circuits and Waveforms		35 35	ns

TEST CIRCUITS AND WAVEFORMS





NOTES:
1. Including probe and jig capacitance
2. All diodes are 1N3064
3. Pulse generator characteristics

P.A. = 3.5V
$Z_{OUT} = 50\Omega$
$P_{RR} = 1MHz$
$t_r = t_f \leq 10ns$ (10% to 90%)
Duty Cycle = 50%

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BUS RECEIVER 8T380

TYPICAL APPLICATIONS

A generalized "Party Line" bus interface is shown in Figure 1. Each driver/receiver combination can communicate with any other pair or all. Open collector NAND Gates such as the Signetics 7439 have adequate drive capability for the bus terminations as well as 20 driver/receiver pairs. In addition the bussing scheme is non-inverting as shown and bus drivers are activated by a logic "1" whereas bus receivers are activated by a Logic "0."

Each termination consisting of a 180 ohm resistor to V_{CC} and 390 ohm to ground is a 120 ohm Thevenin's equivalent circuit. The maximum length of cable that can be driven is a complex relationship involving the type of cable used as well as the distribution of drivers and receivers on the bus. Using flat ribbon cable, a maximum reasonable length is 50 ft. minus the combined length of all taps or stubs.

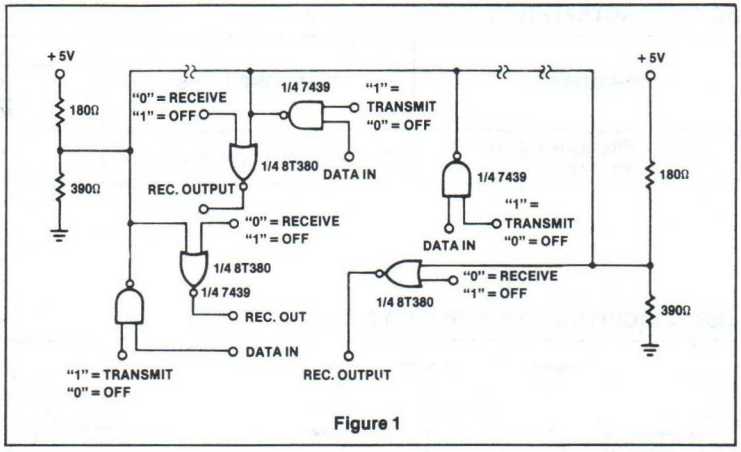
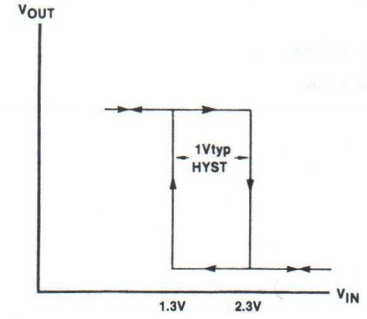


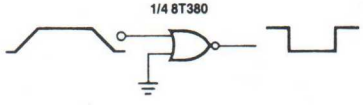
Figure 1

SCHMITT TRIGGER

The receiver transfer curve shown in Figure 2a makes the 8T380 ideal in a variety of Schmitt Trigger and waveshaping applications such as Figure 2b.



a.



b.

Figure 2

MOS/C-MOS INTERFACE

The input current which is only 50μA MAX in the logical "1" state and no current in the logical "0" state marks the 8T380 an ideal MOS/C-MOS interface element.

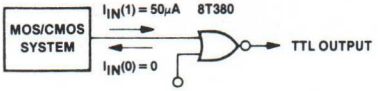


Figure 3

LATCH 8T3404

High Speed 6-Bit Latch

- **Low input load current: .25mA max., 1/6 standard TTL input load**
- **Minimum line reflection: low voltage diode input clamp**
- **Outputs sink 10mA min.**
- **16-pin dual in-line package**
- **Simple expansion: enable inputs**
- **12ns max. data to output delay over 0°C to 75°C temperature**
- **Directly compatible with DTL and TTL logic circuits**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
N8T3404	6ns (Data) 8ns (Write Enable)	47mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +75°C
Plastic DIP	N8T3404N
Ceramic DIP	N8T3404F

FUNCTION TABLE

MODE	INPUTS		OUTPUTS
	$\overline{W}$	D	$\overline{Q}$
Write Latches	L L	L H	H L
Latch Inputs	H H	l h	H L

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH $\overline{W}$ transition.
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH $\overline{W}$ transition.

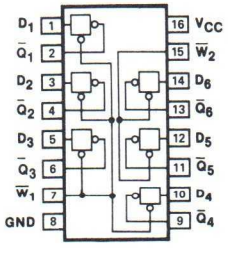
4

DESCRIPTION

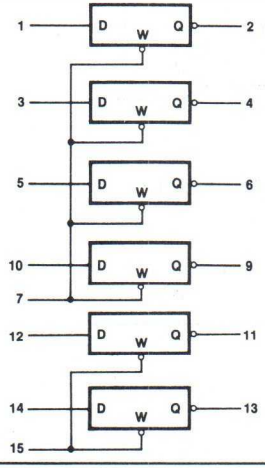
The Signetics 8T3404 contains six high speed latches organized as independent 2-bit and 4-bit latches. They are designed for use as memory address registers, data registers, or other storage elements. The latches act as high speed inverters when the "Write" input is "low."

The 8T3404 is packaged in a standard 16-pin dual in-line package; and its performance is specified over the temperature range of 0°C to +75°C, ambient. To obtain fast switching speeds resulting in higher performance than equivalent devices made with a gold diffusion process, Schottky barrier diode clamped transistors are used.

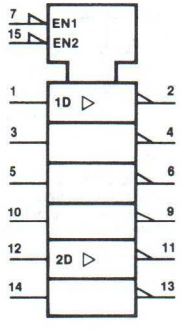
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted).

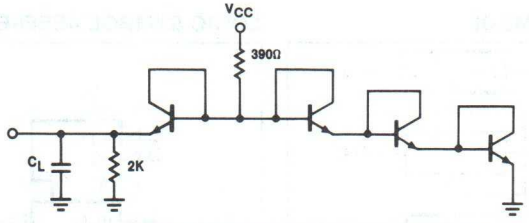
PARAMETER		N8T	UNIT
V_{CC}	Supply voltage	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	V
I_{IN}	Input current	−30mA to +100μA	
I_{OL}	Continuous	100	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	0 to 75	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		8T			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
V_{IH}	HIGH-level output voltage	2.0			V
V_{IL}	LOW-level input voltage			+0.8	V
I_C	Input clamp current			−5.0	mA
I_{OH}	HIGH-level output current			−1.5	mA
I_{OL}	LOW-level output current			40	mA
T_A	Operating free-air temperature	0		75	°C

TEST LOAD CIRCUIT

8T3404 6-BIT LATCH (Switching Characteristics)



ALL TRANSISTORS 2N2369 OR EQUIVALENT, C_L = 30pF

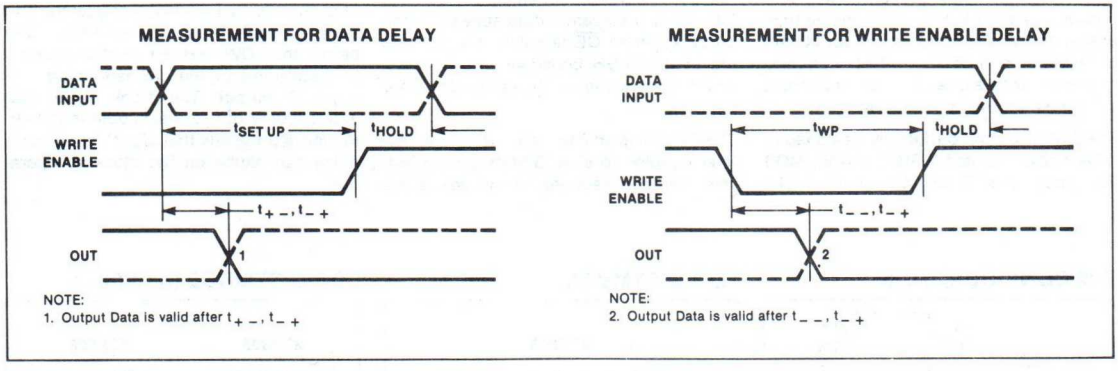
NOTE
CONDITIONS OF TEST:
Input pulse amplitudes: 3.0V
Input rise and fall times: 5ns between 10% and 90%
Measurements are made at 1.5V

DC CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$

PARAMETER		TEST CONDITIONS[1]	8T3404			UNIT
			Min	Typ	Max	
I_F	Input load current	$V_{CC} = 5.25V$, $V_F = 0.45V$			– 0.25	mA
I_R	Input leakage current	$V_{CC} = 5.25V$, $V_R = 5.25V$			10	μA
V_C	Input forward clamp voltage	$V_{CC} = 4.75V$, $I_C = -5.0mA$			– 1.0	V
V_{OL}	Output LOW voltage	$V_{CC} = 4.75V$, $I_{OL} = 10.0mA$			0.45	V
V_{OH}	Output HIGH voltage	$V_{CC} = 4.75V$, $I_{OH} = -1.5mA$	2.4			V
V_{IL}	Input LOW voltage	$V_{CC} = 5.0V$			0.85	V
V_{IH}	Input HIGH voltage	$V_{CC} = 5.0V$	2.0			V
I_{SC}	Output HIGH short circuit current[2]	$V_{CC} = 5.0V$	– 40		– 120	mA
V_{OX}	Output LOW voltage @ HIGH current	$V_{CC} = 5.0V$, $I_{OX} = 40mA$			0.8	V
I_{CC}	Power supply current	$V_{CC} = 5.25V$			75	mA
I_{FW1}	Write enable load current Pin 7	$V_{CC} = 5.25V$, $V_W = 0.45V$			– 1.00	mA
I_{FW2}	Write enable load current Pin 15	$V_{CC} = 5.25V$, $V_W = 0.45V$			– 0.50	mA
I_{RW}	Write enable leakage current	$V_R = 5.25V$			10	μA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. I_{SC} is tested with $V_{OUT} = +0.5V$ and $V_{CC} = V_{CC}$ MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

AC WAVEFORMS



AC CHARACTERISTICS $T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0V \pm 5\%$; unless otherwise specified.

PARAMETER		TEST CONDITIONS		8T			UNIT
				Min	Typ	Max	
t_{+-}, t_{-+}	Data to output delay					12	ns
t_{--}, t_{-+}	Write enable to output delay					17	ns
$t_{set\text{-}up}$	Time data must be present before rising edge of write enable			12			ns
t_{hold}	Time data must remain after rising edge of write enable			8			ns
t_{WP}	Write enable pulse width			15			ns
C_{IND}	Data input capacitance	3404N 3404F	f = 1MHz, $V_{CC} = 0V$ $V_{BIAS} = 2.0V$, $T_A = 25°C$		4 5		pF pF
C_{INW}	Write enable capacitance	3404N 3404F	f = 1MHz, $V_{CC} = 0V$ $V_{BIAS} = 2.0V$, $T_A = 25°C$		7 8		pF pF

8TS805 Octal Transparent Latch With 3-State Outputs
8TS806 Octal D Flip-Flop With 3-State Outputs

- **8-bit transparent latch — 8TS805**
- **8-bit positive, edge-triggered register — 8TS806**
- **3-State output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS805	10ns	105mA
8TS806	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ± 10%; T_A = −55°C to +125°C
Plastic DIP	N8TS805N • N8TS806N	
Ceramic DIP	N8TS805F • N8TS806F	S8TS805F • S8TS806F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

The 8TS805 is an octal, transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

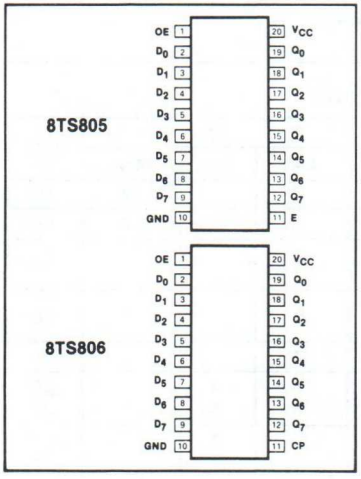
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

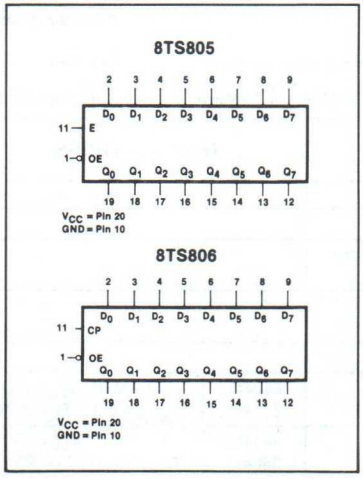
The 8TS806 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

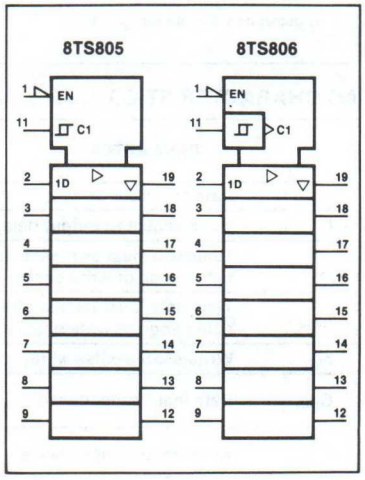
PIN CONFIGURATION



LOGIC SYMBOL

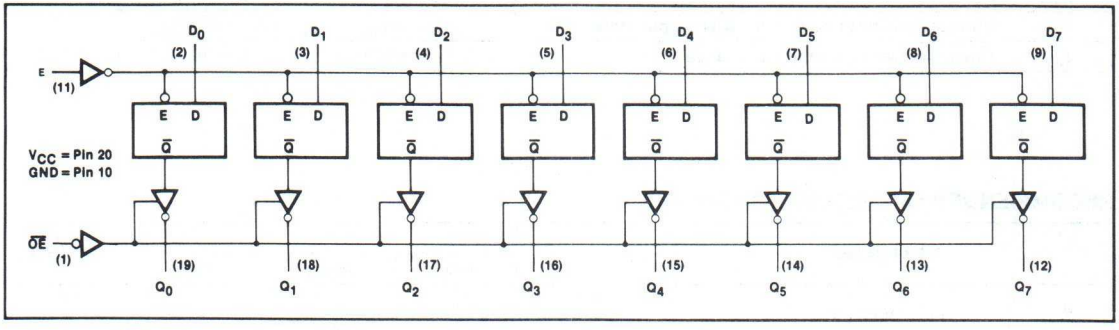


LOGIC SYMBOL (IEEE/IEC)

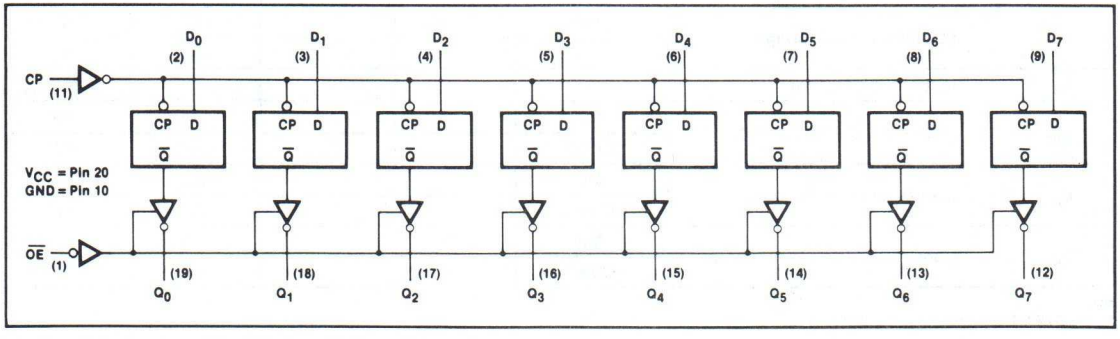


The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS805



LOGIC DIAGRAM, 8TS806



MODE SELECT—FUNCTION TABLE, 8TS805

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	L H
Latch and read register	L L	L L	l h	L H	L H
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

MODE SELECT—FUNCTION TABLE, 8TS806

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L L	↑ ↑	l h	L H	L H
Load register and disable outputs	H H	↑ ↑	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition or HIGH-to-LOW OE transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state.	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS805, 806 Min	8TS805, 806 Typ[2]	8TS805, 806 Max	UNIT
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCL}	8TS805		105	160	mA
			I_{CCL}	All inputs grounded, 8TS806		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.5V, D inputs = GND, 8TS806		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

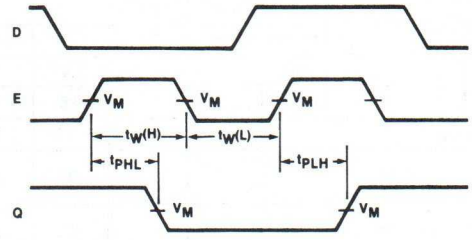
AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8TS C_L = 15pF, R_L = 280Ω Min	8TS C_L = 15pF, R_L = 280Ω Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 6, 8TS806	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 8TS805		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 8TS805		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 8TS806		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3 8TS805 8TS806		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		12	ns

NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

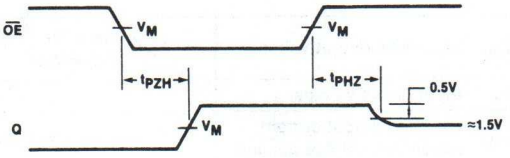
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



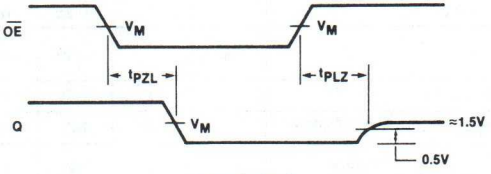
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



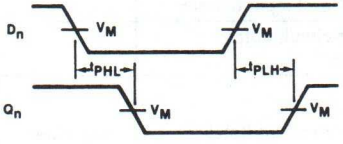
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



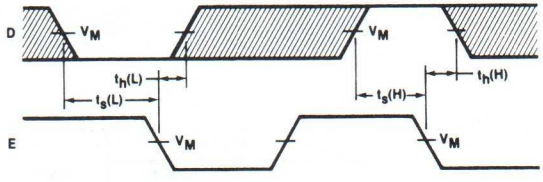
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



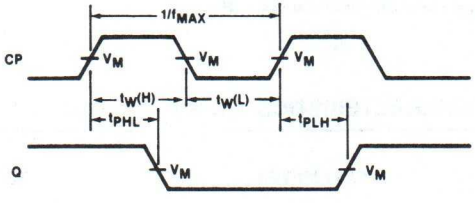
Waveform 4

DATA SETUP AND HOLD TIMES



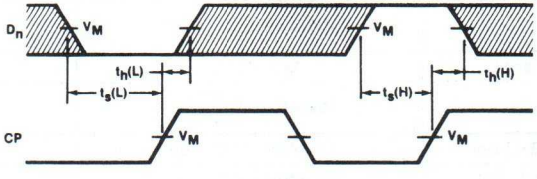
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

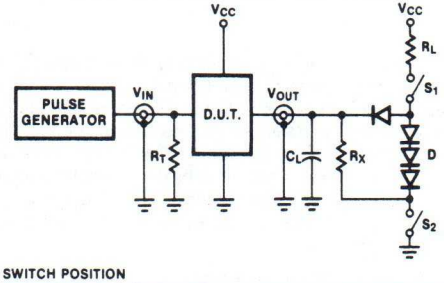
AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS		UNIT
			Min	Max	
$t_{W(H)}$ $t_{W(L)}$	Latch Enable pulse width	Waveform 1, 8TS805	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, 8TS805	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, 8TS805	10		ns
$t_{W(H)}$ $t_{W(L)}$	Clock pulse width	Waveform 6, 8TS806	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, 8TS806	5		ns
t_h	Hold time, Data to Clock	Waveform 7, 8TS806	2		ns

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



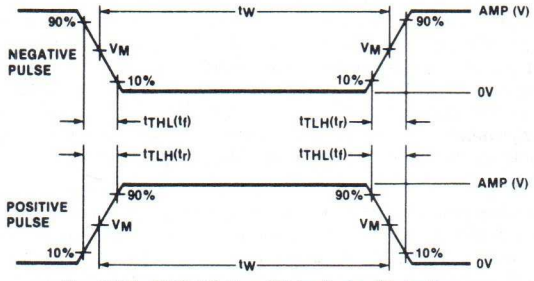
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

'807 Octal Transparent Latch With 3-State Outputs
'808 Octal D Flip-Flop With 3-State Outputs

- **8-bit transparent latch — 8TS807**
- **8-bit positive, edge-triggered register — 8TS808**
- **3-State inverting output buffers**
- **Common 3-State Output Enable**
- **Independent register and 3-State buffer operation**

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS807	10ns	105mA
8TS808	8ns	116mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8TS807N • N8TS808N	
Ceramic DIP	N8TS807F • N8TS808F	S8TS807F • S8TS808F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

DESCRIPTION

The 8TS807 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

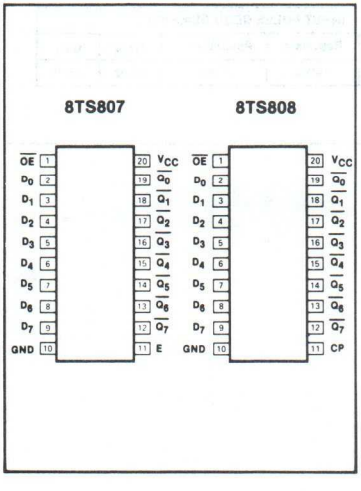
The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

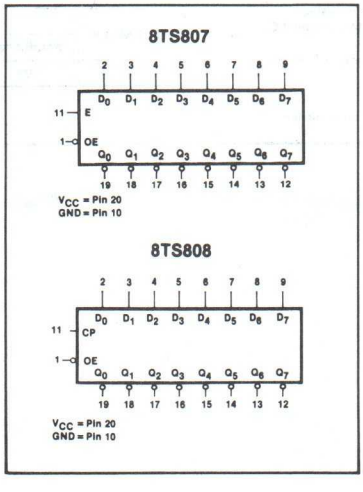
The 8TS808 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The clock buffer has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the clocking operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The

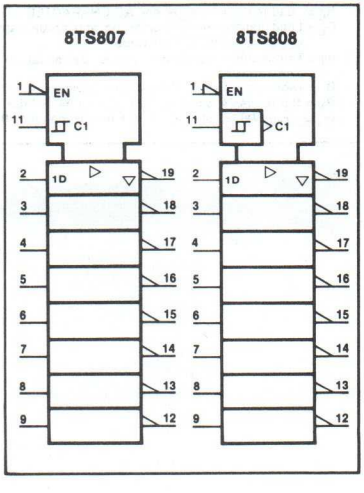
PIN CONFIGURATION



LOGIC SYMBOL

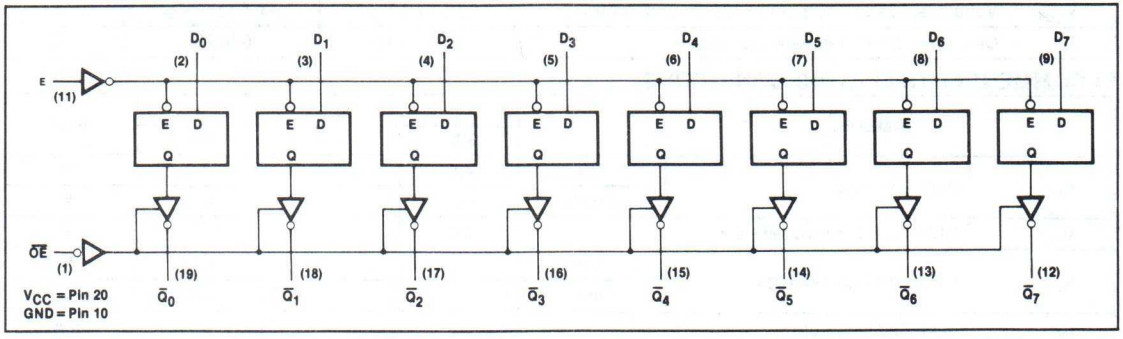


LOGIC SYMBOL (IEEE/IEC)

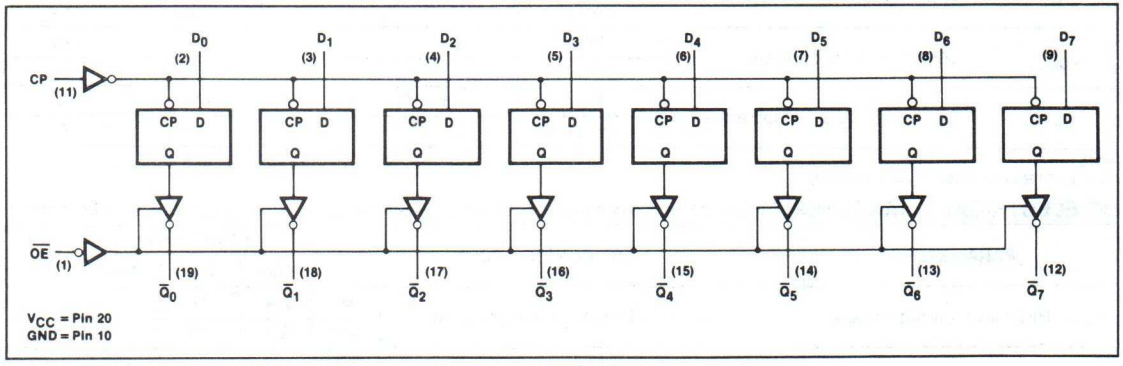


active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is LOW, the data in the register appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

LOGIC DIAGRAM, 8TS807



LOGIC DIAGRAM, 8TS808



MODE SELECT—FUNCTION TABLE, 8TS807

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L	H	L	L	H
	L	H	H	H	L
Latch and read register	L	L	l	L	H
	L	L	h	H	L
Latch register and disable outputs	H	L	l	L	(Z)
	H	L	h	H	(Z)

MODE SELECT—FUNCTION TABLE, 8TS808

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load and read register	L	↑	l	L	H
	L	↑	h	H	L
Load register and disable outputs	H	↑	l	L	(Z)
	H	↑	h	H	(Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+0.8	V
		Com'l			+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Mil			−2.0	mA
		Com'l			−6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = +0.7V MAX for S8TS at T_A = +125°C only.

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS807, 808			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					−1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					−0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current (total)	V_{CC} = MAX	I_{CCL}	8TS807		105	160	mA
			I_{CCL}	All inputs grounded, 8TS808		102	140	mA
			I_{CCZ}	CP, $\overline{OE}$ = 4.5V, D inputs = GND, 8TS807		131	180	mA

NOTES
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

AC CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS $C_L = 15pF$, $R_L = 280\Omega$ Min	8TS $C_L = 15pF$, $R_L = 280\Omega$ Max	UNIT
f_{MAX}	Maximum clock frequency	Waveform 6, 8TS808	75		MHz
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1, 8TS807		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4, 8TS807		9 13	ns
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 6, 8TS808		15 17	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3 8TS807 8TS808		18 18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, $C_L = 5pF$		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, $C_L = 5pF$		12	ns

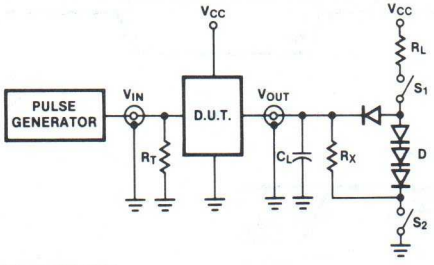
NOTE
Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

AC SETUP REQUIREMENTS $T_A = 25°C$, $V_{CC} = 5.0V$

PARAMETER		TEST CONDITIONS	8TS Min	8TS Max	UNIT
$t_W(H)$ $t_W(L)$	Latch Enable pulse width	Waveform 1, 8TS807	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5, 8TS807	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5, 8TS807	10		ns
$t_W(H)$ $t_W(L)$	Clock pulse width	Waveform 6, 8TS808	6 7.3		ns
t_s	Setup time, Data to Clock	Waveform 7, 8TS808	5		ns
t_h	Hold time, Data to Clock	Waveform 7, 8TS808	2		ns

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS

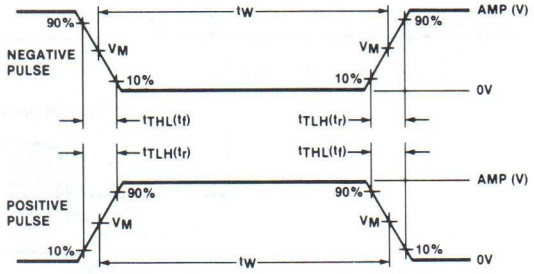


SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS
R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS

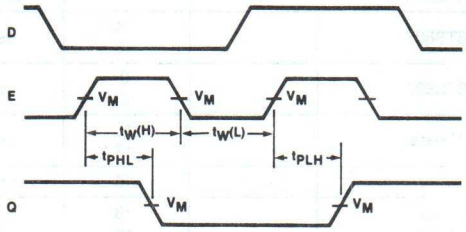


V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

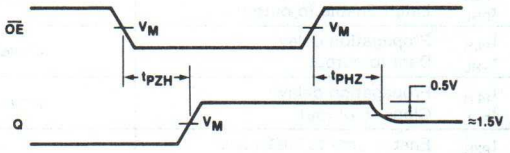
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



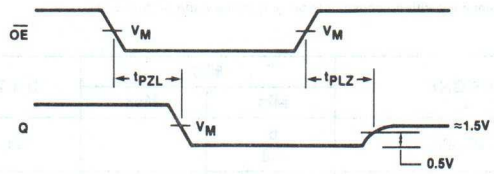
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



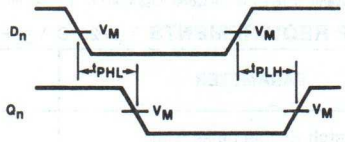
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



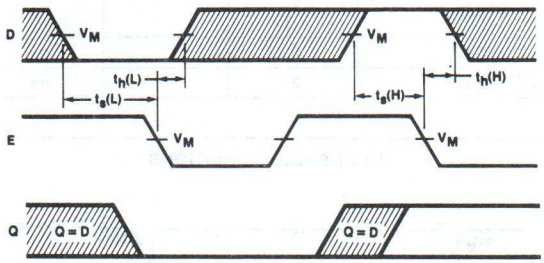
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



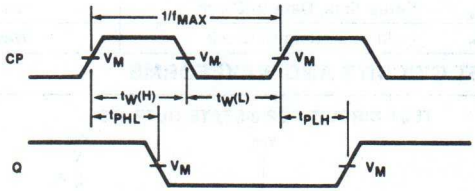
Waveform 4

DATA SETUP AND HOLD TIMES



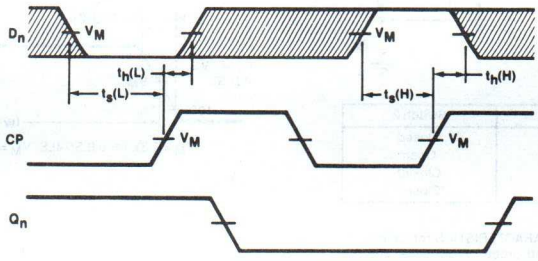
Waveform 5

CLOCK TO OUTPUT DELAYS AND CLOCK PULSE WIDTH



Waveform 6

DATA SETUP AND HOLD TIMES



Waveform 7

V_M = 1.5V for 54/74 and 54S/74S, V_M = 1.3V for 54LS/74LS.
The shaded areas indicate when the input is permitted to change for predictable output performance.

LATCH 8TS809

Octal Transparent Latch With Inverting 3-State Outputs

- 8-bit transparent latch
- 3-State inverting output buffers
- Common 3-State Output Enable
- Independent register and 3-State buffer operation

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (Total)
8TS809	10ns	105mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ±5%; T_A = 0°C to +70°C	MILITARY RANGES V_{CC} = 5V ±10%; T_A = −55°C to +125°C
Plastic DIP	N8TS809N	
Ceramic DIP	N8TS809F	S8TS809F

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	8TS
All	Inputs	1Sul
All	Outputs	10Sul

NOTE
An 8TS unit load (Sul) is 50μA I_{IH} and −2.0mA I_{IL}.

4

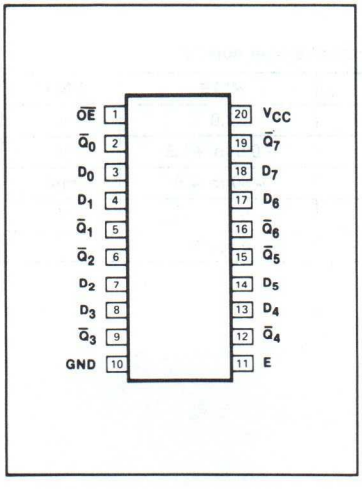
DESCRIPTION

The 8TS809 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Latch Enable (E) and Output Enable ($\overline{OE}$) control gates.

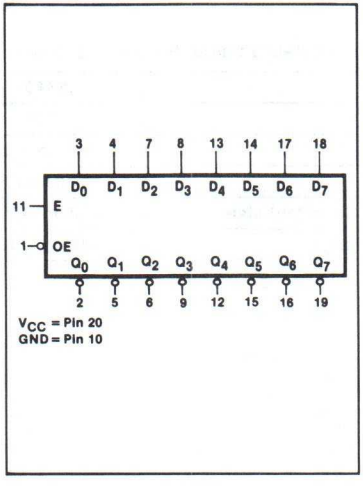
The data on the D inputs are transferred to the inverting latch outputs when the Latch Enable (E) input is HIGH. The latch remains transparent to the data inputs while E is HIGH, and stores the data present one setup time before the HIGH-to-LOW enable transition. The enable gate has about 400mV of hysteresis built in to help minimize problems that signal and ground noise can cause on the latching operation.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active LOW Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation. When $\overline{OE}$ is LOW, the latched or transparent data appears at the outputs. When $\overline{OE}$ is HIGH, the outputs are in the HIGH impedance "off" state, which means they will neither drive nor load the bus.

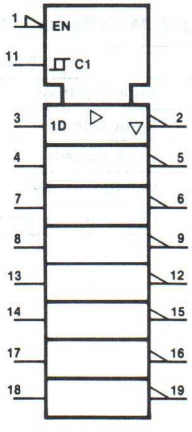
PIN CONFIGURATION



LOGIC SYMBOL

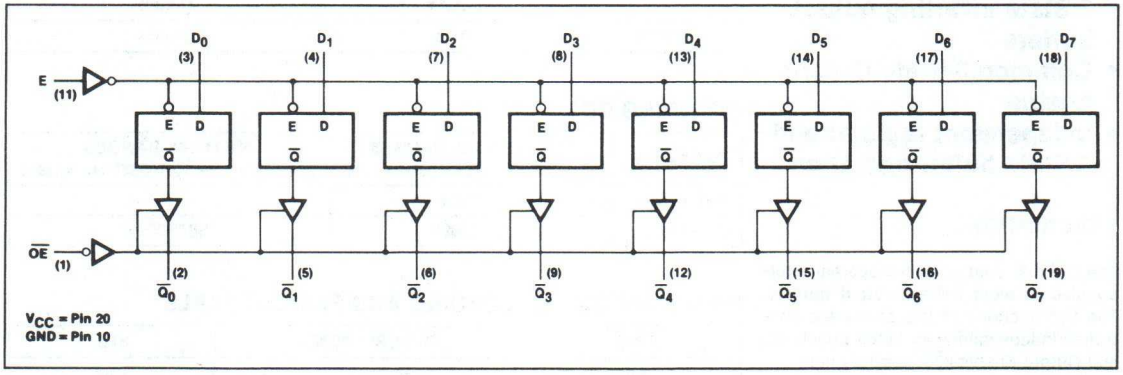


LOGIC SYMBOL (IEEE/IEC)



LATCH 8TS809

LOGIC DIAGRAM



MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	E	D_n		Q_0-Q_7
Enable and read register	L L	H H	L H	L H	H L
Latch and read register	L L	L L	l h	L H	H L
Latch register and disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = HIGH impedance (off) state

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		S8TS	N8TS	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +5.5	−0.5 to +5.5	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

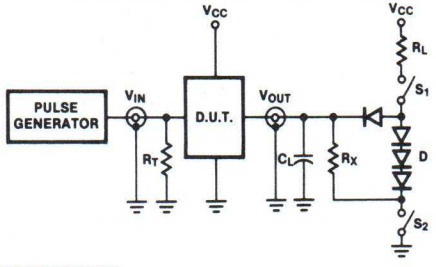
PARAMETER			8TS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage	Mil			+ 0.8	V
		Com'l			+ 0.8	V
I_{IK}	Input clamp current				− 18	mA
I_{OH}	HIGH-level output current	Mil			− 2.0	mA
		Com'l			− 6.5	mA
I_{OL}	LOW-level output current	Mil			20	mA
		Com'l			20	mA
T_A	Operating free-air temperature	Mil	− 55		+ 125	°C
		Com'l	0		70	°C

NOTE
V_{IL} = + 0.7V MAX for S8TS at T_A = + 125°C only.

4

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUIT FOR 3-STATE OUTPUTS



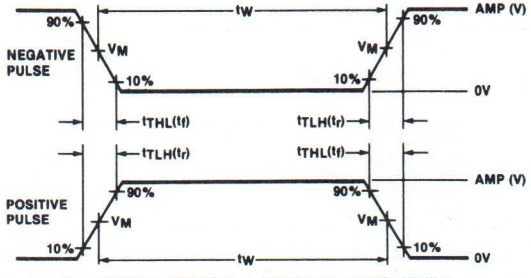
SWITCH POSITION

Test	Switch 1	Switch 2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed

DEFINITIONS

R_L = Load resistor to V_{CC}; see AC CHARACTERISTICS for value.
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
R_X = 1kΩ for 54/74, 54S/74S, R_X = 5kΩ for 54LS/74LS.
t_{TLH}, t_{THL} Values should be less than or equal to the table entries.

INPUT PULSE DEFINITIONS



V_M = 1.3V for 54LS/74LS; V_M = 1.5V for all other TTL families.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
8TS	3.0V	1MHz	500ns	2.5ns	2.5ns

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]			8TS809			UNIT
					Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX, I_{OH} = MAX		Mil	2.4	3.0		V
				Com'l	2.4	3.1		V
V_{OL}	LOW-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	I_{OL} = MAX	Mil			0.5[4]	V
				Com'l			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}					-1.2	V
I_{OZH}	Off-state output current, HIGH-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 2.4V					50	μA
I_{OZL}	Off-state output current, LOW-level voltage applied	V_{CC} = MAX, V_{IH} = MIN, V_O = 0.5V					-50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V					1.0	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V					50	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V					-0.25	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX			-40		-100	mA
I_{CCL}	Supply current (total)	V_{CC} = MAX				105	160	mA

NOTES

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. V_{OL} = +0.45V MAX for S8TS at T_A = +125°C only.

AC CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

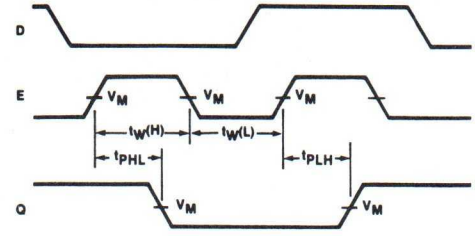
PARAMETER		TEST CONDITIONS	8TS		UNIT
			C_L = 15pF, R_L = 280Ω		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Latch Enable to output	Waveform 1		14 18	ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 4		9 13	ns
t_{PZH}	Enable time to HIGH level	Waveform 2		15	ns
t_{PZL}	Enable time to LOW level	Waveform 3		18	ns
t_{PHZ}	Disable time from HIGH level	Waveform 2, C_L = 5pF		9	ns
t_{PLZ}	Disable time from LOW level	Waveform 3, C_L = 5pF		12	ns

AC SETUP REQUIREMENTS T_A = 25°C, V_{CC} = 5.0V

PARAMETER		TEST CONDITIONS	8TS		UNIT
			Min	Max	
$t_W(H)$ $t_W(L)$	Latch Enable pulse width	Waveform 1	6 7.3		ns
t_s	Setup time, Data to Latch Enable	Waveform 5	0		ns
t_h	Hold time, Data to Latch Enable	Waveform 5	10		ns

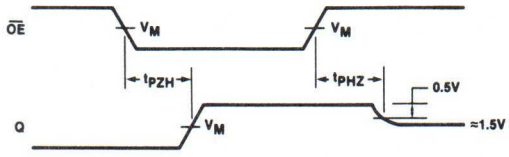
AC WAVEFORMS

LATCH ENABLE TO OUTPUT DELAYS AND LATCH ENABLE PULSE WIDTH



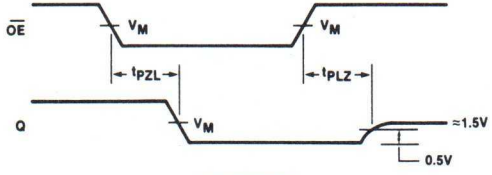
Waveform 1

3-STATE ENABLE TIME TO HIGH LEVEL AND DISABLE TIME FROM HIGH LEVEL



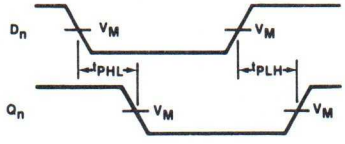
Waveform 2

3-STATE ENABLE TIME TO LOW LEVEL AND DISABLE TIME FROM LOW LEVEL



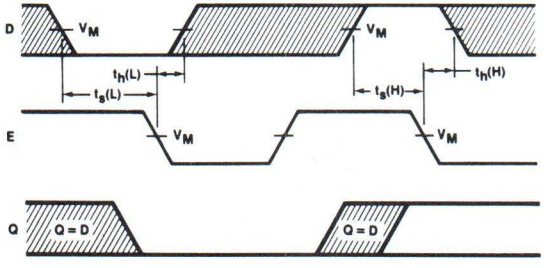
Waveform 3

PROPAGATION DELAY DATA TO Q OUTPUTS



Waveform 4

DATA SETUP AND HOLD TIMES

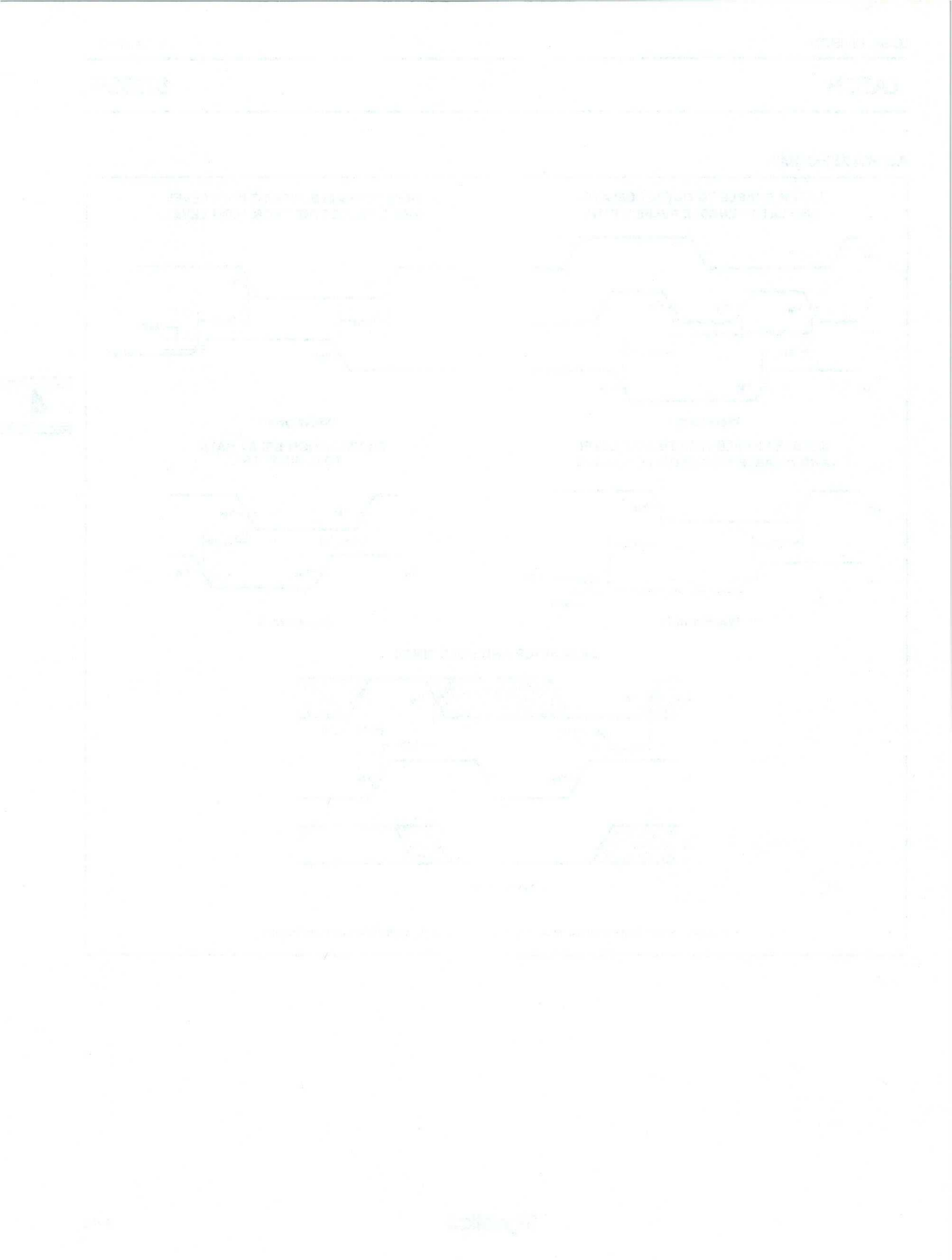


Waveform 5

$V_M = 1.5V$

The shaded areas indicate when the input is permitted to change for predictable output performance.

4



Section 5
54F/74F Fast TTL

THE HIGH-SPEED LOGIC OF THE 80'S

54/74F FAST TTL

PRODUCT DESCRIPTION

Signetics has combined advanced oxide-isolated fabrication techniques with standard TTL functions to create a new family designed for the 80's. The high operating speeds of FAST can push system operating speeds into areas previously reserved for 10K ECL, but with simple TTL design rules and single 5V power supplies. Low input loading allows the user to mix LS, ALS,and HCMOS in the same system without the need for translators and restrictive fanout requirements.

FAST circuits are pin-for-pin replacements for 74S types, but offer power dissipation 3-4 times lower and higher operating speeds. Existing systems can achieve much lower power by replacing the 74S types with the corresponding FAST devices, with no changes other than reducing the size of the power supply.

The input structure provides better noise immunity because of higher thresholds, while the oxide-isolation and new circuit techniques create devices that have less variation with temperature or supply voltage than existing TTL logic families. Signetics guarantees all ac parameters under realistic system conditions—across the supply voltage spread and the temperature range, and with heavy 50pF output loads.

The use of high-capacitance PNP inputs has been avoided, and clamping diodes have been added to both the inputs and outputs to prevent negative overshoots. High input breakdown voltages allow unused inputs to be tied directly to V_{CC} without pullup resistors.

Multiple sources and a complete family of powerful circuits combine to make Signetics FAST the logic choice of the 80's!

FEATURES

- **3ns propagation delays**
- **4mW/gate power dissipation**
- **Guaranteed AC performance over temperature and supply voltage spreads**
- **Improved input and output structures**
- **Standard TTL functions and pinouts**
- **Replacement for "S" types . . . 1/4 the power**
- **Designer's choice for new system designs**

5

THE SPEED/POWER SPECTRUM

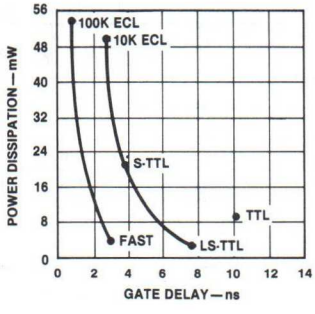


Figure 1

BASIC FAST GATE

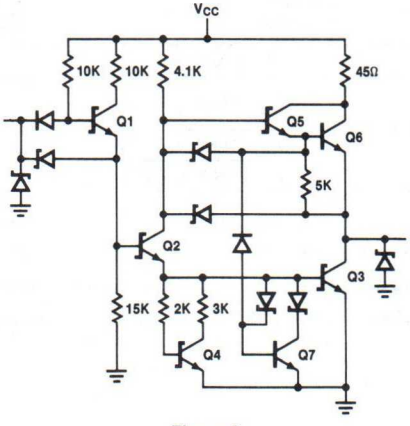


Figure 2

TRANSFER FUNCTIONS AT ROOM TEMPERATURE

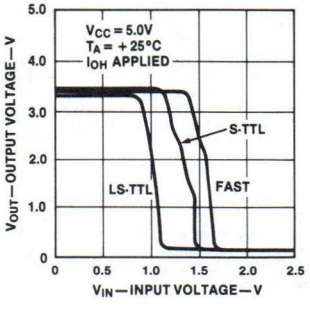


Figure 3

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		54F	74F	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	−30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	−0.5 to +V_{CC}	−0.5 to +V_{CC}	V
T_A	Operating free-air temperature range	−55 to +125	0 to 70	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER			54/74F			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage	Mil	4.5	5.0	5.5	V
		Com'l	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage		2.0			V
V_{IL}	LOW-level input voltage				+0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	HIGH-level output current	Std.			−1.0	mA
		Buffer			−15.0	mA
I_{OL}	LOW-level output current	Std.			20	mA
		Buffer (Com'l)			64	mA
T_A	Operating free-air temperature	Mil	−55		+125	°C
		Com'l	0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER		TEST CONDITIONS[1]		54/74F			UNIT
				Min	Typ[2]	Max	
V_{OH}	HIGH-level output voltage	V_{CC} = MIN, V_{IH} = MIN, V_{IL} = 0.5V, I_{OH} = −15mA	Buffer	2.0			V
		V_{CC} = MIN, V_{IH} = MIN, V_{IL} = MAX	Std — I_{OH} = −1mA	2.7	3.4		V
			Buffer—I_{OH} = −3mA	2.7	3.4		V
V_{OL}	LOW-level output voltage	V_{CC} = Min, V_H = MIN, V_{IL} = MAX, I_{OL} = MAX	Std.		0.35	0.5	V
			Buffer			0.55	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_{IK} = I_{IK}				−1.2	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				0.1	mA
I_{IH}	HIGH-level input current	V_{CC} = MAX, V_I = 2.7V				20	μA
I_{IL}	LOW-level input current	V_{CC} = MAX, V_I = 0.5V				−0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = MAX	Std.	−60		−150	mA
			Buffer	−100		−225	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

FAST ADVANCED SCHOTTKY TTL STATUS GUIDE

Device	Pin #	Description	Availability
54/74F00	14	Quad 2-Input NAND Gate	1982
54/74F02	14	Quad 2-Input NOR Gate	1982
54/74F04	14	Hex Inverter	1982
54/74F08	14	Quad 2-Input AND Gate	1982
54/74F10	14	Triple 3-Input NAND Gate	1982
54/74F11	14	Triple 3-Input AND Gate	1982
54/74F14	14	Hex Inverter Schmitt Trigger	Planned
54/74F20	14	Dual 4-Input NAND Gate	1982
54/74F32	14	Quad 2-Input OR Gate	1982
54/74F37	14	Quad Input NAND Buffer	Planned
54/74F38	14	Quad Input NAND Buffer (Open Collector)	Planned
54/74F40	14	Dual 4-Input NAND Buffer	Planned
54/74F64	14	AND/OR Invert Gate	1982
54/74F74	14	Dual D-Type Flip-Flop	1982
54/74F85	16	4-Bit Magnitude Comparator	Planned
54/74F86	14	Quad 2-Input Exclusive-OR Gate	1982
54/74F109	16	Dual JK Flip-Flop	1982
54/74F112	16	Dual JK Flip-Flop	1982
54/74F113	16	Dual JK Flip-Flop	1982
54/74F114	16	Dual JK Flip-Flop	1982
54/74F138	16	One-of-Eight Decoder/Demultiplexer	1982
54/74F139	16	Dual One-of-Four Decoder/Demultiplexer	1982
54/74F148	16	8-Bit Priority Encoder	1982
54/74F151	16	8-Input Multiplexer	1982
54/74F153	16	Dual 4-Input Multiplexer	1982
54/74F157	16	Quad 2-Input Multiplexer	1982
54/74F158	16	Quad 2-Input Multiplexer	1982
54/74F160	16	BCD Decade Ctr., Asyn. Reset	1982
54/74F161	16	4-Bit Binary Ctr., Asyn. Reset	1982
54/74F162	16	BCD Decade Ctr., Synch. Reset	1982
54/74F163	16	4-Bit Binary Ctr., Synch. Reset	1982
54/74F164	14	8-Bit Serial-In Parallel-Out Shift Register	Planned
54/74F168	16	Up/Down Decade Counter	1982
54/74F169	16	Up/Down Binary Counter	1982
54/74F174	16	Hex D Flip-Flop w/Common Master Reset	1982
54/74F175	16	Quad D Flip-Flop w/Common Master Reset	1982
54/74F181	24	Arithmetic Logic Unit	1982
54/74F182	16	Carry Look-Ahead Generator	1982
54/74F190	16	Up/Down Decade Counter	1982
54/74F191	16	Up/Down Binary Counter	1982
54/74F192	16	Up/Down Decade Counter	1982
54/74F193	16	Up/Down Binary Counter	1982
54/74F194	16	4-Bit Bidirectional Universal Shift Register	1982
54/74F195	16	4-Bit Parallel Access Shift Register	Planned
54/74F240	20	Octal Inv. Bus/Line Driver	1982
54/74F241	20	Octal Bus/Line Driver	1982
54/74F242	14	Quad Bus Transceiver	Planned
54/74F243	14	Quad Bus Transceiver	Planned
54/74F244	20	Octal Bus/Line Driver	1982
54/74F245	20	Octal Bus Transceiver	1982
54/74F251	16	8-Input Multiplexer 3-State	1982
54/74F253	16	Dual 4-Input Multiplexer 3-State	1982
54/74F257	16	Quad 2-Input Multiplexer 3-State	1982
54/74F258	16	Quad 2-Input Multiplexer 3-State	1982
54/74F259	16	8-Bit Addressable Latch	Planned
54/74F269	24	8-Bit Up/Down Counter	Planned
54/74F273	20	Octal D Flip-Flop	Planned
54/74F280	14	9-Bit Parity Generator/Checker	1982

Device	Pin #	Description	Availability
54/74F298	16	Quad 2-Port Register	Planned
54/74F299	20	Octal Shift/Storage Register 3-State	Planned
54/74F322	20	Octal Shift/Storage Register 3-State	Planned
54/74F323	20	Octal Shift/Storage Register 3-State	Planned
54/74F350	16	4-Bit Shifter 3-State	1982
54/74F352	16	Dual 4-Input Multiplexer (Inverted '153)	1982
54/74F353	16	Dual 4-Input Multiplexer (Inverted '253)	1982
54/74F365	16	Hex Buffer/Driver 3-State	Planned
54/74F366	16	Hex Inverter Buffer 3-State	Planned
54/74F367	16	Hex Buffer/Driver 3-State	Planned
54/74F368	16	Hex Inverter Buffer 3-State	Planned
54/74F373	20	Octal D Latch 3-State	1982
54/74F374	20	Octal D Flip-Flop 3-State	1982
54/74F377	20	Octal D Flip-Flop with Clock Enable	Planned
54/74F378	16	Hex D Flip-Flop with Enable	1982
54/74F379	16	Quad D Flip-Flop with Enable	1982
54/74F395	16	4-Bit Cascadable Shift Register 3-State	Planned
54/74F398	20	4-Bit Flip-Flop, True and Comp. Outputs	Planned
54/74F399	16	4-Bit Flip-Flop, True and Comp. Outputs	Planned
54/74F412	24	Multimode Octal Latch	1982
54/74F431	24	8-Bit Output Port	1982
54/74F432	24	Inverting Multimode Octal Latch	1982
54/74F521	20	Octal Comparator	1982
54/74F524	20	8-Bit Registered Comparator	Planned
54/74F533	20	Inverting Octal D Latch, 3-State	1982
54/74F534	20	Inverting Octal D Flip-Flop, 3-State	1982
54/74F545	20	Octal Bus Transceiver	1982
54/74F568	20	4-Bit Binary Up/Down Counter, 3-State	1982
54/74F569	20	4-Bit Decade Up/Down Counter, 3-State	1982
54/74F579	20	8-Bit Up/Down Counter, Common I/O	Planned
54/74F588	20	GPIB Compatible Octal Transceiver	1982
54/74F595	16	8-Bit Shift Register w/Output Latch	Planned
54/74F596	16	8-Bit Shift Register w/Output Latch	Planned
54/74F597	16	8-Bit Shift Register w/Input Latch	Planned
54/74F598	16	8-Bit Shift Register w/Input Latch	Planned
54/74F604	28	Dual 8-Bit Latch	1982
54/74F605	28	Dual 8-Bit Latch	1982
54/74F606	28	Dual 8-Bit Latch	1982
54/74F607	28	Dual 8-Bit Latch	1982
54/74F620	20	Octal Inverting Transceiver 3-State	Planned
54/74F621	20	Octal Transceiver Open-Collector	Planned
54/74F622	20	Octal Inverting Transceiver Open-Collector	Planned
54/74F623	20	Octal Transceiver 3-State	Planned
54/74F630	28	Memory Error Detector/Corrector, 3-State	Planned
54/74F631	28	Memory Error Detector/Corrector, Open Collector	Planned
54/74F646	24	Registered Octal Bus Transceiver 3-State	Planned
54/74F647	24	Registered Octal Bus Transceiver Open-Collector	Planned
54/74F648	24	Inverting Registered Octal Bus Transceiver 3-State	Planned
54/74F649	24	Inverting Registered Octal Bus Transceiver Open-Collector	Planned
54/74F673	24	16-Bit Serial-In/Parallel-Out Shift Register	Planned
54/74F674	24	16-Bit Parallel-In/Serial-Out Shift Register	Planned
54/74F675	24	16-Bit SI/PO Shift Register w/S.O. Capability	Planned
54/74F676	24	16-Bit PI/SO Shift Register w/S.O. Capability	Planned
54/74F779	16	8-Bit Bidirectional Binary Counter	Planned

5

PROPAGATION DELAY VS LOAD CAPACITANCE
'F00

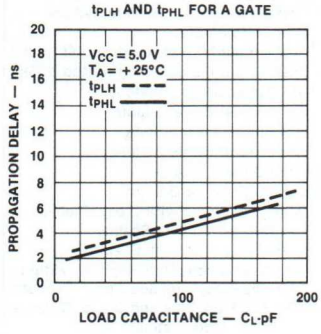


Figure 4

OUTPUT LOW CHARACTERISTICS
'F00

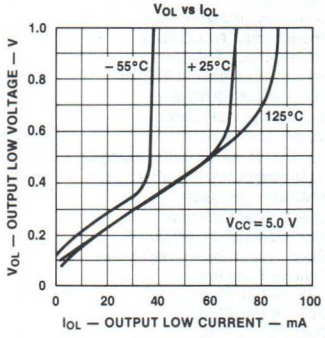


Figure 5

FALL TIME VS LOAD CAPACITANCE
'F00

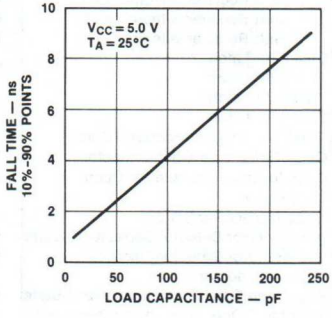


Figure 6

OUTPUT HIGH CHARACTERISTICS
'F00

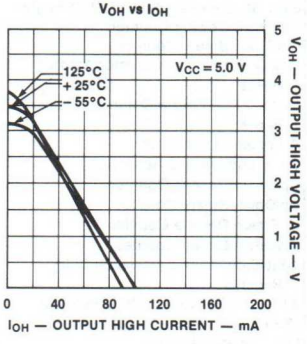


Figure 7

Section 6
Military Products

MILITARY PRODUCTS

INTRODUCTION

Manufacturing integrated circuits to the stringent requirements of the Defense and Aerospace industries has been a dedication of Signetics since its founding in 1961. Today, Signetics remains unchanged in charter and continues to produce integrated circuits for this market segment with state-of-the-art process technologies which result in unequalled overall reliability.

Signetics' dedicated approach to the military market is evidenced by the fact that in 1981 the division was moved into a brand-new building in Sacramento. The Military Products Division has its own production facilities, engineering staff and marketing organization. Rather than dealing with each individual product division, as they must at many companies, Signetics' military customers can deal with the company's broad product capability as well as with the special requirements of the military market.

Assessing the individual products of any high-reliability supplier is enhanced by a complete understanding of the company's technological processes and the degree of its commitment to quality control and reliabilty.

Table 1 MILITARY PACKAGE AVAILABILITY

JAN CASE OUTLINE AND LEAD FINISH	SIGNETICS MILITARY PACKAGE TYPES						
	CAN		DUAL-IN-LINE				
	8-PIN	10-PIN	8-PIN	14-PIN	16-PIN	18-PIN	24-PIN
PB	—	—	FE	—	—	—	—
CB	—	—	—	F	—	—	—
EB	—	—	—	—	F	—	—
JB	—	—	—	—	—	—	F
DB	—	—	—	W	—	—	—
FB	—	—	—	—	W	—	—
ZC	—	—	—	—	—	—	Q
GC	H	—	—	—	—	—	—
IC	—	H	—	—	—	—	—
VB	—	—	—	—	—	I	—

All products listed are also available in Die form.

Table 2 MILITARY SUMMARY

	JS/JB	RB	RC
	JAN QUALIFIED	883B	883C
54	X	X	X
54LS	X	X	X
54S	X	X	X
82	X	X	X
8T	—	X	X
93XX	X	X	X
96XX	—	X	X
Analog	X	X	X
Bipolar Memory	X	X	X
Microprocessor	—	X	X

MILITARY PRODUCTS/PROCESS LEVELS

The Signetics Military 38510/883 Program is organized to provide a broad selection of processing options, structured around the most commonly requested customer flows. The program is designed to provide our customers:

- Fully compliant 883 flows on all products.
- Standard processing flows to help minimize the need for custom specs.
- Cost savings realized by using standard processing flows in lieu of custom flows.
- Better delivery lead times by minimizing spec negotiation time, plus allows customer to buy product off-the-shelf or in various stages of production rather than waiting for devices started specifically to custom specs.

The following explains the different processing options available to you. Special device marking clearly distinguishes the type of screening performed. Refer to Tables 2, 3, 4 and 5.

JAN QUALIFIED

JAN Qualified product is designed to give you the optimum in quality and reliability. The JAN processing level is offered as the result of the government's product standardization programs, and is monitored by the Defense Electronic Supply Center (DESC), through the use of industry-wide procedures and specifications.

JAN Qualified products are manufactured, processed and tested in a government certified facility to Mil-M-35810, and appropriate device slash sheet specifications. Design documentation, lot sampling plans, electrical test data and qualification data for each specific part type has been approved by DESC and products appear on the DESC Qualified Products List (QPL-38510).

Group B testing, per Mil-Std-883, Method 5005, is performed each week of production for each package type. Group C, per Mil-Std-883, Method 5005 is performed every ninety days for each microcircuit group. Group D testing, per Mil-Std-883, Method 5005, is performed every six months for each package type.

In addition to the common specs used throughout the industry for processing and testing, JAN Qualified products also possess a requirement for a standard marking used throughout the IC industry.

For JAN Qualified Class S type products, refer to Signetics JAN Class S Bulletin.

MIL-STD-883, LEVEL B

Processing to this option is ideal when no JAN slash sheets are released on devices required. Product is processed to Mil-Std-883, Method 5004, and is 100% electrically tested to industry data sheets. Devices are selectively available as custom processed parts with electricals screened to the JAN Slash Sheets.

MIL-STD-883, LEVEL C

If you need a Military temp. range device, but do not require burn in screening performed, our 883C product is ideal. 883C parts are the standard full Mil-Temperature range product to the Signetics data sheet parameters and screened to MIL-STD-883, Class C.

MILITARY PRODUCTS

MILITARY GENERIC DATA

Signetics maintains a program for those customers who require quality conformance data on their products. This program allows our customers to obtain reliability information without the necessity of running Groups B, C and D inspections for their particular purchase order. It provides for the customer something that has not been readily available before in the semiconductor industry in that all Military Generic Data is controlled and audited by both Government Inspection in the case of JAN data and Signetics Quality Assurance.

Signetics Military Generic Data is compiled by the Military Products Division based on data from 1) JAN quality conformance lots, and 2) Data generated by quality conformance lots run for other reliability programs. Refer to Table 4.

A Military Generic family is defined as consisting of die function and package type families.

Military Generic Data

- Allows our customers to qualify Signetics products based on existing quality conformance data performed at Signetics.
- Allows our customers to reduce costs and improve deliveries.
- Provides assurance that all Signetics die function families and packages meet Mil-M-38510 and customer reliability requirements.
- Provides an attributes summary to the customer backed by lot identity and traceability.

Table 3 MILITARY PRODUCTS PROCESSING MATRIX

PROCESS LEVEL AND MARKETING	PRE-CAP VISUAL	BURN IN	FUNCTIONAL TEST	DC/AC @25°C	DC/AC @TEMP	QPL	OFFSHORE
JS JS38510/XXX	2010, Cond. A + Nondestructive Bondpull	Yes	100%	100%	100%	Yes	No
JB JM38510/XXXX	2010, Cond. B	Yes	100%	100%	100% DC Sample AC	Yes	No
RB SXXXX883B	2010, Cond. B	Yes	100%	100%	100% DC only	No	Yes
RC SXXXX883C	2010, Cond. B	No	100%	100% DC Sample AC	Sample DC only	No	Yes

Table 4 DEFINITION AND QUALIFYING MANUFACTURING PERIODS FOR GENERIC DATA

QUALIFIED SUB-GROUPS	QUALIFIES	OPTION 1	OPTION 2
A*	Electrical Test		
B	Package—Same package construction and lead finish.	Data selected from devices manufactured within the manufacturing week on the same production line through final seal.	Data selected from devices manufactured within 26 weeks of manufacturing period.
C	Die/Process—Devices representing the same process families.	Data selected from representative devices from the same microcircuit group and sealed within 12 weeks of the manufacturing period.	Data selected from the representative devices from the same microcircuit group and sealed within 52 weeks of the manufacturing period.
D	Package—Same package construction and lead finish.	Data selected from the devices representing the same package construction and lead finish manufactured within the 26 weeks of manufacturing period. If specific data not available, Option 2 will be supplied.	Data selected from the devices representing the same package construction and lead finish manufactured within the 52 weeks of manufacturing period.

NOTE*
Group A is performed on each lot or sublot of Signetics devices.

MILITARY PRODUCTS

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			JAN QUALIFIED S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
General Mil-M-38510 1. Pre-Certification A. Product Assurance Program Plan B. Manufacturer's Certification	The Manufacturer shall establish and implement a Products Assurance Program Plan and provide for a manufacturer survey by the qualifying activity, Para. 3.4.1.1	—	X	X	N/A	N/A
2. Certification	Received after manufacturer has completed a successful survey, Para. 3.4.1.2	—	X	X	N/A	N/A
3. Device Qualification	Device qualification shall consist of subjecting the desired device to groups A, B, C & D of Method 5005 to tightened LTPD, Para. 3.4.1.2	—	X	X	N/A	N/A
4. Traceability	Traceability maintained back to a production lot, Para. 3.4.6	—	X	X	X	X
5. Country of Origin	Devices must be manufactured, assembled, and tested within the U.S. or its territories, Para. 3.2.1	—	X	X	N/A	N/A
Screening Per Method 5004 of Mil-Std-883						
6. Internal Visual (Precap)	2010, Cond. A or B	100%	XA	XB	XB	XB
7. Stabilization Bake	1008, Cond. C Min; (24 Hrs @ 150°C min.)	100%	X	X	X	X
8. Temperature Cycling	1010, Cond. C; (10 cycles, −65°C to +150°C)	100%	X	X	X	X
9. Constant Acceleration	2001, Cond. E; (30kg) in YI Plane	100%	X	X	X	X
10. Visual Inspection	There is no test method for this screen; it is intended only for the removal of "Catastrophic Failures" defined as "Missing Leads, Broken Packages or Lids Off."	100%	X	X	X	X
11. Seal (Hermeticity)	1014					
A. Fine	Cond. A or B (5.0×10^{-8} CC/Sec)	100%	X	X	X	X
B. Gross	Cond. C2	100%	X	X	X	X
12. Interim Electricals (Pre Burn-In)	Per applicable device specification	100%	100% Read & Record	Slash Sheet Optional	Data Sheet Optional	N/A
13. Burn-In	1015, Cond. as specified (160 hrs. Min. at 125°C)	100%	100% 240 hrs.	X	X	N/A
14. Final Electricals	Per applicable Device Specification	100%	100% Read & Record	Slash Sheet	Data Sheet	Data Sheet
A. Static Tests @ 25°C	Sub Group 1	100%	X	X	X	X
B. Static Tests @ +125°C	Sub Group 2	100%	X	X	X	N/A
C. Static Tests @ −55°C	Sub Group 3	100%	X	X	X	N/A
D. Dynamic Test @ 25°C	Sub Group 4 (for Linear Product Mainly)	100%	X	X	X	X
E. Functional Test @ 25°C	Sub Group 7	100%	X	X	X	X
F. Switching Test @ 25°C	Sub Group 9	100%	X	X	X	N/A

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MILITARY PRODUCTS

Table 5 REQUIREMENTS AND SCREENING FLOWS FOR STANDARD PRODUCTS (Continued)

DESCRIPTION OF REQUIREMENTS AND SCREENS	MIL-M-38510 AND MIL-STD-883 REQUIREMENTS, METHODS AND TEST CONDITIONS	REQUIREMENT	PROCESSING LEVELS			
			JAN QUALIFIED S	JAN QUALIFIED (JB)	883B (RB)	883C (RC)
15. Percent Defective Allowable (PDA)	A PDA of 10% is a normal requirement applied against the static tests @ 25°C (A-1). This is controlled by the slash sheets for JB products. For RB 10% is standard.	10%	5% 3% Funct'l	X	X	N/A
16. Marking	Fungus Inhibiting Paint	100%	JM38510/ XXX Slash Sheet #	JM38510/ XXXX Slash Sheet #	SXXXX 883B	SXXXX 883C
17. X-Ray	2012, 2 views	100%		N/A	N/A	N/A
18. External Visual	2009	100%	X	X	X	X
Quality Conformance Inspection Per Method 5005 of Mil-Std-883						
19. Group A	Electrical Tests—Final Electricals (#14 above) repeated on a sample basis. (Sub Groups 1 thru 12 as specified.)	Each sublot	X	X	X	X
20. Group B	Package functional and constructional related test I.E. package dimensions, resistance to solvents, internal visual & mechanical, bond strength & solderability.	Every week per package group	Each lot	X	Generic Data Available	Generic Data Available
21. Group C	Die related tests I.E. 1,000 hr. operating life, temperature cycling, & constant acceleration.	Every 3 months per μcircuit group	N/A	X	Generic Data Available	Generic Data Available
22. Group D	Package related tests I.E. physical dimensions, lead fatigue, thermal shock, temperature cycle, moisture resistance, mechanical shock, vibration variable frequency constant acceleration, & salt atmosphere.	Every 6 months per package type	X	X	Generic Data Available	Generic Data Available

MILITARY PRODUCTS

ORDERING INFORMATION

The Signetics Military Products are available in a variety of different process levels and several different packages. The correct ordering code or part number for the devices is an alphanumeric sequence as explained below. Not all devices are available in all the packages. The ordering codes on the individual data sheets indicate the present or planned availability of the products. However, availability of specific part numbers can be obtained from your local sales office or franchised distributor.

Ordering Code

1) JM38510/07801BJB
- LEAD FINISH
- PACKAGE TYPE
- CLASS "B"
- SLASH SHEET NUMBER (BASIC DEVICE TYPE)
- JAN QUALIFIED

2) JB54S181F
- PACKAGE TYPE
- BASIC DEVICE TYPE
- CLASS "B"
- JAN QUALIFIED

3) S54S181F883B
- LEVEL "B"
- MIL-STD-883
- PACKAGE TYPE
- BASIC DEVICE TYPE
- MILITARY TEMPERATURE RANGE (– 55 TO 125°C)

4) RB54S181F
- PACKAGE TYPE
- BASIC DEVICE TYPE
- MIL-STD-883, LEVEL "B"

NOTE:
1) and 2) JAN qualified products.
3) and 4) Non-JAN MIL-STD-883 products.

For minimum quantity orders, contact your local Signetics sales representative.

PACKAGES AVAILABLE*

F = Ceramic DIP
I = Ceramic DIP
G = Ceramic Leadless Chip Carrier**
Q = Ceramic Flatpack
W = Ceramic Flatpack
H = Metal Can

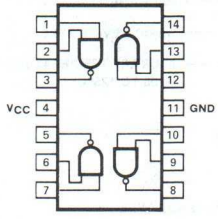
*See Section 7 for more package information.
**1982.

MILITARY PRODUCTS

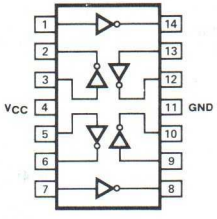
FLATPACK CONFIGURATIONS

Generally the flatpack pin configurations are *identical* to the appropriate dual-in-line packages. The only *exceptions* are illustrated in the following configurations:

S5400W ONLY



S5404W ONLY



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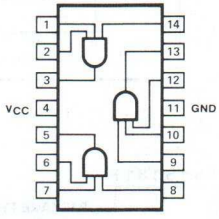

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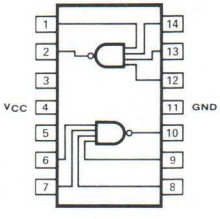

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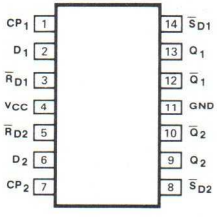

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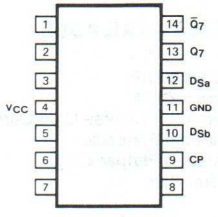

MILITARY PRODUCT GUIDE

LOGIC—5400 SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
5400	Quad 2-Input NAND Gate	/00104	1	1	F	W
5403	Quad 2-Input NAND Gate with o/c	/00109	—	—	F	—
5404	Hex Inverter	/00105	1	1	F	W
5411	Triple 3-Input AND Gate	—	—	—	F	W
5414	Hex Schmitt Trigger	/15102	—	—	F	W
5420	Dual 4-Input NAND Gate	/00102	1	1	F	W
5426	Quad 2-Input NAND Gate with o/c	/00805	1	—	F	—
5432	Quad 2-Input OR Gate	/16101	1	1	F	W
5442	BCD-to-Decimal Decoder	/01001	1	1	F	W
5443	Excess 3-to-Decimal Decoder	/01002	—	—	F	W
5446A	BCD-to-7 Segment Decoder/Driver	/01006	—	—	F	W
5447A	BCD-to-7 Segment Decoder/Driver	/01007	—	—	F	W
5473	Dual J-K Master-Slave Flip-Flop	/00202	1	1	F	W
5470	Dual D-Type Edge-Triggered Flip-Flop	/00205	—	—	F	W
5475	Quad Bistable Latch	/01501	1	1	F	W
5476	Dual J-K Master-Slave Flip-Flop	/00204	1	1	F	W
5477	Quad Bistable Latch	/01502	—	—	—	W
5483	4-Bit Binary Full Adder	/00602	—	—	F	W
5485	4-Bit Magnitude Comparator	/15001	1	1	F	W
5486	Quad 2-Input Exclusive-OR Gate	/00701	1	1	F	W
5491	8-Bit Shift Register	—	—	—	F	W
5493	4-Bit Binary Counter	/01302	1	1	F	W
5494	4-Bit Shift Register {PISO}	—	—	—	F	W
5496	5-Bit Shift Register	/00902	1	1	F	W
54109	Dual J-K Positive Edge-Triggered Flip-Flop	—	—	—	F	W
54116	Dual 4-Bit Latch with Clear	/01503	1	—	F	W
54121	Monostable Multivibrator	/01201	1	1	F	W
54122	Retriggerable Monostable Multivibrator	/01202	—	—	—	—
54123	Retriggerable Monostable Multivibrator	/01203	1	1	F	W
54132	Quad Schmitt Trigger	/15103	1	1	F	W
54148	8-Line to 3-Line Priority Encoder	/15602	—	—	F	W
54151	8-Line to 1-Line Mux	/01406	1	1	F	W
54153	Dual 4-Line to 1-Line Mux	/01403	1	1	F	W
54154	4-Line to 16-Line Decoder/Demux	/15201	1	—	F	W
54160	Synchronous 4-Bit Decade Counter	/01303	1	1	F	W
54161	Synchronous 4-Bit Binary Counter	/01306	1	1	F	W
54163	Synchronous 4-Bit Binary Counter	/01304	1	1	F	W
54164	8-Bit Parallel-Out Serial Shift Register	/00903	1	—	F	—
54165	Parallel-Load 8-Bit Shift Register	/00904	*	*	F	W
54174	Hex D-Type Flip-Flop with Clear	/01701	1	1	F	W
54175	Quad D-Type Edge-Triggered Flip-Flop	/01702	1	1	F	W
54180	8-Bit Odd/Even Parity Checker	/01901	1	1	F	W
54181	4-Bit Arithmetic Logic Unit	/01101	1	—	F	—
54190	Synchronous Up/Down Counter (BCD)	—	—	—	*	*
54191	Synchronous Up/Down Counter (Binary)	—	—	—	*	*
54193	Synchronous 4-Bit Binary Up/Down Counter	/01309	1	1	F	W
54194	4-Bit Bidirectional Universal Shift Register	/00905	1	1	F	W
54279	Quad S-R Latch	—	—	—	F	W
54365A	Hex Buffer w/Common Enable (3-State)	/16301	1	—	F	R
54366A	Hex Buffer w/Common Enable (3-State)	/16302	1	—	F	R
54367A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16303	1	—	F	R
54368A	Hex Buffer, 4-Bit and 2-Bit (3-State)	/16304	1	—	F	R
9309	Dual 4-Input Multiplexer	/01404	1	1	F	W

NOTE
1 = QPLI 2 = QPLII * = In process

MILITARY PRODUCT GUIDE

LOGIC—54LS SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS00	Quad 2-Input NAND Gate	/30001	1	1	F	W
54LS02	Quad 2-Input NOR Gate	/30301	1	1	F	W
54LS04	Hex Inverter	/30003	1	1	F	W
54LS08	Quad 2-Input AND Gate	/31004	1	1	F	W
54LS10	Triple 3-Input NAND Gate	/30005	1	1	F	W
54LS14	Hex Schmitt Trigger	/31302	1	1	F	W
54LS20	Dual 4-Input NAND Gate	/30007	1	1	F	W
54LS28	Quad 2-Input NOR Buffer	/30204	—	—	F	W
54LS30	8-Input NAND Gate	/30009	—	—	F	W
54LS32	Quad 2-Input OR Gate	/30501	1	1	F	W
54LS37	Quad 2-Input NAND Buffer	/30202	1	1	F	W
54LS42	BCD-to-Decimal Decoder	/30703	1	1	F	W
54LS51	Dual 2-Wide 2-Input A01 Gate	/30401	—	—	F	W
54LS73	Dual J-K Master-Slave Flip-Flop	/30101	2	2	F	W
54LS74	Dual D-Type Edge-Triggered Flip-Flop	/30102	1	1	F	W
54LS75	Quad Bistable Latch	31601	2	2	F	W
54LS76	Dual J-K Master-Slave Flip-Flop	30110	1	1	F	W
54LS83A	4-Bit Binary Full Adder	/31201	—	—	F	W
54LS85	4-Bit Magnitude Comparator Gate	/31101	1	1	F	W
54LS86	Quad 2-Input Exclusive-OR Gate	/30502	1	1	F	W
54LS90	Decade Counter	/31501	1	1	F	W
54LS92	Divide-by-Twelve Counter	/31510	1	1	F	W
54LS93	4-Bit Binary Counter	/31502	1	1	F	W
54LS95	4-Bit Left-Right Shift Register	/30603	1	1	F	W
54LS96	5-Bit Shift Register	/30604	1	1	F	W
54LS107	Dual J-K Master-Slave Flip-Flop	/30108	1	1	F	W
54LS109	Dual J-K Positive Edge-Triggered Flip-Flop	/30109	1	1	F	W
54LS112	Dual J-K Negative Edge-Triggered Flip-Flop	/30103	1	1	F	W
54LS113	Dual J-K Negative Edge-Triggered Flip-Flop	/30104	1	1	F	W
54LS125	Quad Bus Buffer Gate w/3-State Outputs	/32301	1	1	F	W
54LS126	Quad Bus Buffer Gate w/3-State Outputs	/32302	1	1	F	W
54LS13	Quad Schmitt Trigger	/31303	—	—	F	W
54LS136	Quad Exclusive-or with o/c	—	—	—	F	W
54LS138	3-to-8 Line Decoder/Demux	/30701	1	1	F	W
54LS139	Dual 2-to-4 Line Decoder/Demux	/30702	—	—	F	W
54LS151	8-Line to 1-Line Mux	/30901	—	—	*	*
54LS153	Dual 4-Line to 1-Line Mux	/30902	1	1	F	W
54LS154	4-Line to 16-Line Decoder/Demux	—	—	—	1	Q
54LS156	Dual 2-Line to 4-Line Decode/Demux	/32602	2	2	F	W
54LS157	Quad 2-Input Data Selector (non-inv.)	/30903	—	—	F	W
54LS158	Quad 2-Input Data Selector (inv.)	/30904	—	—	F	W
54LS160A	Synchronous 4-Bit Decade Counter	/31503	*	*	F	W
54LS161A	Synchronous 4-Bit Binary Counter	/31504	*	*	F	W
54LS162	Synchronous 4-Bit Decade Counter	/31511	—	—	F	W
54LS163	Synchronous 4-Bit Binary Counter	/31512	1	1	F	W
54LS164	8-Bit Parallel-Out Serial Shift Register	/30605	1	1	F	W
54LS173	Quad D-Type Flip-Flop (3-State) (8T10)	—	—	—	F	W
54LS174	Hex D-Type Flip-Flop with Clear	/30106	1	1	F	W
54LS175	Quad D-Type Edge-Triggered Flip-Flop	/30107	1	1	F	W
54LS181	4-Bit Arithmetic Logic Unit	/30801	1	—	F	W
54LS190	Synchronous Up/Down Counter (BCD)	/31513	1	1	F	W
54LS191	Synchronous Up/Down Counter (Binary)	/31509	1	1	F	W

NOTE
1 = Level 1 Qualification 2 = Level 2 Qualification * = In process

MILITARY PRODUCT GUIDE

LOGIC—54LS SERIES (Cont'd)

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54LS192	Synchronous Decade Up/Down Counter	/31507	•	•	F	W
54LS193	Synchronous 4-Bit Binary Up/Down Counter	/31508	1	1	F	W
54LS194A	4-Bit Bidirectional Universal Shift Register	/30601	—	—	F	W
54LS195A	4-Bit Parallel-Access Shift Register	/30602	1	1	F	W
54LS197	Presettable Binary Counter/Latch (8291)	/32002	•	•	F	W
54LS221	Dual Monostable Multivibrator	/31402	—	—	•	•
54LS240	Octal Inverter Buffer 3-State	/32401	•	—	F	—
54LS241	Octal Buffer 3-State	/32402	•	—	F	—
54LS242	Quad Inverting TCRS. 3-State	/32801	•	•	F	W
54LS243	Quad TCRS. 3-State	/32802	•	•	F	W
54LS244	Octal Buffer 3-State	/32403	•	—	F	—
54LS245	Octal TCRS. 3-State	/32803	•	—	F	—
54LS251	Data Selector/Mux with 3-State Outputs	/30905	—	—	•	•
54LS253	Dual 4-Line to 1-Line Data Selector/Mux	/30908	—	—	F	W
54LS257A	Quad 2-Line to 1-Line Data Selector/Mux	/30906	1	1	•	•
54LS258A	Quad 2-Line to 1-Line Data Selector/Mux	/30907	1	1	•	•
54LS260	Dual 5-Input NOR Gate	—	—	—	F	W
54LS261	2X4 Parallel Binary Multiplier	/31801	—	—	F	W
54LS266	Quad Exclusive-NOR Gate	/30303	1	1	F	W
54LS273	Octal D. Flip Flop	/32501	2	•	F	W
54LS279	Quad S-R Latch	/31602	•	•	F	W
54LS283	4-Bit Adder	/31202	—	—	F	W
54LS290	Decade Counter	/32003	1	1	F	W
54LS293	4-Bit Binary Counter	/32004	1	1	F	W
54LS295B	4-Bit Right-Shift Left-Shift Register	/30606	1	1	F	W
54LS298	Quad 2-Input Mux with Storage	—	—	—	F	W
54LS365	Hex Buffer w/common Enable (3-State)	/32201	1	1	F	W
54LS366	Hex Buffer w/Common Enable (3-State)	/32202	—	—	F	W
54LS367	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32203	1	1	F	W
54LS368	Hex Buffer, 4-Bit and 2-Bit (3-State)	/32204	1	1	F	W
54LS373	Octal Transparent Latch (3-State)	/32502	•	—	F	—
54LS374	Octal D Flip Flop (3-State)	/32503	—	—	F	—
54LS375	Quad Latch	—	—	—	F	W
54LS377	Octal D Flip Flop Clock Enable	/32504	—	—	F	—
54LS395A	4-Bit Cascadeable Shift Register (3-State)	/30607	1	1	F	W
54LS670	4X4 Register File (3-State)	/31901	—	—	F	W

NOTE
1=Level 1 Qualification
2=Level 2 Qualification
•=in Process

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MILITARY PRODUCT GUIDE

LOGIC—54S SERIES

DEVICE	DESCRIPTION	JM38510 SLASH SHEET	JAN QUALIFIED		MIL-STD 883	
			DIP	FLAT-PACK	DIP	FLAT-PACK
54S00	Quad 2-Input NAND Gate	/07001	1	1	F	W
54S02	Quad 2-Input NOR Gate	/07301	1	1	F	W
54S04	Hex Inverter	/07003	1	1	F	W
54S08	Quad 2-Input AND Gate	/08003	1	1	F	W
54S10	Triple 3-Input NAND Gate	/07005	1	1	F	W
54S11	Triple 3-Input NAND Gate	/08001	1	1	F	W
54S20	Dual 4-Input NAND Gate	/07006	—	—	F	W
54S30	8-Input NAND Gate	/07008	—	—	—	—
54S40	Dual 4-Input NAND Buffer	/07201	1	1	F	W
54S51	Dual 2-Wide 2-Input A01 Gate	/07401	1	1	F	W
54S74	Dual D-Type Edge-Triggered Flip-Flop	/07101	1	1	F	W
54S85	4-Bit Magnitude Comparator	/08201	1	—	F	—
54S86	Quad 2-Input Exclusive-OR Gate	/07501	1	1	F	W
54S112	Dual J-K Negative Edge-Triggered Flip-Flop	/07102	1	1	F	W
54S113	Dual J-K Negative Edge-Triggered Flip-Flop	/07103	2	2	F	W
54S133	13-Input NAND Gate	/07009	1	1	F	W
54S135	Quad Exclusive-OR/NOR Gate	/07502	—	—	—	—
54S138	3-to-8 Line Decoder/Demux	/07701	—	—	—	—
54S139	Dual 2-to-4 Line Decoder/Demux	/07702	—	—	F	W
54S140	Dual 4-Input NAND Line Driver	/08101	1	1	F	W
54S151	8-Line to 1-Line Mux	/07901	1	1	F	W
54S153	Dual 4-Line to 1-Line Mux	/07902	1	1	F	W
54S157	Quad 2-Input Data Selector (non.inv.)	/07903	1	1	F	W
54S158	Quad 2-Input Data Selector (inv)	/07904	1	1	F	W
54S174	Hex D-Type Flip-Flop with Clear	/07105	—	—	F	W
54S175	Quad D-Type Edge-Triggered Flip-Flop	/07106	—	—	—	—
54S181	4-Bit Arthmetic Logic unit	/07801	1	—	F	*
54S182	Look-Ahead Carry Generator	/07802	—	—	*	*
54S194	4-Bit Bidirectional Universal Shift Register	/07601	—	—	—	—
54S195	4-Bit Parallel-Access Shift Register	/07602	—	—	—	—
54S251	Data Selector/Mux with 3-State Outputs	/07905	—	—	—	—
54S253	Dual 4-Line to 1-Line Data Selector/Mux	—	—	—	F	W
54S257	Quad 2-Line to 1-Line Data Selector/Mux	/07906	—	—	—	—
54S258	Quad 2-Line to 1-Line Data Selector/Mux	/07907	—	—	—	—
54S26C	Dual 5-Input NOR Gate	—	—	—	F	W
54S280	9-Bit Odd/Even Parity Generator/Checker	/07703	—	—	—	—

NOTE

Per QPL 38510-32 dated
10 January 1978
1=Level 1 Qualification
2=Level 2 Qualification
*=In Process

MILITARY PRODUCT GUIDE

LOGIC—8T INTERFACE SERIES

DEVICE	DESCRIPTION	JAN M38510 SHEET	MIL-STD 883	
			DIP	FLAT-PACK
8T05	7-Segment Decoder Display Driver (Active-Hi Outputs)	—	F	W
8T09	Quad Bus Driver with 3-State Outputs	—	F	W
8T13	Dual Line Driver	—	F	W
8T18	Dual 2-Input NAND (High Voltage to TTL Interface)	—	F	W
8T22	Retriggerable Monostable Multivibrator (54122/9601)	—	F	W
8T26A	Quad Bus Driver/Receiver (3-State Outputs)	—	F	R
8T28	Quad Non-Inverting Bus Driver/Receiver (3-State Outputs)	—	F	W
8T31	8-Bit Bidirectional I/O Port	—	*	*
8T32	Programmable 8-Bit, I/O Port (3-State), IV Byte	—	I	*
8T33	Programmable 8-Bit, I/O Port (Open Collector), IV Byte	—	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)		I	W
8T37	Hex Bus Receiver with Hysteresis-Schmitt Trigger		F	W
8T38	Quad Bus Transceiver (Open Collector) (DM8838)		F	W
8T80	Quad 2-Input NAND Gate (High Voltage)		F	W
8T90	Hex Inverter (High Voltage)	—	F	W
8T95	High Speed Hex Buffers/Inverters (74365/DM8095)	—	F	R
8T97	High Speed Hex Buffers/Inverters (74367/DM8097)		F	R
8T98	High Speed Hex Buffers/Inverters (74368/DM8098)		F	R
8T126	Quad 3-State Transceivers	—	F	W
8T127	Quad 3-State Transceivers	—	F	W
8T128	Quad 3-State Transceivers	—	F	W
8T129	Quad 3-State Transceivers	—	F	W

* = Qualification planned

MILITARY PRODUCT GUIDE

MICROPROCESSOR SUPPORT CIRCUITS

PRODUCT	DESCRIPTION	AVAILABILITY	
		DIP	FLAT PACK
LOGIC			
54123	Retriggerable Monostable Multivibrator	F	R
54180	8-Bit Odd/Even Parity Checker	F	R
54LS194	4-Bit Bidirectional Shift Register	I	*
54LS195	4-Bit Parallel Access Shift Register	I	*
54LS365	High Speed Hex 3-State Buffer	F	W
54LS366	High Speed Hex 3-State Buffer	F	W
54LS367	High Speed Hex 3-State Buffer	F	W
54LS368	High Speed Hex 3-State Buffer	F	W
	INTERFACE		
8T09	Quad Bus Driver with 3-State Output	F	W
8T13	Dual Line Driver	F	W
8T26A	Quad Bus Driver/Receiver (3-State)	F	W
8T28	Quad Bus Non-Inverting Driver/Receiver (3-State)	F	W
8T32	Programmable 8-Bit I/O Port (3-State), IV Byte	I	*
8T35	Asynchronous Programmable 8-Bit I/O Port (Open Collector)	I	*
8T95	High Speed Hex Buffer (3-State)	F	R
8T97	High Speed Hex Buffer (3-State)	F	R
8T98	High Speed Hex Inverter (3-State)	F	R
8T126	Quad 3-State Transceivers	F	W
8T127	Quad 3-State Transceivers	F	W
8T128	Quad 3-State Transceivers	F	W
8T129	Quad 3-State Transceivers	F	W

* Under development

Section 7
Package Outlines

Section 7
Packaging Outlines

PACKAGE OUTLINES

INTRODUCTION

The following information applies to all packages unless otherwise specified on individual package outline drawings.

General

1. Dimensions shown are metric units (millimeters), except those in parentheses which are English units (inches).
2. Lead spacing shall be measured within this zone.
   a. Shoulder and lead tip dimensions are to centerline of leads.
3. Tolerances non-cumulative.
4. Thermal resistance values are determined by utilizing the linear temperature dependence of the forward voltage drop across the substrate diode in a digital device to monitor the junction temperature rise during known power applications across V_{CC} and ground. The values are based upon 120 mils square die for plastic packages and a 90 mils square die in the smallest available cavity for hermetic packages. All units were solder mounted to P.C. boards, with standard stand-off, for measurement.

Plastic Only

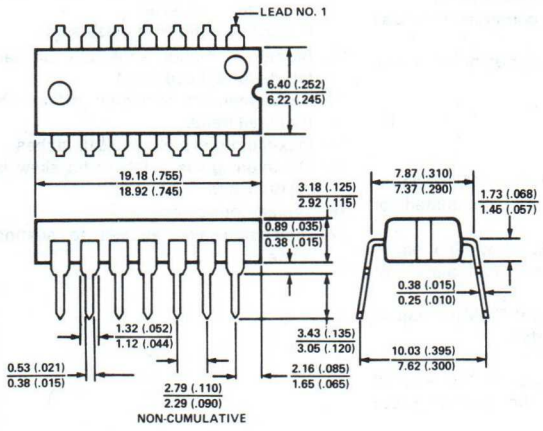
5. Lead material: Alloy 42 (Nickel/Iron Alloy) Olin 194 (Copper Alloy) or equivalents, solder dipped.
6. Body material: Plastic (Epoxy)
7. Round hole in top corner denotes lead No. 1.
8. Body dimensions do not include molding flash.

Hermetic Only

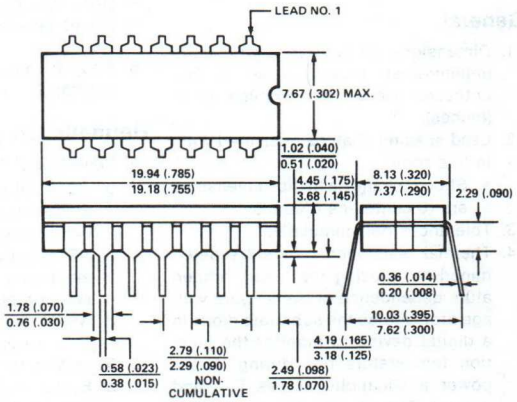
9. Lead material
   a. ASTM alloy F-15 (KOVAR) or equivalent—gold plated, tin plated, or solder dipped.
   b. ASTM alloy F-30 (Alloy 42) or equivalent—tin plated, gold plated, or solder dipped.
   c. ASTM alloy F-15 (KOVAR) or equivalent—gold plated.
10. Body Material
    a. Eyelet, ASTM alloy F-15 or equivalent—gold or tin plated, glass body.
    b. Ceramic with glass seal at leads.
    c. BeO ceramic with glass seal at leads.
    d. Ceramic with ASTM alloy F-30 or equivalent.
11. Lid Material
    a. Nickel or tin plated nickel, weld seal.
    b. Ceramic, glass seal.
    c. ASTM alloy F-15 or equivalent, gold plated, alloy seal.
    d. BeO ceramic with glass seal.
12. Signetics symbol, angle cut, or lead tab denotes Lead No. 1.
13. Recommended minimum offset before lead bend.
14. Maximum glass climb 0.010 inches.
15. Maximum glass climb or lid skew is 0.010 inches.
16. Typical four places.
17. Dimension also applied to seating plane.

PACKAGE OUTLINES

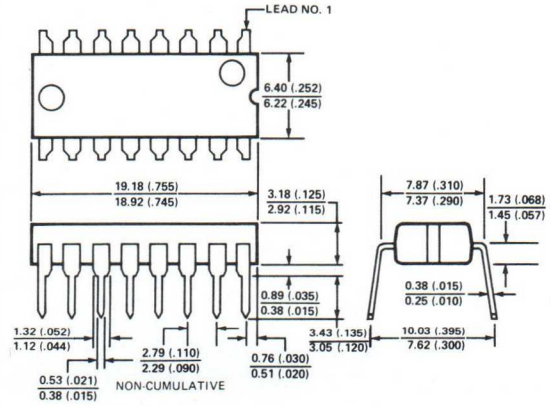
N PACKAGE PLASTIC (14-PIN DIP)



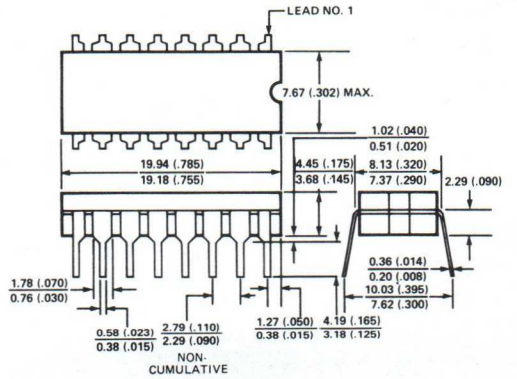
F PACKAGE CERAMIC (14-PIN DIP)



N PACKAGE PLASTIC (16-PIN DIP)

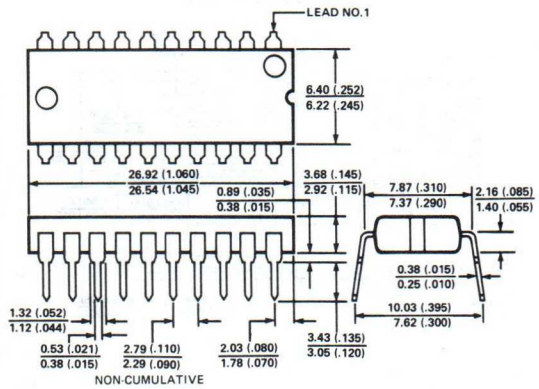


F PACKAGE CERAMIC (16-PIN DIP)

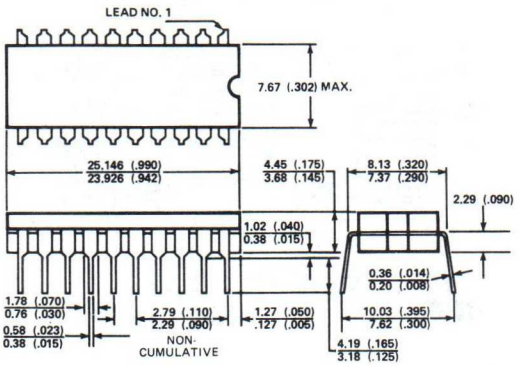


PACKAGE OUTLINES

N PACKAGE PLASTIC
(20-PIN DIP)



F PACKAGE CERAMIC
(20-PIN DIP)



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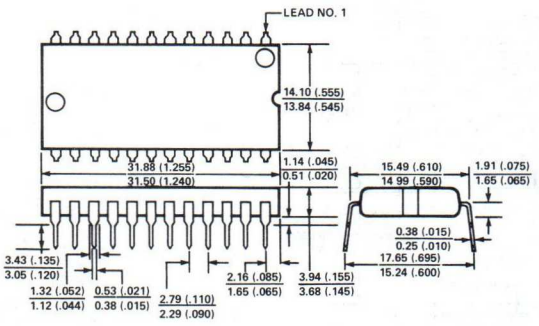
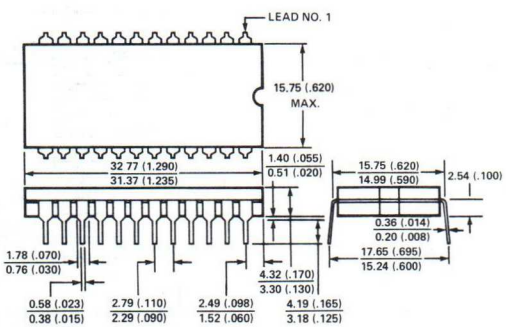
N PACKAGE PLASTIC
(24-PIN DIP)

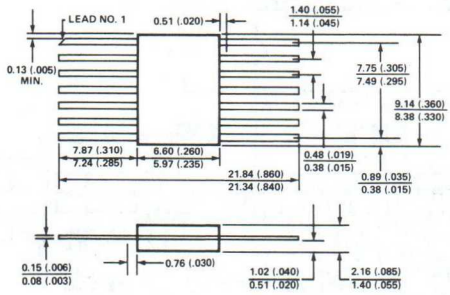


F PACKAGE CERAMIC
(24-PIN DIP)

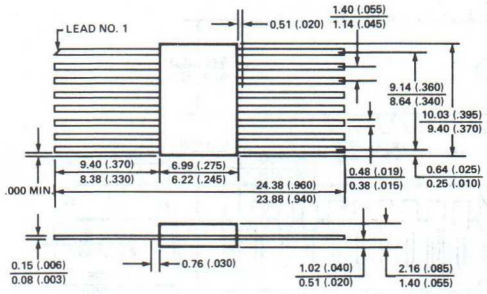


PACKAGE OUTLINES

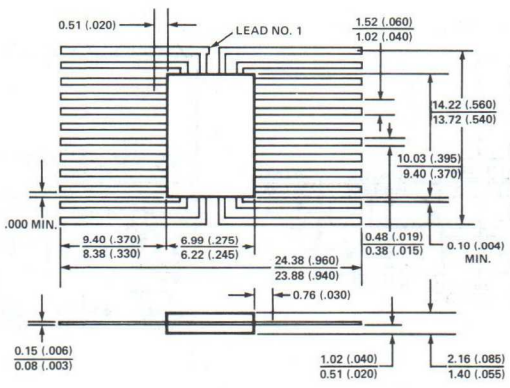
W PACKAGE CERAMIC (14-PIN FLATPACK)



W PACKAGE CERAMIC (16-PIN FLATPACK)



W PACKAGE CERAMIC (24-PIN FLATPACK)



NOTES

NOTES

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