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PRODUCT BOOK

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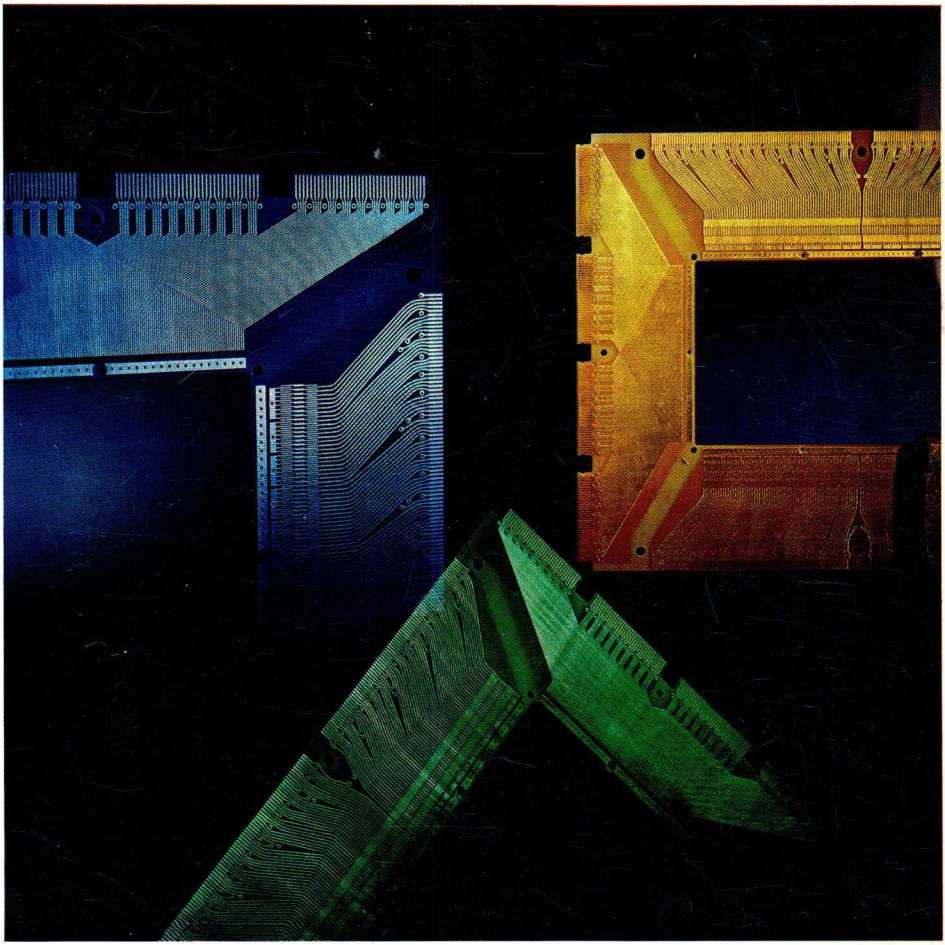
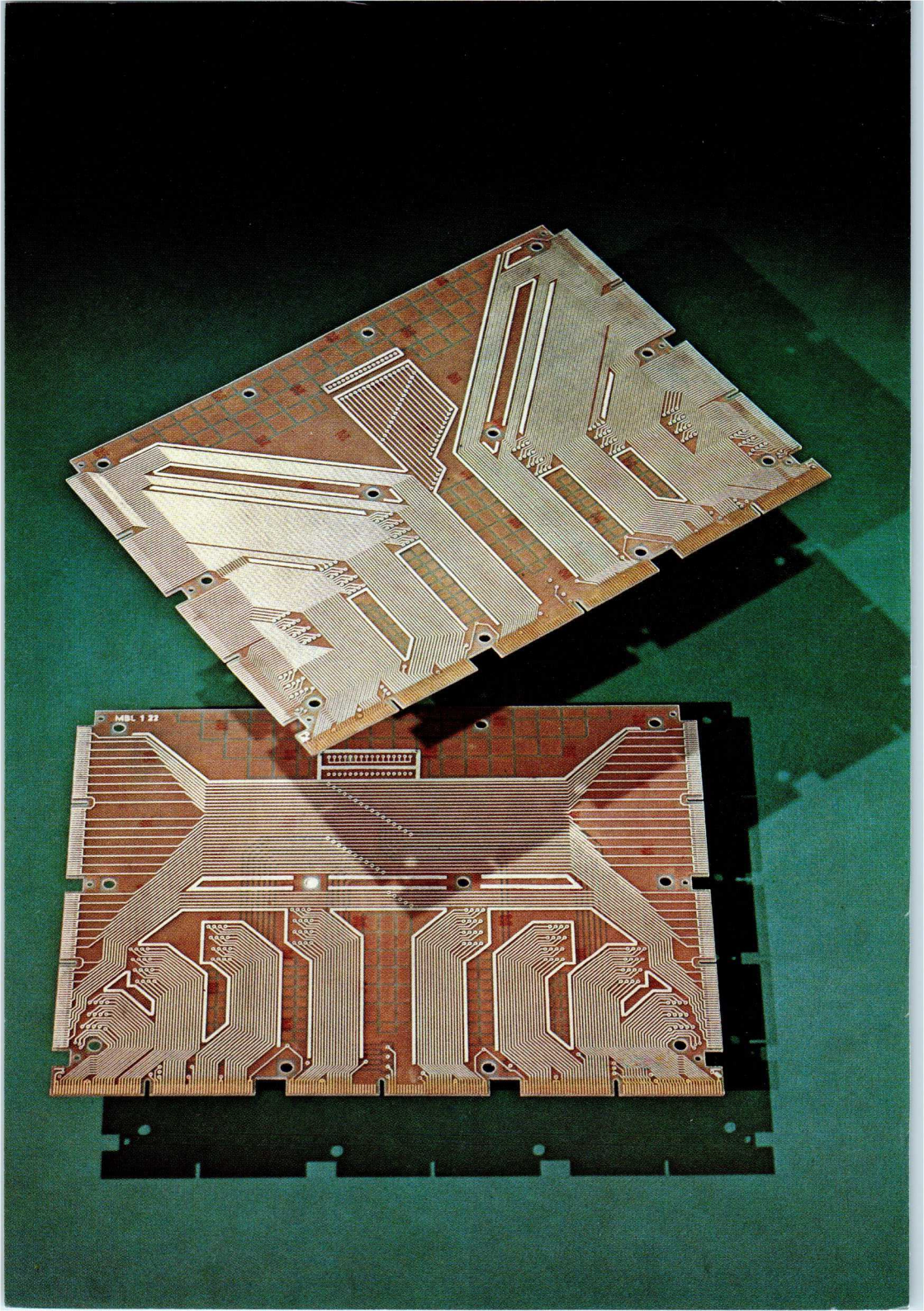
ELECTRONIC COMPONENTS AND MATERIALS

PRINTED CIRCUIT BOARDS

A guide to specifying and designing



Printed Circuit Boards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Printed Circuit Boards

A guide to specifying and designing

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PUBLICATIONS DEPARTMENT
ELECTRONIC COMPONENTS AND MATERIALS DIVISION

EINDHOVEN - The Netherlands

October 1971

Contents

Acknowledgement

Acknowledgement is made to W. van der Zwaal of the Development Laboratory, Eindhoven, who supplied the information on which this book is based.

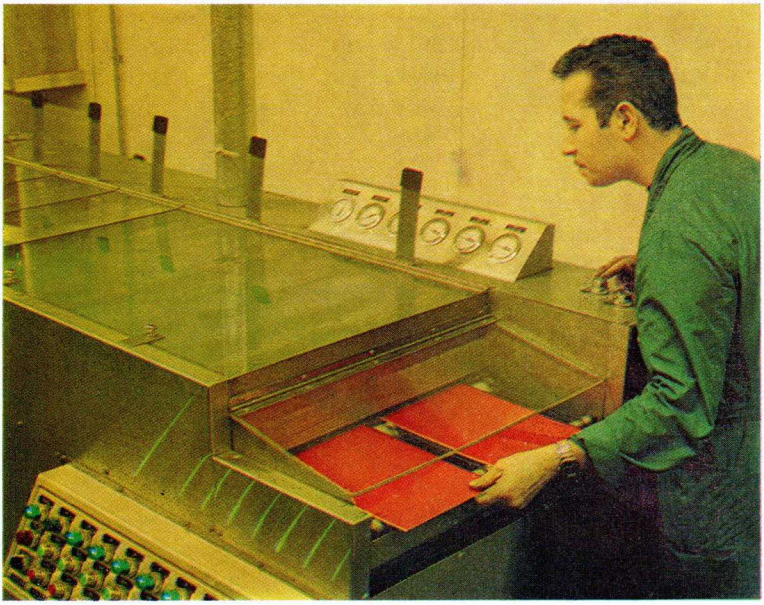
Foreword

This book is primarily intended as a working handbook to assist intending customers to produce their own designs for Printed Circuit Boards and, at the same time, make the most advantageous use of our production capability. It includes details on the selection of materials, processes and finishes and provides a standardised approach to specifying. This should help to obviate some of the fabrication difficulties which frequently have an unfavourable effect on the price and delivery of PCB's.

A second objective is to provide some insight into the scale and potential of our PCB manufacturing facility and also to indicate levels of quality and reliability which can be obtained when the right approach is made at the outset.

To-day's largest volume requirement for PCB's is for rigid double-sided boards with finely detailed wiring patterns and it is these which are discussed in this book. It is our experience that specifications for PCB's of this type are not always representative of the actual requirement and that they are frequently expressed in a manner which can be misinterpreted. Surprising though it may seem in these days of value engineering, where every component is subject to scrutiny, PCB's with, for example, inappropriate and costly platings and unnecessarily close tolerances, are regularly asked for. Precious metal finishes are often added purely for appearance since this is an important influence on the acceptability of high value products; but care must be exercised to make sure that eye-appeal is not at the expense of other properties. For instance, it may not be generally realised that gold diffusion can cause embrittlement of solder joints and that it is of small value as a protective finish unless a carefully controlled, impervious layer is deposited.

A supplier might sometimes feel inclined to advise his customer that a more economic and appropriate design is possible; but, at a stage where all the drawings and documentation have been raised, such advice is unlikely to be received with enthusiasm. It is to preclude the need for such advice that this book has been prepared.



Dry film processor

1 General

1.1 Introduction

Detailed recommendations follow for the design of rigid single and double-sided printed circuit boards, with or without plated-through holes and with or without edge-connectors. These recommendations are in accordance with the General Specification which appears as an Appendix at the rear of the book. Table 1.1 summarizes the main design considerations and cross-refers to later sub-sections where the various points are dealt with.

1.2 Definitions

Artwork – an accurately scaled representation of the conductor pattern layout which is used to produce the master pattern.

Master drawing – a drawing showing the dimensional limits or grid location applicable to any or all parts of a PCB, including the base.

Master pattern (or photo master) – a 1 to 1 scale pattern which is used to produce the conductor pattern within the accuracy specified on the master drawing.

These definitions are in accordance with Specification IPC.D. 310.

1.3 Classification of board types

The types of printed circuit boards discussed in this book are classified in Table 1.2.

1.4 Producing the conductor pattern

1.4.1 Subtractive process

From a base material clad on one or both sides with copper of, usually, 35 μm thickness, the excess copper is etched away to leave the desired conductor pattern.

Table 1.1 Summary of main design considerations

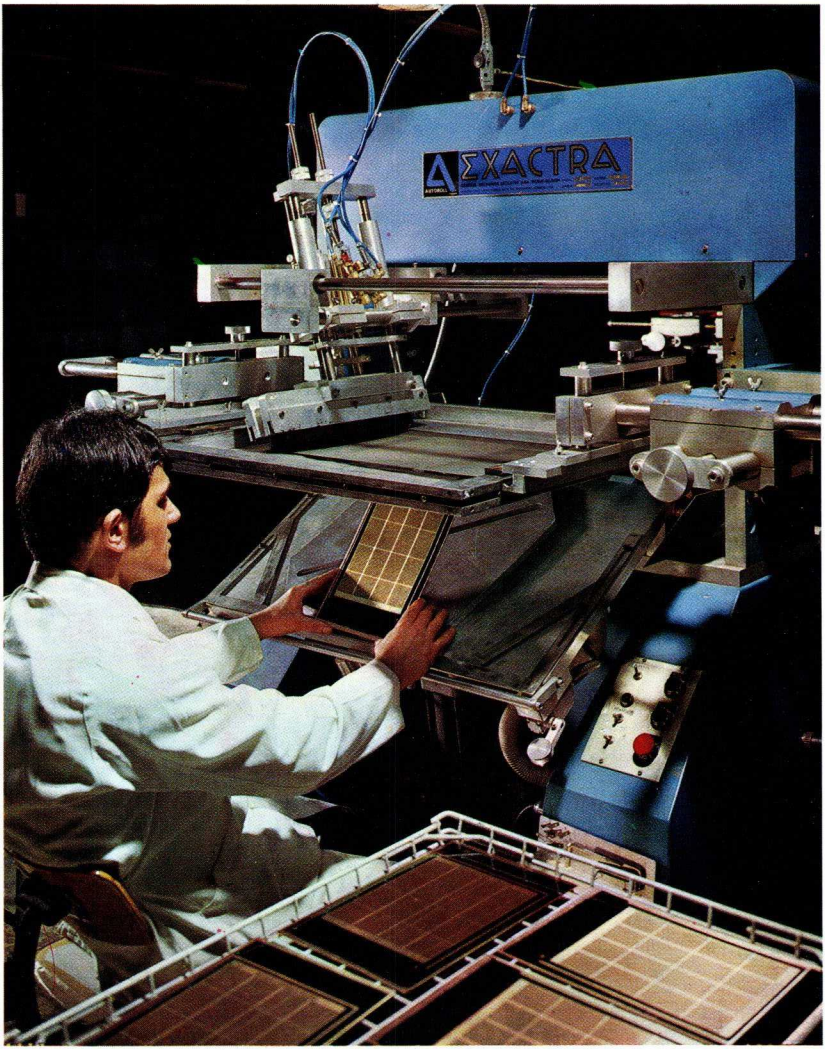
design consideration	recommendation	advantage gained	to be achieved by
length of production run	– as large as possible (see sub-section 3.1)	– acquisition of special tool justified	– standard outer dimensions for different patterns
dimensions	– as small as possible (see sub-section 3.4)	– less influence by tolerances – less reject cost	– adapting the electrical design
shape	– rectangular – without flatness limits (see sub-sections 3.1 and 3.5)	– ease of contour fabrication – reject percentage reduced	– adapting the device where the PCB is to be used
base material	– not paper base laminate – no specified supplier (see section 2)	– better hole quality – base material always available from stock	– accepting different makes and slight difference in colour
plated-through holes	– one hole diameter per board – diameter according to preferred diameter range – same hole pattern for as many board types as possible (see sub-section 3.2)	– cheaper	– adapting the electrical design and using suitable components

Table 1.1 (Continued)

pattern	– avoid fine detail wherever possible – even distribution – front to back registration as accurate as possible – suitable, correctly placed, distribution aids – eliminate effect of pattern on solderability (see Section 4)	– fewer rejects – better electro-plating quality – better hole solderability	– adapting the electrical design – following recommendations in Section 4
operating conditions	– arrange to be in accordance with para *A* 2.2 (see also sub-section 9.1)	– no need for extra investigation	– adapting the device where the PCB is to be used
master pattern (photo master)	– produce as accurately as possible – arrange front to back registration as accurately as possible (see sub-section 10.1)	– no delay in delivery (due to inaccurate master pattern)	– automated artwork generation – use of precision camera
master drawing (Engineering detail drawing)	– produced in a clear and unambiguous form (see sub-section 10.2)	– no misunderstandings, no delays in production	– employing a standard drawing system, preferably as recommended in sub-section 10.2

Table 1.2 PCB *Classification*

board type	plating	holes	process (see sub-section 1.2)	mask application (see sub-section 1.3)
single-and double-sided PCB's	plated	plated-through	subtractive	screen resist, reversed etch photopolymer dry film resist, reversed etch
			semi-additive	
		non-plated	subtractive	
	non-plated	plated-through	semi-additive	
		non-plated	subtractive	screen resist, direct photopolymer dry film resist, direct photo resist, direct



Semi-automatic screen printing machine.

1.4.2 Additive process

Copper is deposited on a dielectric material, by chemical reduction, to produce the desired conductor pattern. Etching is not required.

A variant of this method is the semi-additive process, here a copper layer is deposited on the entire surface of a plain base material by chemical reduction and then built-up to 5 μm thickness by electroplating. Thereafter, resist is applied and the copper in the holes and on the conductor pattern is built-up to the desired thickness by a further stage of electroplating. Finally the excess copper is removed by etching. Both the additive and the semi-additive processes are suitable for the production of PCB's with plated-through holes but without etch resistant electroplatings. From a printing point of view, copper-plated boards are preferred. For solderability see para 7.2.2. For organic coatings see subsection 6.5.

1.5 Resist Application Methods

1.5.1 Screen resist

Resist is forced through the openings of a tightly stretched screen, usually made of metal, onto the underlying board. The desired conductor pattern can be either the unmasked portion of the screen (see "direct method") para 1.5.5) or the masked portion (see "reversed etch method" para 1.5.4). Screen masking is accomplished photomechanically.

1.5.2 Photopolymer film resist

This is a dry film resist which forms a light-sensitive film when laminated to the board surface. For the reversed etch method it is exposed to light through a positive. For the direct method it is exposed through a negative of the desired wiring configuration. The light sensitive film is a negative photo-layer, so after development the exposed areas harden and are retained on the board.

Dry film resist techniques are particularly suitable for boards requiring plated-through holes and patterns too finely detailed for the screen-printing method. In addition, they enable boards with plated-through holes to be made with the conductor pattern and hole plating of bare copper. This is achieved by applying a positive resist on the plated board so that the holes are bridged over.

As the dry film is an etch resist, it seals the interiors of the plated-through holes and protects the walls during etching. This is known as the "tenting-over" technique.

1.5.3 Photo resist

This is a liquid light-sensitive resist which is applied on the board by dipping, and then dried.

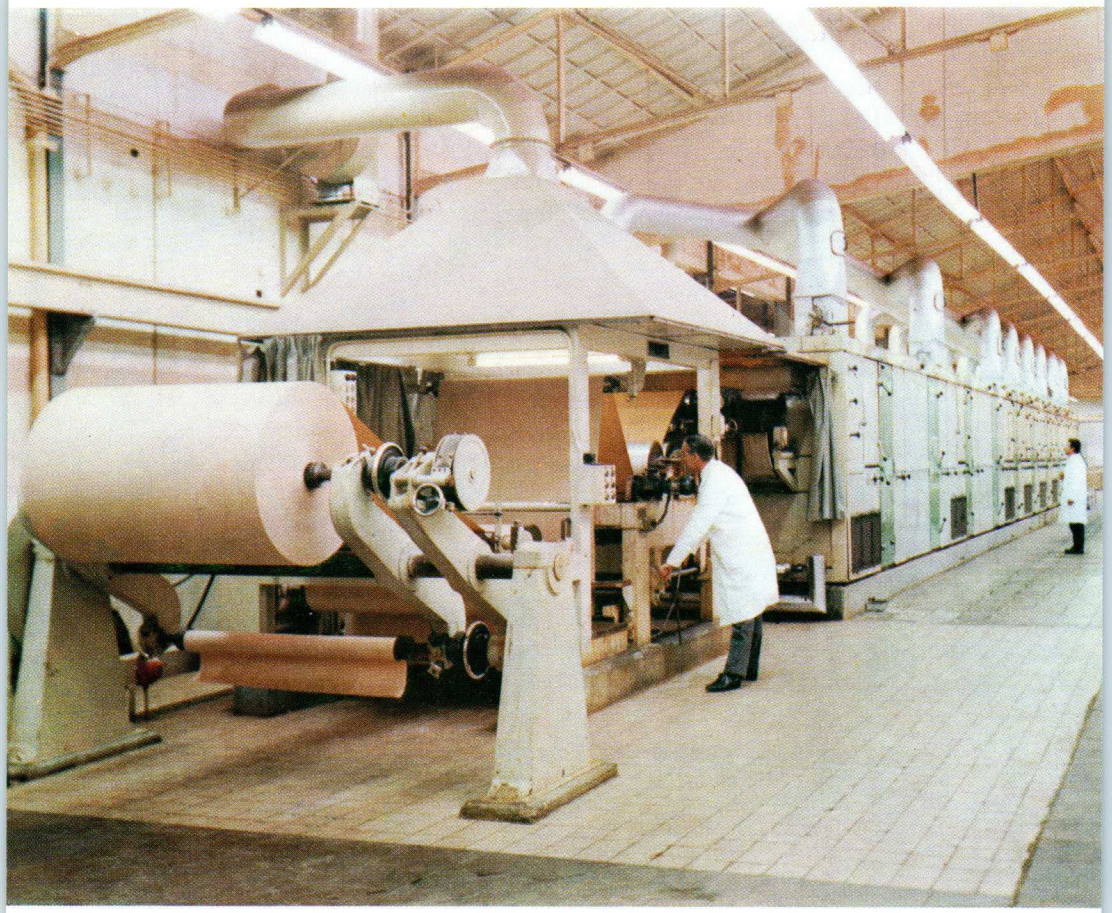
In most cases a negative resist is used so that the exposed areas are retained on the board after development. Liquid light sensitive resist is not recommended for boards with plated-through holes.

1.5.4 Reversed etch method

With this method a negative, or reverse resist pattern is applied over the unwanted metal. Copper is then electroplated on the walls of the holes and on the exposed conductor pattern. Finally a metal etch resist is applied in these areas. The negative resist pattern is then removed and the unwanted copper is etched away. After etching, the conductor side-faces consist of bare copper.

1.5.5 Direct method

With the direct method an etching resist, usually of the photo sensitive variety, is applied over the conductor pattern. This method is used for boards without plated-through holes and without electroplating.



Manufacture of base material.

2 Base materials

2.1 Classification

The most important base materials for PCB's fall into the following two main categories:

2.1.1 Paper base laminates

These consist of paper layers impregnated with synthetic resin and laminated under heat and high pressure. Paper base phenolic resin and paper base epoxy resin laminates are commonly used. They are unsuitable as base material for boards with plated-through holes where the electrical interfacial connection (see Section 5) is important.

Where they are used, non-reproducible warp and twist must be taken into consideration.

As a rule, paper base laminates are not recommended for professional applications.

2.1.2 Glass base laminates

These consist of glass-fabric or glass-fibre layers impregnated with synthetic resin and laminated under heat and high pressure. For PCB's with plated-through holes where the electrical interfacial connection is important, use is made of glass-fabric epoxy resin laminate and glass-fibre polyester resin laminate. Of the glass-fabric epoxy laminates the three most widely used grades are: FR-5 (flame retardant and temperature resistant); FR-4 (flame-retardant); and G-10 (general purpose). Of the glass-fibre polyester laminates the grade GC MIL-P13949D is preferred.

2.2 Essential Properties

2.2.1 Comparison of types

The values quoted in Table 2.1 are for comparison only since they may vary from supplier to supplier.

Table 2.1 Properties of base materials

property	paper base phenol	paper base epoxy	glass-fabric base epoxy	glass-fibre base polyester
min. peel strength (N/mm)	1.10	1.25	1.25	1.20
surface resistivity ($M\Omega$[1])	10^3	10^3	10^4	10^4
volume resistivity ($M\Omega$[1])	10^4	10^5	10^6	10^6
water absorption (%)	0.65	0.55	0.35	0.35
dielectric constant ε (f = 1 MHz)	5.3	5	5.8	3.4
dissipation factor tan $\delta \times 10^{-4}$ (f = 1 MHz)	500	450	450	115
min. flexural strength (N/cm^2)	7000	9000	31000	20000
max. operating temp. (°C)	110	110	125[2])	110
max. soldering time and temperature	5s /260 °C	15s /260 °C	30s /260 °C	10s /260 °C
price index	1	2.5	4	1.5

[1]) Surface and volume resistance measured after 96 h at 35 °C and 90% RH.
[2]) 125 °C for FR-4; 155 °C for FR-5, see 2.3.2

2.2.2 Surface and volume resistance

When the PCB's have plated-through holes, certain requirements are made on the surface resistance (conductor pattern) as well as on the volume resistance (plated-through holes).

The resistance measured on the board is a combination of both the surface and the volume resistance, and is referred to simply as the insulation resistance.

The surface and volume resistances quoted in the base material specifications cannot be translated directly into an insulation resistance for the PCB. This is because the changes in the resistances are influenced in a non-linear manner according to the pattern dimensions (spacings). Hence, the insulation resistance can only be determined by measurements performed on the actual PCB.

A further consideration is that differences are found after long-term damp heat tests.

Fig. 2.1 shows the change in insulation resistance at 28 °C and 94% RH measured on glass-fabric base epoxy and paper base phenol laminate PCB's of a given size. The difference in quality between the two laminates is evident.

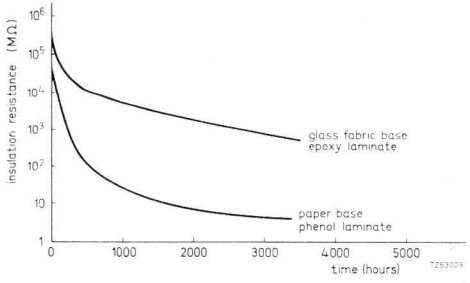


Fig. 2.1. Change in insulation resistance of paper base and glass fabric laminate at 28 °C and 94% RH.

The volume and surface resistance, as specified by the base material supplier, is determined by the "ring and disk" method given in IEC publication 249-1 (see para 9.3.5). In general, the volume resistance measured on plated-through holes at 0.1″ spacings will be less than this.

As a rule, the volume resistance of a PCB with plated-through holes must not change to a value of less than 100 MΩ during a humidity test.

2.2.3 Max. operating temperature

When PCB's, which have been subjected to a dip-soldering or wave-soldering operation, are used at the specified maximum operating temperature, a discoloration of the base material may occur. Hence, an operating temperature lower than the specified maximum operating temperature is recommended.

2.2.4 Flatness limits

The maximum warp or twist specified by the base material supplier relates to the base materials and not to the finished boards.

2.3 Material Specification and U.L. Approval

2.3.1 Base materials

These are covered by the following specifications:

MIL-P-139489	paper base epoxy laminates and glass-fabric base laminates.
NEMA LI-1	paper base phenol, paper base expoxy, and glass-fabric base laminates.
IEC-publ. 249-1	test methods for metal clad base materials for printed circuits.
IEC-publ. 249-2-1	phenolic cellulose paper, high electrical quality.
IEC-publ. 249-2-2	paper phenolic copper clad, economic grade.
IEC-publ. 249-2-3	epoxide cellulose copper clad laminated sheet, flame retardant grade.
IEC-publ. 249-2-4	epoxide woven glass fabric copper clad laminated sheet, general purpose grade.
IEC-publ. 249-2-5	epoxide woven glass fabric copper clad laminated sheet, flame retardant grade.

The tests and the test methods quoted in the various specifications may differ, but the base materials which satisfy the various specifications are interchangeable.

The governing specifications are primarily the IEC publications. However, these have not yet been adopted by the suppliers of base materials and thus the base materials available on the market are covered by MIL and NEMA specifications.

For some properties the suppliers' specifications quote values which are higher than the minimum specifications quoted in the MIL and NEMA specifications.

2.3.2 Base materials identification

Identification codes used in the various specifications are not standardised. The identifications for similar materials are given for comparison in Table 2.2.

Table 2.2 Base material identification by code

Type	NEMA	MIL	IEC 249-2-
phenol paper	xxxp	—	PF-CP-Cu-1
phenol paper, cold punching grade	xxxpc	—	-
epoxy paper, flame retardant	FR-3	PX	EP-CP-Cu-3
phenol paper, flame retardant	FR-2	—	-
epoxy glass-fabric, general purpose	G-10	GE	EP-GC-Cu-4
epoxy glass-fabric, flame retardant	FR-4	GF	EP-GC-Cu-5
epoxy glass-fabric, flame retardant and temperature resistant	FR-5	GH	-

Nearly all base materials of more than 0.8 mm thickness carry manufacturer's marks spaced at approximately 75 mm distance. The type of material is identified by the colour of the marks, see Table 2.3.

Table 2.3 Base material identification by colour

type	colour identification
glass-fabric, general purpose	white
glass-fabric, flame retardant	red
glass-fabric, temperature resistant	black
paper base, all types except flame retardant	any contrasting colour except red
paper base, flame retardant	red

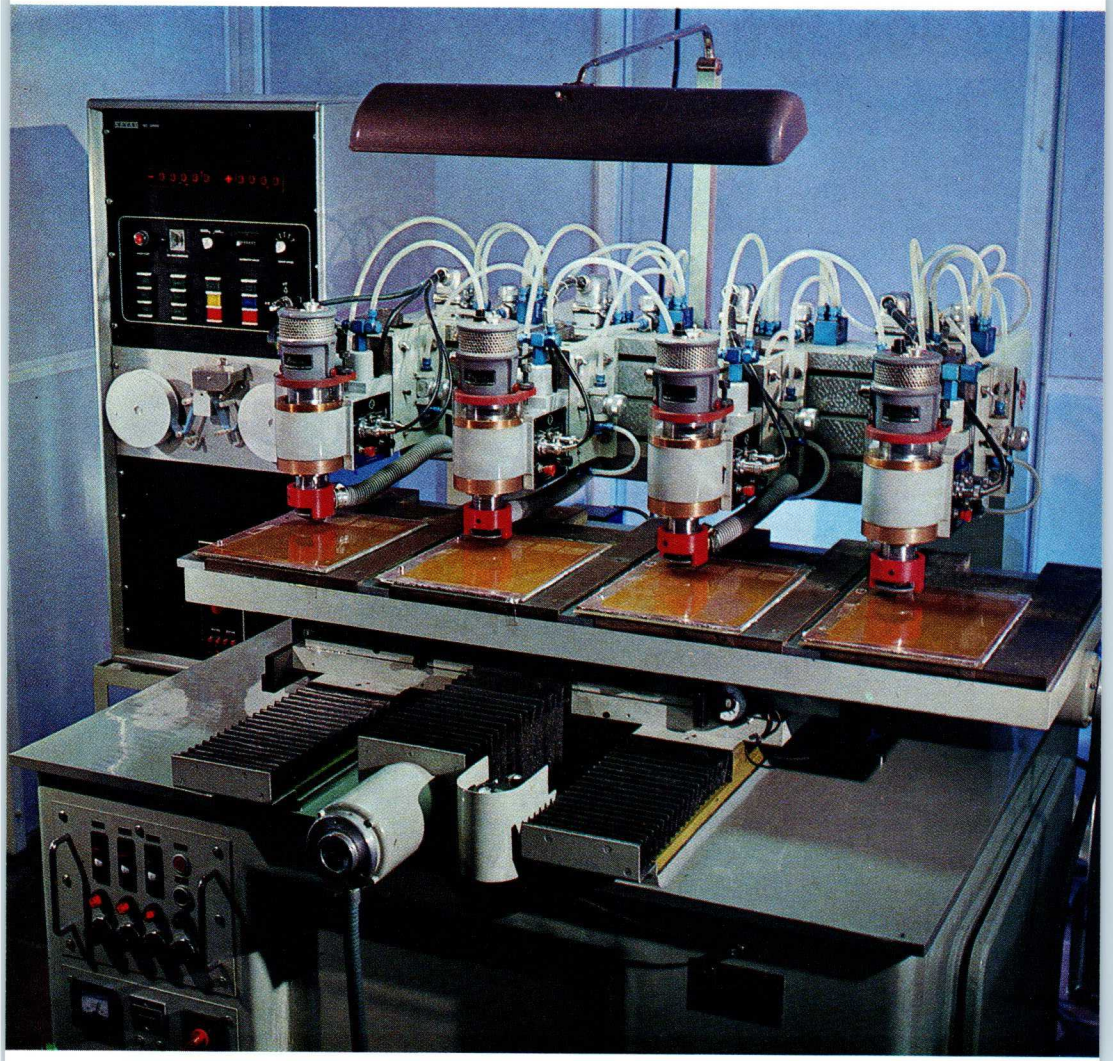
2.3.3 U.L. APPROVAL

The Underwriters' Laboratories Inc. approval for PCB's (see 9.4) may be obtained only if the base material has been given a U.L. file number.

The makes and types used by us and which have received U.L. approval are quoted in Table 2.4.

Table 2.4 U.L. Approved base materials

manufacturer	type	U.L. file number
mica-ply	G10, FR4 and FR5	E 39560
mas.	FR2, FR3, FR4, FR5 and G10	E 41668 - 67M 2482



Four-spindle n.c. drilling machine.

3 Board Fabrication

3.1 Board Contour and its Location w.r.t. Holes and Pattern

The three board contouring methods employed are sawing, milling, and punching. The choice depends on the quantity of boards involved, the shape of the board and the tolerance. The punching method is preferred and is invariably used for long production runs. For short production runs of rectangular shaped boards, the sawing method is used. Any cut-outs which are required in the rectangular contour are then accomplished by milling.

For short production runs of non-rectangular shaped boards the milling method is used.

For short production runs of rectangular shaped boards, where the dimensions are not critical, the size may be judged by eye, printed sawing marks then serving as a guide.

Whether long or short run production, the board contour should be kept simple, i.e. rectangular with no cut-outs.

3.1.1 Contouring by sawing with a sawing jig

This method employs a sawing jig centred on holes inside the board contour. The jig is moved past a straight-edge which is fixed with respect to the circular saw. The method is suitable for short production runs of rectangular boards.

Centring is accomplished by locating on three plated-through holes or, alternatively, two non-plated holes whose minimum diameter is 2 mm. The two non-plated holes provide the best anchorage and this method should always be used where awkward sized (very large, or very small) boards are being made.

Dimensioning and tolerancing (Fig. 3.1)

- The sides X and Y are specified with respect to one hole "A", which may or may not be plated-through.
- The tolerance on the dimensions 1, 2, 5 and 6 is $\pm$ 0.2 mm.
- The pattern is automatically fixed with respect to the contour.

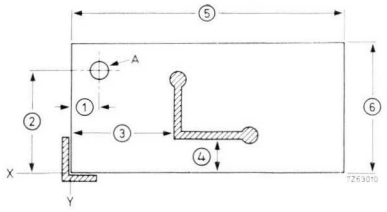


Fig. 3.1. Reference dimensions for rectangular PCB with no cut-outs.

- The dimensions 3 and 4 must not be entered (reference dimensions), they are shown here for information purposes only.
- The tolerance on the dimensions 3 and 4 depends on the pattern misalignment, which in turn depends on the pattern class.
- The tolerance is $\pm$ 0.5 mm for pattern class I.
  $\pm$ 0.33 mm for pattern class II and III.
- When the centring holes (A) are judged by eye, with printed centring areas serving as a guide, the tolerance on the dimensions 3 and 4 is $\pm$ 0.3 mm for all pattern classes.

3.1.2 Contouring by milling

This method employs a milling jig which is centred on two holes inside the board contour. The jig is moved by hand past the non-cutting section of a vertical end mill. The method is suitable for short production runs of boards of any shape.

Centring is accomplished by locating on two non-plated holes whose minimum diameter is 2 mm.

Dimensioning and tolerancing

As 3.1.1

3.1.3 Contouring by sawing without a sawing jig

The board size is judged by eye, printed sawing marks serving as a guide. This method is suitable for short production runs of rectangular boards where the board dimensions are not critical.

Dimensioning and tolerancing (Fig. 3.1)

- Dimensioning is superfluous when the entire contouring operation consists of sawing to printed sawing marks.
- If two sides are cut by sawing to a stop, then the dimensions 5 and 6 have to be entered.
- When sawing to printed sawing marks only the tolerances are as follows:

  Dimensions 1 and 2: $\pm$ 0.8 mm for pattern class I
  $\pm$ 0.6 mm for pattern class II and III
  3 and 4: $\pm$ 0.5 mm, independent of pattern class.
  5 and 6: $\pm$ 1 mm, independent of pattern class.
- When the sides X and Y are cut by sawing to printed sawing marks and the two opposite sides by sawing to a stop, the tolerance on the dimensions 5 and 6 is $\pm$ 0.2 mm.

3.1.4 Contouring by punching

A die is used to cut the board to size in one or more operations. As the dies are expensive, this method is used only where the length of the production run justifies the cost. Two non-plated holes are used for centring.

Punching may be carried out at ambient temperature, or at a slightly higher temperature attained by preheating.

Dimensioning and tolerancing (Fig. 3.1)

- The sides X and Y are specified with respect to a plated-through hole.
- The tolerance on the dimensions 1, 2, 5 and 6 is $\pm$ 0.15 mm.
- The pattern is automatically fixed with respect to the contour.
- The dimensions 3 and 4 must not be entered (reference dimensions).
- The tolerance on the dimensions 3 and 4 depends on the pattern class.
- The tolerance is $\pm$ 0.5 mm for pattern class I
  $\pm$ 0.3 mm for pattern classes II and III

3.1.5 Making cut-cuts by milling to a stop

Two sides are moved by hand past a stop which is adjustable with respect to a vertical end mill.

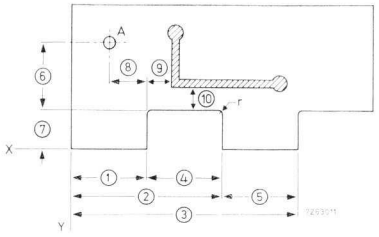


Fig. 3.2. Reference dimensions for PCB with cut-outs.

Dimensioning and tolerancing (Fig. 3.2)

- The dimensions are specified from the sides X and Y which serve as stops during the milling operation.
- Only the dimensions 1, 2, 3 and 7 are entered.
- The tolerance on the dimensions 1, 2, 3 and 7 is $\pm$ 0.1 mm.
- The corners should be provided with a radius of not less than 1.5 $\pm$ 0.5.
- The dimensions 4, 5, 6, 8, 9 and 10 must not be entered (reference dimensions).

Note 1 (board contouring to method 3.1.1)
The tolerance on the dimensions 6 and 8 is $\pm$ 0.3 mm and the tolerance on the dimensions 9 and 10 is $\pm$ 0.6 mm for pattern class I and $\pm$ 0.4 mm for pattern class II and III.

Note 2 (board contouring to method 3.1.3)
The tolerance on the dimensions 6 and 8 is $\pm$ 0.9 mm for pattern class I and $\pm$ 0.7 mm for pattern class II and III; the tolerance on the dimensions 9 and 10 is $\pm$ 0.6 mm irrespective of the pattern class.

3.1.6 Milling cut-outs by means of a milling jig

As mentioned in para 3.1.2, with the cut-outs being part of the contour.

Dimensioning and tolerancing (Fig. 3.2)

- The dimensions 1, 3, 4 and 7 are entered.
- The tolerance on these dimensions is $\pm$ 0.2 mm.

- The dimensions 6, 8, 9 and 10 are not entered (reference dimensions)
- The tolerance on the dimensions 6 and 8 is $\pm$ 0.2 mm.
- The tolerance on the dimensions 9 and 10 is $\pm$ 0.3 mm for all pattern classes.
- With this method, centring holes with respect to pattern have to be made by eye, with printed centring areas serving as a guide.

3.2 Hole Size

3.2.1 Plated-through holes

The plated-through hole diameter must satisfy the following requirement:
Nominal hole diameter in whole tenths of millimeters $=$

$$\geqslant \frac{\text{nominal board thickness}}{3}$$

Preferred diameters are: 0.6 ($\pm$ 0.1), 0.8 ($\pm$ 0.1), 1 ($\pm$ 0.13), 1.3 ($\pm$ 0.13) mm. Interfacial connection in double-sided PCB's up to 1.6 mm in thickness may be made via a plated-through hole of 0.5 (-0.2) mm diameter. That is if the plated-through hole is not to be used for component mounting.

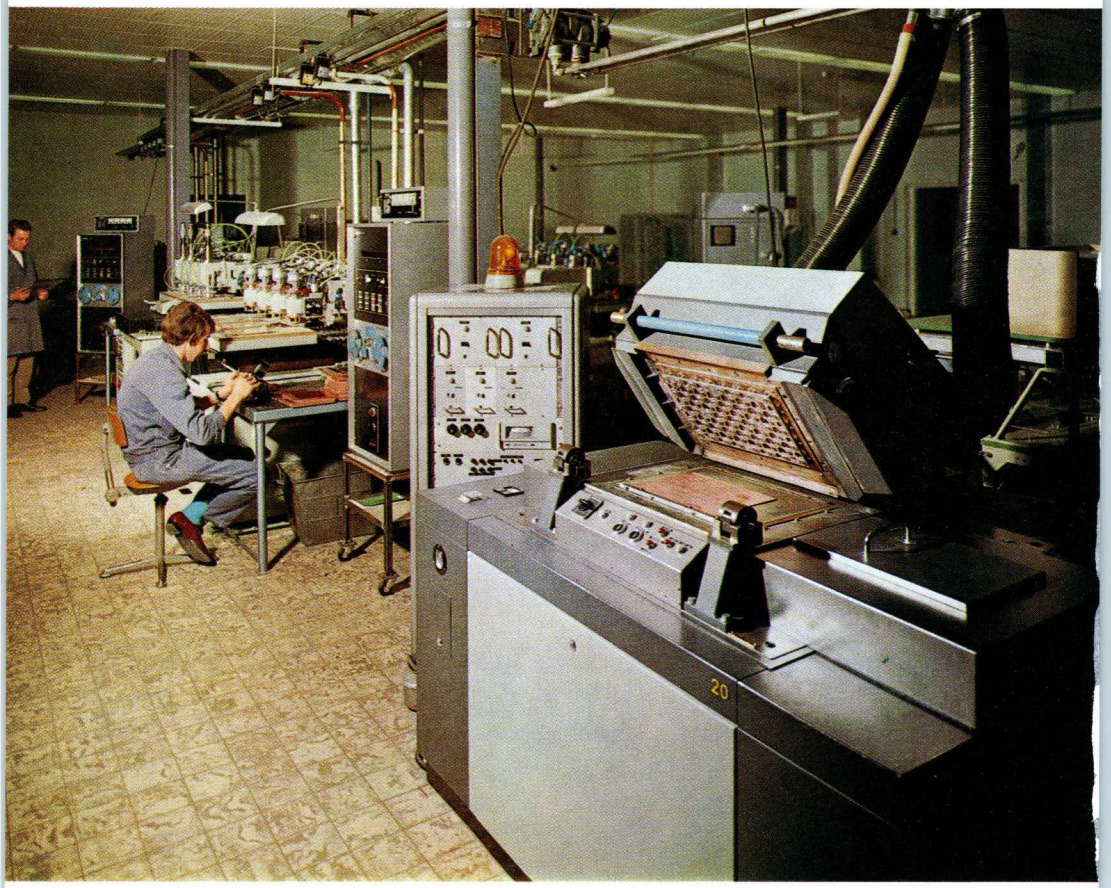
3.2.2 Non-plated holes

Drilled plain holes of any diameter are available in whole tenths of millimeters.
The tolerance on the diameter is:

$\pm$ 0.05 mm when diameter is $\leqslant$ 0.8 mm
$\pm$ 0.1 mm when diameter is $\leqslant$ 0.9 mm.

In the case of punched holes, the diameter and tolerance depend on the die used, but in general the tolerance on the diameter will be $\pm$ 0.1 mm. The diameter must not be less than:

$$\frac{\text{nominal board thickness}}{2}$$



Forty-spindle automatic jig drilling machine (foreground).

3.3 Tolerance on Hole Spacing

3.3.1 Plated-through holes

These holes are drilled with a numerically controlled drilling machine programmed with information on hole location via a punched tape. In principle the tape information may be derived from one of three sources:

I The master pattern.
II A list of co-ordinates.
III Direct from a tape used to programme a numerically controlled drawing machine for artwork generation.

Method I

- The drilled holes have a radial deviation of max. 0.08 mm with respect to the location on the master pattern.
- The tolerance on the hole spacing is $2 \times 0.08 = \pm 0.16$ mm with respect to the master pattern.
- The hole spacing of the finished board is guaranteed with respect to the spacing on the master pattern.
- When the spacing is more than 200 mm, a larger tolerance must be taken into consideration. This is due to expansion or shrinkage during the PCB fabrication process (see para 3.4.1).
- No requirements can be made on the nominal hole spacing since this depends on the accuracy of the artwork, the master pattern and the punched tape information.
  This undefined hole spacing may present difficulties when components are mounted on the printed board by automatic methods.
- As the hole and pattern locations are derived from the same master, the pattern to hole registration is good.

Method II

- When the pattern is not made on a numerically controlled drawing machine, the hole location is determined independently from the pattern. The pattern to hole registration is then determined by the accuracy achieved in the artwork.
- In practice, artwork not made by an automatic method does not possess sufficient accuracy of hole to terminal-area registration and therefore this method cannot be adopted.

Method III

- This method is preferred since the hole and the pattern locations are determined from the same coordinates.
- The drilled holes have a radial deviation of max. 0.05 mm with respect to the master pattern.
- The tolerance on the hole spacing is $2 \times 0.05 = \pm 0.1$ mm with respect to the master pattern.
- The hole spacing of the finished board is guaranteed with respect to the spacing on the master pattern.
- When the hole spacing is more than 200 mm, a tolerance increase must be taken into consideration. This is due to expansion or shrinkage during the PCB fabrication process (see para 3.4.1).
- This method permits the highest possible accuracy as far as the registration of the pattern, holes, and hole spacing is concerned.
- It is the obvious method to employ when automated component mounting techniques are in use.

3.3.2 NON-PLATED HOLES

Three methods are available for obtaining non-plated holes. They are always made after PCB fabrication has been completed, unless the dry film resist "tenting over" technique is used.

Method I Reaming a plated-through hole

- A pre-requisite is that the plain hole is at least 0.5 mm larger than the plated-through hole and that it is indicated on the master pattern, or on the tape for the numerically controlled drilling machine.
- Reamed holes have a radial deviation of 0.1 mm with respect to the location on the master pattern.
- The tolerance on the hole spacing is $2 \times 0.1 = \pm 0.2$ mm when method 3.3.1 (I) is used, and the radial deviation is 0.075 mm (tolerance on the hole spacing is $2 \times 0.075 = \pm 0.15$ mm) when the plated-through holes are made by method 3.3.1 (II)
- When the hole spacing is more than 200 mm, a tolerance increase must be taken into consideration. This is due to expansion or shrinkage of the base material during the PCB fabrication process (see para 3.4.1).

Method II Drilling by means of the numerically controlled drilling machine

- Holes of diameter up to 4 mm, may be made by means of the numerically controlled drilling machine.
  The tolerance on the location of these holes is as in method 3.3.1 (III).
- A separate tape has to be made to provide hole location information in terms of the coordinates.

Method III Using a drilling jig

- Tolerance on hole spacing is:
  $\pm$ 0.05 mm when spacing is $\leqslant$ 200 mm
  $\pm$ 0.1 mm when spacing is $>$ 200 mm
- The drilling jig may be centred with respect to the board edge.
- The tolerance on the hole location with respect to the board edge is $\pm$ 0.1 mm.

3.4 Dimensional Changes Caused by Shrinkage and/or Expansion of the Base Material

The characteristics of the base material influence the ultimate board size in two ways:

3.4.1 Permanent dimensional changes caused by the PCB fabrication process

This should be taken into account when determining the hole spacing for the master pattern or tape for the drilling machine. It relates to holes made at the start of the PCB fabrication process, i.e. plated-through holes; and plain holes made by reaming plated-through holes. These are subject to the cumulative effects of the entire fabrication process. When the hole spacing is more than 200 mm, an extra deviation must be taken into consideration (see also sub-section 3.3). This is $+0.05\%$ for glass fabric and -0.125% for paper base phenol.

Mechanical operations carried out after the completion of the fabrication process do not require a dimensional change allowance.

3.4.2 Dimensional changes in the finished board due to temperature

The specified coefficient of linear expansion enables the dimensional change to be calculated, but the change occurring in practice may deviate from the calculated change. This is because the coefficients of expansion may vary according to supplier and the change with temperature is not always linear.

The approximate figures are $1.5 \times 10^{-5}/°C$ for glass fabric, $1.7 \times 10^{-5}/°C$ for paper base phenol and $2.5 \times 10^{-5}/°C$ for paper base epoxy.

3.5 Flatness Limits

In the board fabrication process the flatness of the base material which is specified on the applicable material standard (see para 2.2.4), is influenced in a non-reproducible way by the shape and distribution of the pattern. Flatness limits specified on the board drawing, may never be better than those quoted for the base material.

As flatness is a hardly reproducible variable on which the board manufacturer has little or no control, its specification on the board drawing usually implies an extra high reject percentage due to the boards being outside the specified limit. Thus it is always advisable to take a certain warpage into consideration when designing the device in which the board is to be housed.

3.5.1 Specifying flatness

Any departure of the board from being a flat surface has previously been specified in terms of "warp" and "twist". In view of the difficulty of defining what precisely constitutes "warp" as distinct from "twist", a recent IEC publication proposes that the future criterion be "flatness".

The proposed means of specifying a maximum permissible deviation from flatness is by reference to a specified maximum radius of curvature of the PCB diagonal. This is described in sub-section *A*5.2.

4 Pattern

4.1 General

A master pattern will always be required whatever the fabrication process may be. It is a precision photo reduction derived from a large scale artwork. Details on the production of artwork are given in Section 10.

Depending upon which fabrication process is adopted, the finished PCB will exhibit certain deviations from the master pattern. The width of the conductors and the diameter of the terminal areas will differ from those on the master pattern. The conductor edges may exhibit blemishes and the pattern as a whole will exhibit a certain misalignment with respect to the holes. Allowance has therefore to be made on the artwork to accommodate these deviations. Since they will be dependent on the fabrication process, separate artworks will be required if the same pattern is to be used with different processes.

The maximum allowable process-dependent deviations are quoted in the Appendix, Table *A*2. The dimensions of the finished PCB are guaranteed to be within the specified maximum allowable deviations, but only with respect to the master pattern.

4.2 Pattern Classes

The specifications given in the Appendix refer to "Board classes". Each class represents a degree of processing difficulty resulting from a combination of board size and pattern detail. Obviously, the larger the board and the finer the pattern, the greater will be the effects of tolerances and the difficulties of inspection.

The Appendix lists a number of board sizes (Table *A*1) and a number of pattern classes (Table *A*2) and also indicates their possible combinations to form board classes. The board sizes quoted in Table *A*2 are nett sizes which are mandatory maxima in a given board class. In principle there are no limitations on size. As soon as a board size appertaining to a board class is exceeded, the next board class will become applicable and the maximum board size will be the size appertaining to that class. Small sizes may be combined into a large size and in that case an edge of at least 5.08 mm (2e) has to be left around each of the small sizes, i.e. a spacing of 4e between the board outlines.

When the desired conductor width and spacing are minimum values, the most critical feature of a pattern class, as quoted in Table *A*2, is the conductor pitch, since the closer the tolerances in a given process, the smaller the conductor pitch will be. Table *A*2 also quotes a minimum conductor pitch for each class, it being assumed that the conductor width and spacing of the finished PCB are also minimum values.

A pattern may combine several pattern classes. In that case the board class is based on the distribution and number of the most difficult pattern classes occurring in the pattern. Wherever possible, the conductors and conductor spacing should be made wide and the terminal areas large. Difficult pattern classes should be avoided, except where absolutely necessary. The Appendix includes graphs to show how the limits can be found for dimensions of the finished board from the corresponding master pattern dimensions. A method of determining the artwork dimensions from the specified minimum conductor width and spacing of the finished PCB follows in sub-section 4.5.

4.3 Pattern Tolerances

To determine the pattern tolerance (i.e. the limits within which the pattern of the finished PCB may deviate from the design dimensions) two types of deviation must be identified. First, the deviations which occur in the artwork and the master pattern (master pattern tolerance) and second, deviations which occur when the PCB is made (fabrication tolerance).

4.3.1 Master pattern tolerance

This tolerance defines the limits within which the dimensions and locations of conductors and terminal areas, as measured on the master pattern, may deviate from the corresponding design figures. The tolerance is necessary to allow for the accumulated deviations occurring when the artwork and master pattern are made. The maximum permissible master pattern tolerances are specified for each pattern class in Table *A*2.

4.3.2 Fabrication tolerance

This defines the limits within which the pattern of the finished PCB may deviate from the master pattern. It relates to conductor width and terminal area diameter and to blemishes in the pattern edges.

Fabrication tolerance on conductor width and terminal area diameter

This defines the limits within which the width of conductors and the diameter of terminal areas may deviate from the corresponding width and diameter measured on the master pattern. It allows for deviations occurring when the resist pattern is applied and for possible overhang of the plating.

The tolerance depends on the processing method and is given for each pattern class in Table *A*2.

Blemishes along the edges of the conductor pattern

According to the adopted processing method, blemishes occur to a greater or lesser degree along the edges of the conductor pattern. They can be isolated projections (excess metal) or isolated indentations or voids (missing metal). Any excess metal reduces the conductor spacing and missing metal reduces the conductor width. These blemishes have to be accounted for in the artwork.

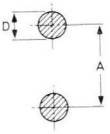
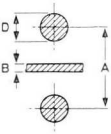
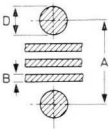
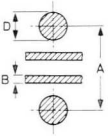
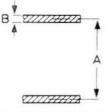
The maximum permissible excess metal is expressed as a percentage of the minimum conductor spacing of the finished board and the maximum permissible missing metal is expressed as a percentage of the minimum conductor width of the finished board. Both are specified in Table *A*2 on page 106 for each processing method and each pattern class.

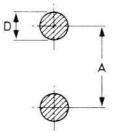
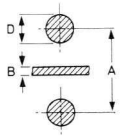
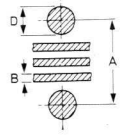
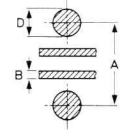
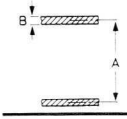
4.4 Misalignment of Pattern with Respect to Holes

The misalignment is not measured directly. It is derived by measuring the smallest distance from the hole edge to the terminal area edge on the finished PCB. The *minimum* permissible distance is specified in Table *A*2. The misalignment of the pattern varies according to the processing method. The minimum alignment tolerance needed in the pattern fabrication process by a given method, is specified in Table *A*2.

The minimum misalignment of the finished PCB pattern needed in the fabrication process is defined as follows: it is the distance by which a minimum diameter terminal area may be out of position, with respect to a maximum diameter non-plated or plated-through hole, which still provides that the permissible minimum distance from hole edge to terminal area edge is not violated. The minimum permissible terminal area diameters which are in accordance with the above, are specified per pattern class in Table *A*2. These diameters are nominal artwork dimensions on 1 to 1 scale. It is recommended that the largest possible terminal area diameter should be used. The larger the board, the larger the terminal area diameter should be.

Table 4.1 Nominal artwork dimensions

configuration	average hole diameter	screen resist to para 1.5.1. minimum pitch A	B	D	pitch in inches A	B	D	format
	0.6 ± 0.1	1.66	—	1.2	1.9053(4e)	—	1.4	≦ 2
								> 2
	0.8 ± 0.1	1.86	—	1.4	1.9053(4e)	—	1.4	≦ 2
								> 2
	1 ± 0.13	2.06	—	1.6	2.54(1e)	—	2	≦ 2
								> 2
	1.3 ± 0.13	2.36	—	1.9	2.54(1e)	—	2	≦ 2
								> 2
	0.6 ± 0.1	2.33	0.25	1.2	2.54(1e)	0.35	1.2	≦ 2
						0.25	1.4	> 2
	0.8 ± 0.1	2.53	0.25	1.4	2.54(1e)	0.25	1.4	≦ 2
								> 2
	1 ± 0.13	2.73	0.25	1.6	3.1755(4e)	0.35	1.8	≦ 2
						0.3	1.9	> 2
	1.3 ± 0.13	3.03	0.25	1.9	3.1755(4e)	0.35	1.9	≦ 2
						0.25	2	> 2
	0.6 ± 0.1	3	0.25	1.2	3.1755(4e)	0.3	1.2	≦ 2
						0.25	1.3	> 2
	0.8 ± 0.1	3.2	0.25	1.4	3.811(5e)	0.35	1.4	≦ 2
						0.3	1.6	> 2
	1 ± 0.13	3.4	0.25	1.6	3.811(5e)	0.35	1.6	≦ 2
						0.3	1.9	> 2
	1.3 ± 0.13	3.7	0.25	1.9	3.811(5e)	0.25	1.9	≦ 2
						0.25	2	> 2
	0.6 ± 0.1	3.7	0.25	1.2	3.811(5e)	0.25	1.2	≦ 2
						0.25	1.3	> 2
	0.8 ± 0.1	3.9	0.25	1.4	4.457(4e)	0.4	1.4	≦ 2
						0.3	1.6	> 2
	1 ± 0.13	4.1	0.25	1.6	4.457(4e)	0.35	1.6	≦ 2
						0.3	1.8	> 2
	1.3 ± 0.13	4.4	0.25	1.9	4.457(4e)	0.25	1.9	≦ 2
						0.25	1.9	> 2
	—	0.675	0.25	—	0.76(30 mil)	0.3	—	≦ 2
								> 2
master pattern tolerance	on width: ± 0.025, on pitch: ± 0.03, top-bottom: ± 0.05							

configuration	average hole diameter	dry film resist to para 1.5.2						for-mat
		minimum pitch			pitch in inches			
		A	B	D	A	B	D	
	0.6 ± 0.1	1.47	—	1.2	1.9053(4e)	—	1.4	≦ 2
							1.6	> 2
	0.8 ± 0.1	1.67	—	1.4	1.9053(4e)	—	1.5	≦ 2
							1.6	> 2
	1 ± 0.13	1.87	—	1.6	1.9053(4e)	—	1.6	≦ 2
							1.6	> 2
	1.3 ± 0.13	2.17	—	1.9	2.54(1e)	—	2	≦ 2
							2.2	> 2
	0.6 ± 0.1	1.97	0.25	1.2	2.54)1e)	0.35	1.4	≦ 2
						0.3	1.5	> 2
	0.8 ± 0.1	2.17	0.25	1.4	2.54(1e)	0.35	1.5	≦ 2
						0.3	1.6	> 2
	1 ± 0.13	2.37	0.25	1.6	2.54(1e)	0.3	1.6	≦ 2
								> 2
	1.3 ± 0.13	2.67	0.25	1.9	3.1755(4e)	0.4	1.9	≦ 2
						0.3	2.2	> 2
	0.6 ± 0.1	2.47	0.25	1.2	2.54(1e)	0.25	1.2	≦ 2
								> 2
	0.8 ± 0.1	2.67	0.25	1.4	3·1755(4e)	0.35	1.4	≦ 2
						0.3	1.6	> 2
	1 ± 0.13	2.87	0.25	1.6	3.1755(4e)	0.35	1.6	≦ 2
								> 2
	1.3 ± 0.13	3.17	0.25	1.9	3.1755(4e)	0.25	1.9	≦ 2
								> 2
	0.6 ± 0.1	2.97	0.25	1.2	3.1755(4e)	0.3	1.2	≦ 2
								> 2
	0.8 ± 0.1	3.17	0.25	1.4	3.1755(4e)	0.25	1.4	≦ 2
								> 2
	1 ± 0.13	3.37	0.25	1.6	3.811(5e)	0.35	1.6	≦ 2
						0.25	1.8	> 2
	1.3 ± 0.13	3.67	0.25	1.9	3.811(5e)	0.25	1.9	≦ 2
								> 2
	—	0.508	0.25	—	0.508(20 mil)	0.25	—	≦ 2
								> 2
master pattern tolerance	on width: ± 0.02, on pitch: ± 0.02 top-bottom: ± 0.03							

4.5 Establishing Artwork Dimensions

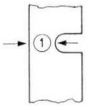
In order to establish the dimensions, the pattern class (see para 4.2) has to be known. If the pattern class is not known, the procedure is started on the basis of the least fine class and if the available space is found to be insufficient, a finer class is adopted. The calculated dimensions for the artwork have to be multiplied by an enlargement factor, as, where possible, the artwork should be prepared on the largest possible scale.

4.6 Minimum Pattern Configuration

Table 4.1 shows various configurations and the required minimum pitch, minimum conductor width and minimum terminal area diameter. All dimensions quoted in Table 4.1 are nominal artwork dimensions based on the minimum finished PCB conductor width and spacing being not less than 0.2 mm. The nearest raster dimension is given for each minimum spacing (1e = 2.54 mm). These raster dimensions are, in general, larger than the minimum possible pitch. The difference is distributed over the conductor width, conductor spacing, and terminal area diameter, in a manner which is favourable from a printing point of view according to PCB size (see sub-section *A* 2.1).

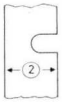
The dimensions are calculated according to the sequence below. The relevant tolerances are specified in Table *A*2, together with the percentages of "missing" or "excess" metal.

1. Minimum conductor width on finished PCB in places where there are indentations and when width on master pattern is at its minimum. This is a "given" value decided by arrangement between customer and supplier.

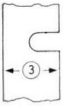


2. Minimum conductor width on finished PCB when width on master pattern is at its minimum. This is calculated from the maximum permissible percentage of "missing" metal.

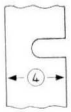
$$2 = \frac{100}{100 - \%\ \text{missing metal}} \times 1$$



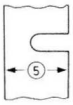
3. Nominal conductor width on finished PCB when width on master pattern is at its minimum. Calculated from the minus tolerance on the conductor width.
   $3 = 2 +$ (minus tolerance on conductor width)



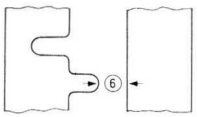
4. Nominal conductor width on artwork.
Calculated from the minus master pattern tolerance.
$4 = 3 +$ (minus master pattern tolerance on conductor width)



5. Maximum conductor width on finished PCB. Calculated from the plus tolerance on conductor width and the plus tolerance on master pattern.
$5 = 4 +$ (plus tolerance on conductor width) $+$ (plus master pattern tolerance).
Remark: Minimum conductor width may be adhered to as in point *1*.
Percentage missing metal is then greater than in point *2*.



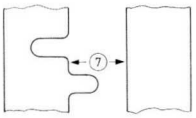
6. Minimum conductor spacing on finished PCB in places where there is excess metal. This is a "given" value which is decided by arrangement between customer and supplier. (It is the smallest conductor spacing permissible in places on a finished PCB.



7. Minimum conductor spacing on finished PCB where there is no excess metal at pattern edge.
Calculated from the permissible percent of excess metal

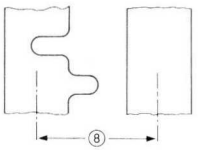
$$7 = \frac{100}{100 - \%\ \text{excess metal}} \times 6$$

When no excess metal is permitted, $7 = 6$.

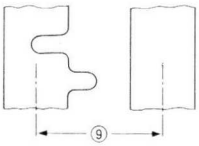


8. Minimum conductor pitch on finished PCB

$8 = 5 + 7$.



9. Nominal conductor pitch on artwork. Calculated from the minus master pattern tolerance on pitch.
$9 = 8 +$ (minus master pattern tolerance on pitch)

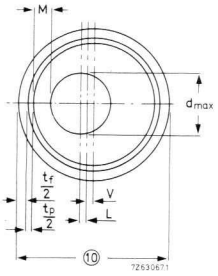


10. Terminal area diameter on artwork.
10 = terminal area diameter as specified in Table *A*2.
If this diameter has to be calculated:

$10 = d_{max} + 2M + t_p + t_f + 2L + 2V$

where

d_{max} = max. diameter of plated-through hole
M = min. distance from hole edge to terminal area edge
V = max. misalignment of pattern
L = tolerance on hole location (see para *A* 5.2)
t_f = photo master tolerance on conductor width and terminal area diameter (see Table *A*2)
t_p = tolerance on conductor width and terminal area diameter (see Table *A*2)



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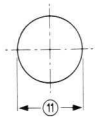
11. Minimum terminal area on finished PCB.
This accounts for the minus master pattern tolerance on conductor width and the specified minus tolerance on conductor width and terminal area diameter.
11 = *10* — (minus master pattern tolerance) — (minus tolerance on width)



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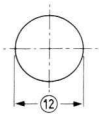
12. Max. terminal area diameter on finished PCB.
Calculated from the master pattern plus tolerance on conductor width and the specified plus tolerance on conductor width and terminal area diameter.
12 = *10* + (plus master pattern tol.) + (plus tolerance on width)



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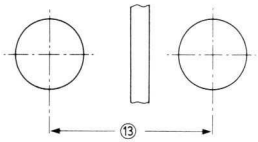
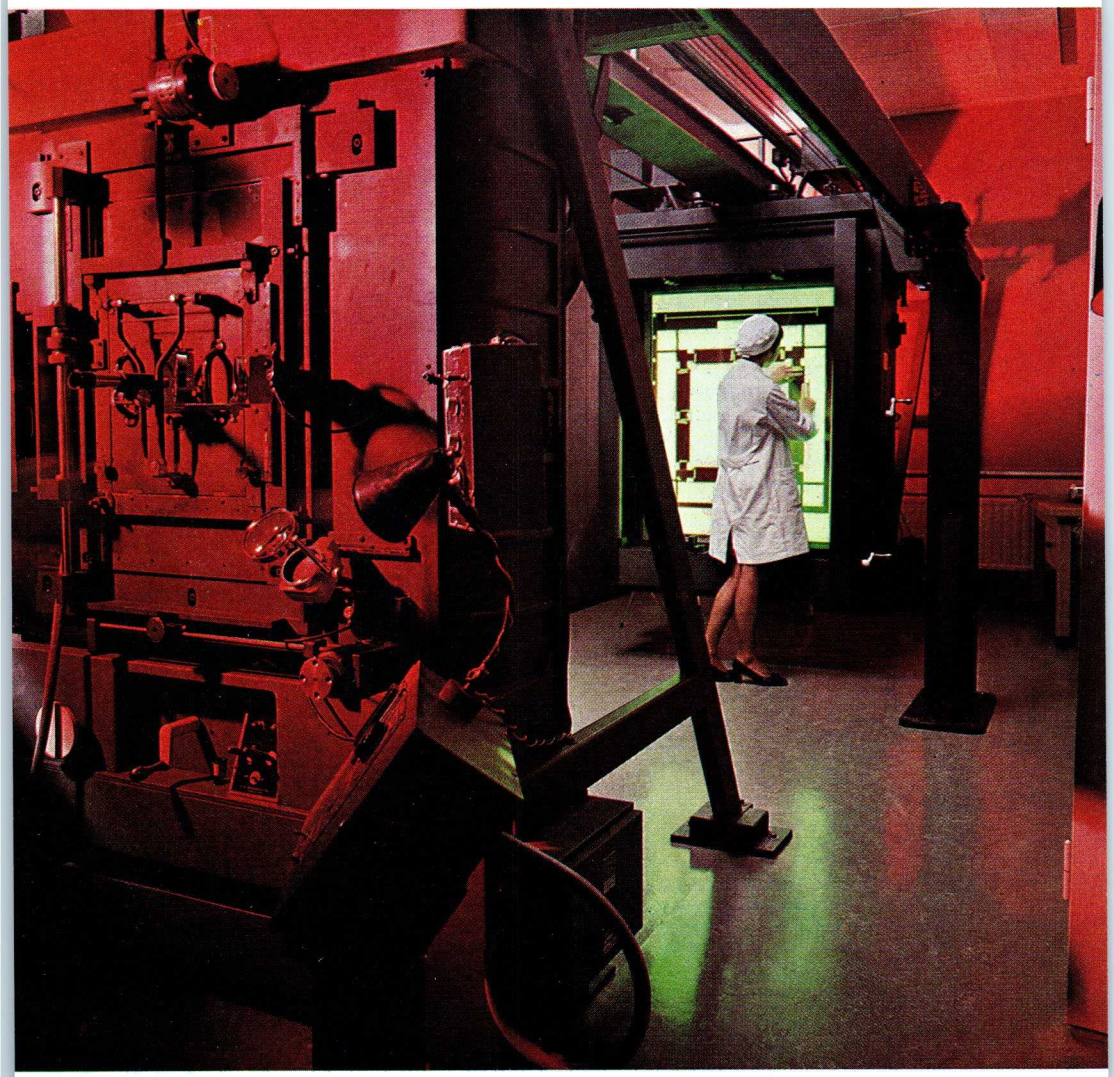
13. Nominal pitch on artwork of two adjacent terminal areas on either side of a conductor. Calculated from the max. terminal area diameter, the min. conductor spacing, the max. conductor width and the master pattern tolerance on the pitch.
13 = *12* + *7* + *5* + *7* + (minus master pattern tolerance on pitch)
In most calculations *6* is used instead of *7*, i.e. there shall be no excess metal in the place where the spacing between the terminal area and the conductor is as its minimum.





Production of photo master by precision reduction on process camera.

4.7 Pattern Configuration

The quality of the PCB, from the aspects of electroplating, solderability of plated holes and flatness, depends on the from of the pattern. The artwork design must satisfy the following rules:

4.7.1 Conductor path and form

(a) On each side of the board the conductor paths should be arranged to run in the same direction as far as possible. On the soldering side, as many of the conductor paths as possible should be arranged to run in the direction that the board moves on the soldering machine, i.e. parallel to the longest board edge.
(b) Corners in the conductors should be made at an angle of approx. 45°
(c) Sharp corners (less than 45°) are not permissible
(d) Conductors should be made as wide as possible, reductions in width being permissible only where absolutely essential.

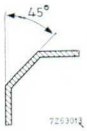


Fig. 4.1. Ideal profile for right angle bend.

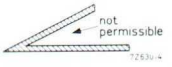


Fig. 4.2. Impermissible acute angle bend.

Fig. 4.3. Reductions in width only where necessary.

4.7.2 Distribution of conductor pattern

(a) The pattern should be distributed as evenly as possible over the the board surface.
(b) The overall pattern surface areas on the two sides of a double-sided board should be made as equal as possible.

To satisfy (a) and (b) additional areas of print can be included in the pattern. These do not form part of the electrical wiring but ensure an even distribution. During the electroplating process they form current distribution aids so that the electroplate is built up in an even manner and isolated areas are protected from "burning".

4.7.3 Configuration of current distribution aids

(a) Current distribution aids, sometimes referred to as "robbers" or "thieves", consist of rasters or grids with a line spacing of approximately 6 mm and a line width of 1 mm. They should be positioned as closely as possible to the other pattern areas, with the specified local conductor spacing taken into consideration, but not less than 1 mm.

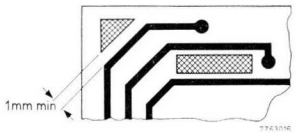


Fig. 4.4. Portion of conductor pattern showing "robbers".

(b) On the soldering side the lines of the grid should lie at an angle of 45° to the direction of movement in the soldering machine, see para 4.7.1 (a).

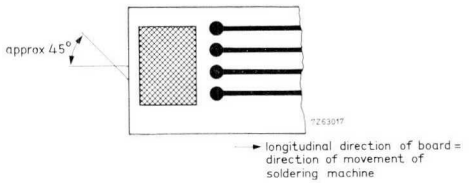


Fig. 4.5. Correct application of "robbers" on soldering side.

(c) A robber of at least 1 mm width should surround the entire pattern. It should be located at the smallest possible distance from the pattern but outside the finished PCB contour.

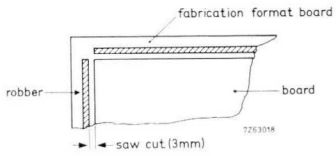


Fig. 4.6. Correct application of "robbers" outside PCB contour.

(d) The robber should not consist of a solid area. This is because, if the robber surface area is large compared with the pattern surface area which is to be shielded, there is a risk of the pattern area acting as a robber. The principle of the current distribution aid is that a smaller surface area shields a larger surface area. Grid spacings other than 6 mm may therefore be needed.

4.7.4. Influence of pattern on solderability of holes

A plated-through hole will possess good solderability when the attached conductor area at the soldering side of the board is larger than that at the component side of the board. This may be achieved in two ways:

(a) By a suitable method of connecting conductors to terminal areas. Two examples are shown in Fig. 4.7.
Where a number of conductor lines extend from the terminal area, they should be arranged on the component side to start at some distance from the terminal area, as shown in Fig. 4.8.

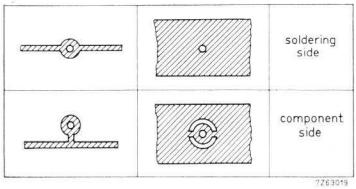


Fig. 4.7. Methods of improving pattern effect on solderability.

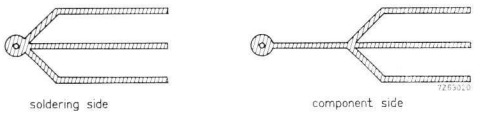


Fig. 4.8. Improving solderability at common terminal point.

(b) By adjusting the size of the terminal area. On the soldering side an isolated hole should be surrounded by a terminal area larger than that on the component side. Alternatively, it should be connected to dummy conductors as indicated in Fig. 4.9.

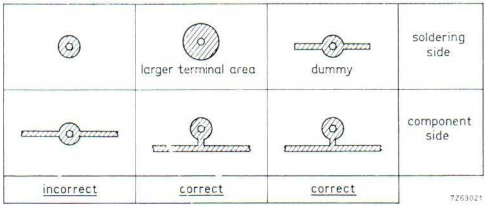


Fig. 4.9. Improving solderability by adjusting terminal area diameters.

4.7.5 Identification marks

Letters, digits and symbols may be reproduced with the pattern. In view of possible overhang they must be of the open type.

Minimum height: 2.5 mm.

Minimum line thickness: 0.4 mm.

4.7.6 Example patterns

A number of example patterns are given in Figs 4.10 through 4.14.

Spotting-out imperfections in photo master.

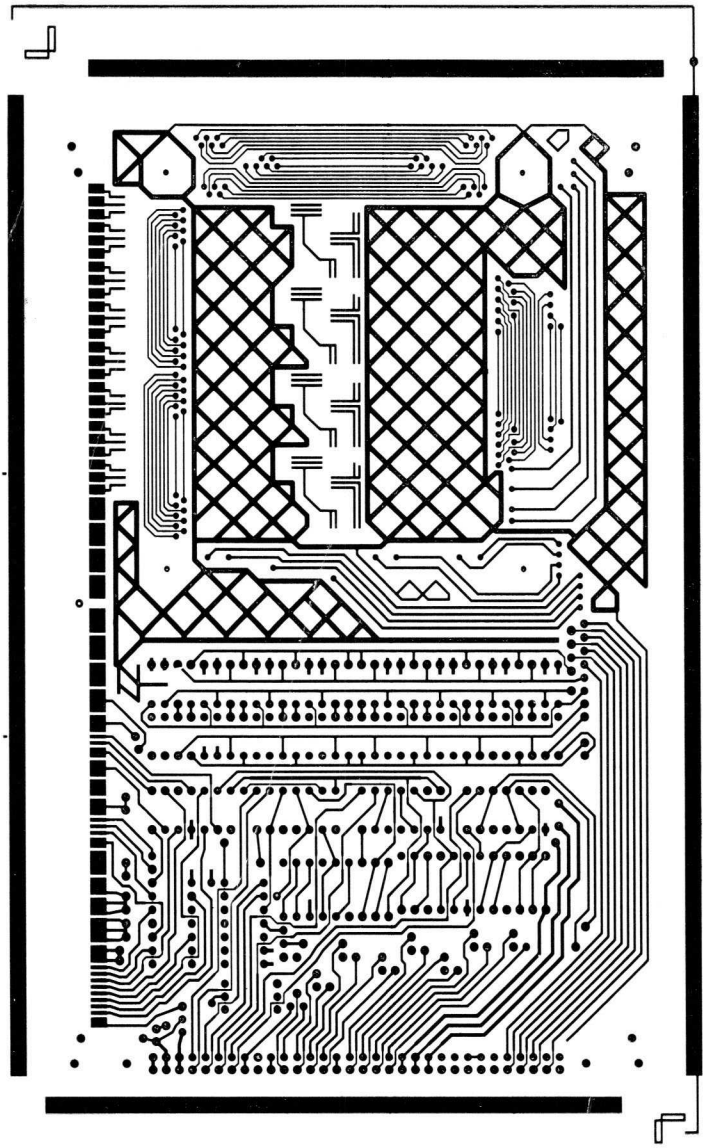


Fig. 4.10. Correct application of "robber".

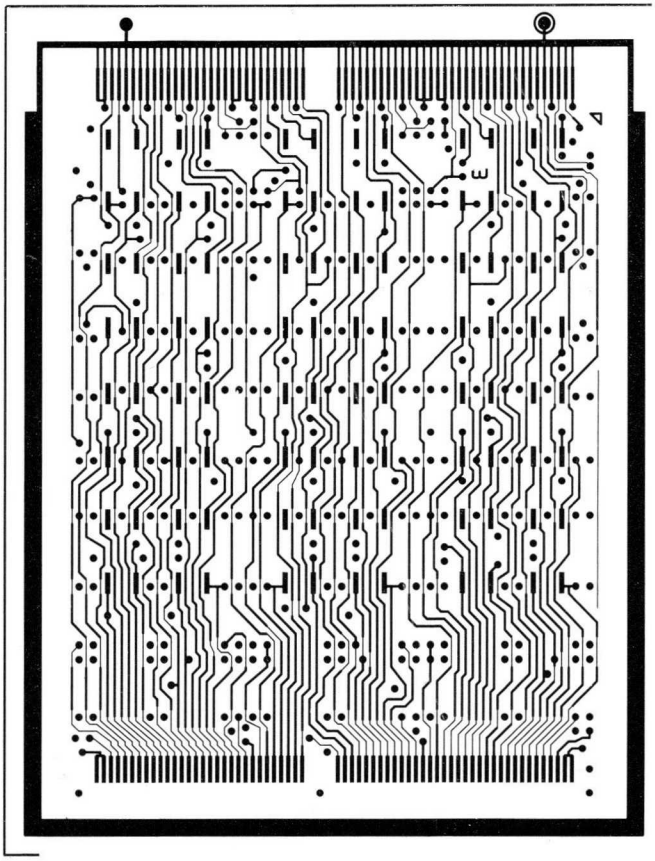


Fig. 4.11. With this even pattern distribution no "robbers" are necessary.

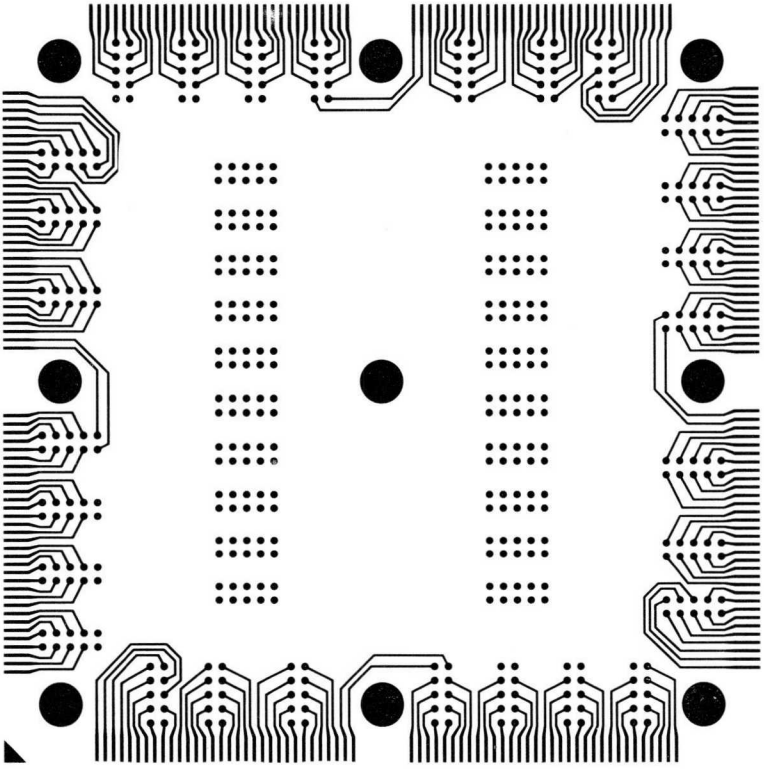


Fig. 4.12. "Robbers" should have been included in this pattern.

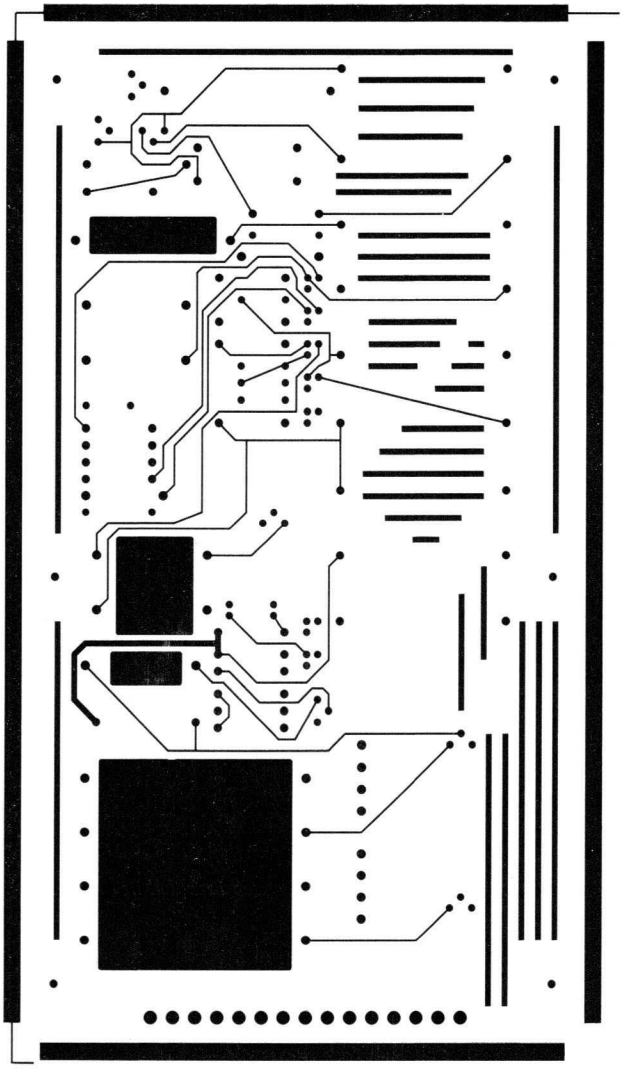


Fig. 4.13. The "robbers" are correctly applied, but their shape is wrong and they should have been rasters. They will present difficulties during soldering.

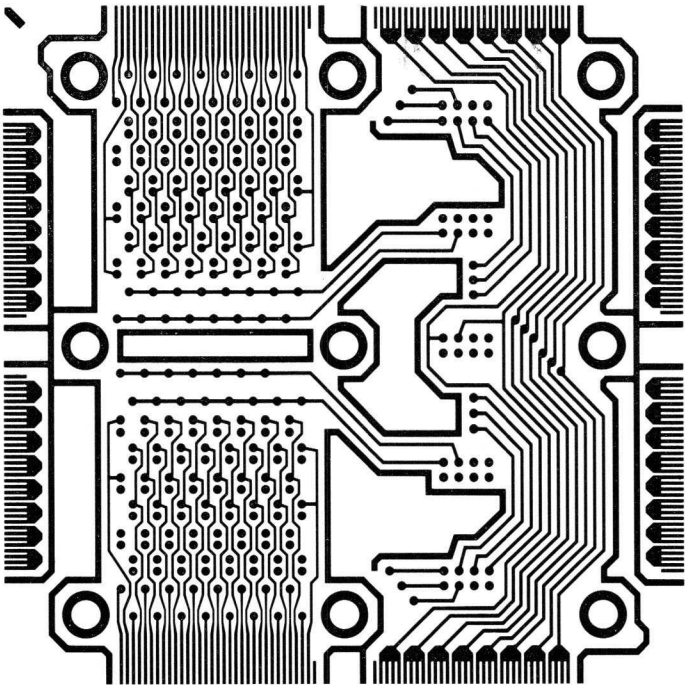


Fig. 4.14. Correct application of "robbers". The bold enclosing line is used as a robber.

4.7.7 Contacts for edge-connectors

Edge-connectors permit PCB's to be exchanged rapidly and easily. They may be of the direct or indirect connecting type.

Direct edge-connector

The female connector receives the edge of the printed board which acts as a plug. For this purpose the board edge must have gold-plated contacts and be specially shaped to fit the female connector. The tolerance on thickness is important. For gold plating see para 6.2.1.

Indirect edge-connector

In this case a multiway plug is soldered to the board. Terminal areas with normal tin-lead plating, are used. No special board shaping is required and dimensions are not critical.

Comparative merits

From the aspect of printing the indirect connector is preferred. Since gold-plated contacts are not needed, the electroplating process is easier. The board dimensions are not critical and there is no special requirement as far as the board thickness is concerned. The direct connector, on the other hand, requires relatively close thickness tolerances to be adhered to. This frequently leads to difficulties and an extra percentage of rejects.

Further, the unavoidable board warpage (see para 2.2.4) may interfere with insertion and good contact. Disadvantages of the indirect connector are that it requires more space than the direct connector, involves the additional cost of the connector and introduces further assembly and testing procedures.

Dimensions

The various types of connectors and the reference numbers of information sheets which specify the appropriate dimensions and tolerances for the PCB edge plug are given on a Survey Sheet, available on request. *

* Survey Sheet, ref. UT-D1181

In the automated fabrication process it is necessary to connect the contacts which have to be gold-plated to an interconnection strip located outside the board contour. This interconnection (see Fig. 4.15) must be shown on the artwork.

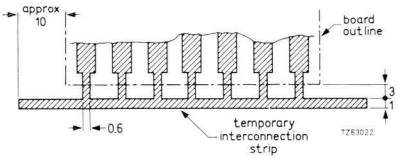


Fig. 4.15. Interconnection strip outside PCB contour for plating-up direct edge-connector.

4.8 Undercut and overhang

4.8.1 Definitions

Undercut

While the excess metal is etched away in the vertical direction, a horizontal etching action takes place along the side of the conductor pattern, below the edges of the resist. The latter causes a reduction in the conductor cross-section. The ratio of the vertical etch (v) to the horizontal etch (x) gives an etch factor which, ordinarily, is 1 : 1, see Fig. 4.16.

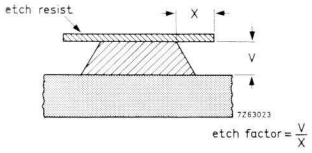


Fig. 4.16. Definition of undercut and etch-factor.

Overhang

This results from overgrowth in the plating build-up. Usually, the plating is thicker than the plating resist and, consequently, the metal grows over the edge of the resist. This causes an increase in conductor width of approximately twice the thickness of the built-up plating, as shown in Fig. 4.17.

The dry photopolymer film technique permits the application of a resist mask whose thickness equals or exceeds the thickness of the electroplating.

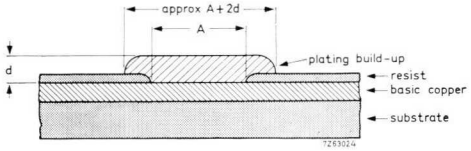


Fig. 4.17. Definition of overhang.

4.8.2 Measurement

Undercut

Undercut can only be measured by metallographic sectioning. In any cross-section the dimension "*A*" (see Fig. 4.18) must not be less than the specified minimum finished board conductor width less twice the undercut (undercut is specified in sub-section *A* 4.4). The minimum finished board conductor width is equal to the corresponding width on the master pattern less the minus tolerance on conductor width.

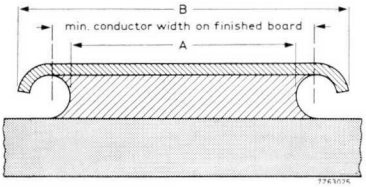


Fig. 4.18. Measurement of undercut and overhang.

Overhang

Dimension "*B*" in Fig. 4.18 must never exceed the corresponding width on the master pattern inclusive of the plus tolerance on conductor width. (see Table *A*2).

5 Plated-through Holes

5.1 Function of Plated-through Hole

5.1.1 Improved component attachment

When the hole is not plated, the strength of the component-to-board joint relies on the adhesive strength between the terminal area and the base material, see Fig. 5.1. This is proportional to the surface area of the terminal area. With high packing densities the terminal areas are, of necessity, small and the adhesive strength is then insufficient to guarantee a reliable attachment.

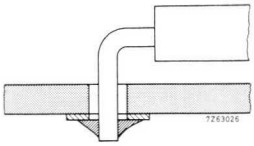


Fig. 5.1. Component attachment with non-plated hole.

When the terminal area is less than 5.5 mm^2, a plated-through hole is recommended, see Fig. 5.2.

Plated-through holes, which are intended solely for improving the component-to-board attachment, should satisfy the solderability requirement quoted in para *A* 7.2.

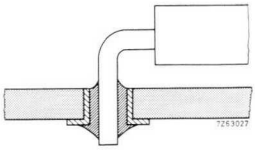


Fig. 5.2. Component attachment with through-hole plating.

5.1.2 Electrical interfacial connection

A plated-through hole may be used to provide electrical connection from one side of a double-sided board to the other, see Fig. 5.3. A reliable connection must be maintained, whether or not a component lead is

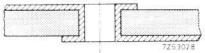


Fig. 5.3. Interfacial connection via plated-through hole.

located in the hole. It must also be maintained after the hole has been subjected to a soldering operation (thermal shock).

Plated-through holes used for electrical interfacial connection must satisfy the following requirements quoted in the Appendix:

Solderability,	para *A* 7.2
Re-soldering,	para *A* 9.1
Continuity,	para *A* 9.2

5.2 Use of Plated-through Holes

5.2.1 In single-sided PCB's

Here the only function of a plated-through hole is to provide a better component attachment, see para 5.1.1. Whatever the base material, the holes must satisfy the solderability requirement quoted in para *A* 7.2.

5.2.2 In double-sided PCB's

Double-sided PCB's made of paper base laminate

Here the only requirement that can be made is for a better component-to-board attachment, i.e. the plated-through holes will only satisfy limited solderability requirements (see para *A* 7.2).

No information is available on the reliability of plated-through holes in paper base boards when used for electrical interfacial connection. With this type of PCB, a guaranteed electrical interfacial connection is only possible via a component lead. The component must thus be placed so that the lead termination can be inspected and is accessible to a soldering iron from the component side of the board, as in Fig. 5.4. This is to allow for the joint to be remade if the solder plug does not entirely

fill the hole. If a component lead termination is not visible and accessible from the component side of the board, use may be made of a parallel hole, as shown in Fig. 5.5. The above methods are not recommended.

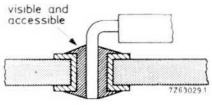


Fig. 5.4. Solder joint visible and accessible.

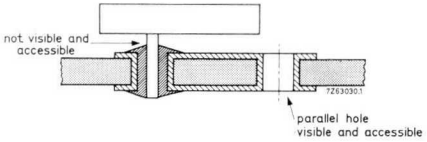


Fig. 5.5. Solder joint hidden by component body. A parallel hole should be provided to allow a faulty interfacial connection to be made good.

Double-sided PCB's made of glass-fabric base laminate

Plated-through holes in glass-fabric laminate boards provide a reliable means of component-to-board attachment and electrical interfacial connection, whether or not a component lead termination is located in the hole.

The holes must satisfy the following requirements given in the Appendix:

Solderability,	para *A* 7.2
Re-soldering,	para *A* 9.1
Continuity,	para *A* 9.2

In the Appendix, the plated-through hole reliability is indicated by the statement that the number of failures shall not exceed 1 in 100,000 (see also para *A* 5.3.3).

A defective plated-through hole which fails to provide electrical interfacial connection after the component has been soldered to the board can be repaired if the component lead termination is visible and accessible from the component side of the board.

5.3 Inspection of the Plated-through Holes

Three tests are called for in the Appendix to be carried out on plated-through holes.

5.3.1 Solderability test

The solderability of the tin-lead plating specified in the Appendix is guaranteed. However, simply using a coating of assured solderability does not necessarily imply that the hole will also possess good solderability. This is because other factors, such as pattern, (para 4.6.4) component lead terminations (see NLN-D 1119), the flux used and the methods of mounting and soldering may have individual or combined influences on solderability. During fabrication, the solderability of the tin-lead coating is checked at regular intervals by means of special test panels. These will reveal deviations from the required solderability which are so small that they cannot be detected on the boards in the pre-delivery inspection.

Before delivery, each batch of PCB's is subjected to a 1 % random test (the minimum sample being 1 board). In this test the sample boards, which have no component lead terminations located in the holes, are dip-soldered under defined conditions. Evaluation of the test results is based on experience as the influence on solderability by the pattern and the hole diameter is unspecified.

In the event of a difference of opinion between user and supplier, a solderability test is performed, as mentioned in para 5.2 of IEC-52/WG4 (secr. 25), to exclude the influence of the pattern (see also para *A* 7.3). The result of this test shall decide the issue.

5.3.2 Re-soldering test

This applies to plated-through holes in glass fabric laminate boards. The test is performed in accordance with para *A* 9.1. The result, however, depends significantly on the person who performs the test. As a rule, holes that satisfy the continuity test, which follows, also satisfy a re-soldering test that is performed correctly.

5.3.3 Continuity

The purpose of the continuity test quoted in para *A* 9.2 is to check the electrical interfacial connection provided by the plated-through hole. Apart from mechanical vibration and shocks, the severest condition which a plated-through hole has to withstand is the thermal shock during soldering. (Vibration and shock tests are not given in our specification. Where necessary, they are arranged by agreement between user and supplier.)

As the base material and the hole plating have different coefficients of expansion, a thermal shock may produce cracks in the hole plating. When proper fabrication methods are employed and the correct base material is used, the hole wall plating must not show any cracks after having been subjected to a thermal shock. A limited change in the Ohmic resistance of the hole plating is permissible (see *A* 9.2).

The continuity test is performed as a process control test with special test panels having at least 100 holes connected in series. The test panels are subjected to 10 thermal shocks. Experience has shown that holes which are still satisfactory after 1 thermal shock, remain satisfactory after 10 thermal shocks.

Without making any definitive conclusions regarding service life, it may be assumed that holes which survive the continuity test will not fail during normal service.

In sub-section *A* 9.3 an indication of plated-through hole reliability can be inferred from the statement that the number of failures in a continuity test shall not exceed 1 in 100,000. This indication cannot be quoted as a guarantee since insufficient statistical evidence is available. An additional difficulty lies in the fact that such a guarantee would still apply after the user had performed a soldering operation, outside the supplier's control.

During fabrication, a routine inspection of a large number of holes is carried out. The results give support to the above indication of plated-through hole reliability and are available to the user. To illustrate some of the points made earlier, the expansion coefficients which affect the thickness of some base materials are listed in Table 5.1 for comparison against the expansion coefficient of copper.

The table reveals the large difference in expansion coefficient between paper base laminate and copper. This will cause considerable stresses in the event of a thermal shock and is one of the reasons why maximum reliability requirements can not be made on boards made from paper base laminates.

Table 5.1 Expansion coefficients of base materials versus copper

mean coefficient of linear thermal expansion $\times 10^{-5}$mm/mm (°C) for 0-60 °C				
copper	glass fabric	paper base XXXP	XXXPC	paper base epoxy
1.7	6	10	20	10

5.4 Mounting Recommendations

- The plated-through hole diameter may not exceed the diameter of the component lead by more than 0.4 mm. This applies to both single and double-sided PCB's.
- The component lead terminations may not be bent at the soldering side.
- The leads may extent beyond the surface of the circuitry (see dimension "*a*" in Fig. 5.6) by a minimum of 0.8 mm and a maximum of 1.1 mm.
- Boards with plated-through holes may be dried at 105 (+5-0) °C for at least 3 hours, prior to soldering. Mounting and processing must take place within 3 days after drying.

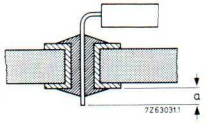
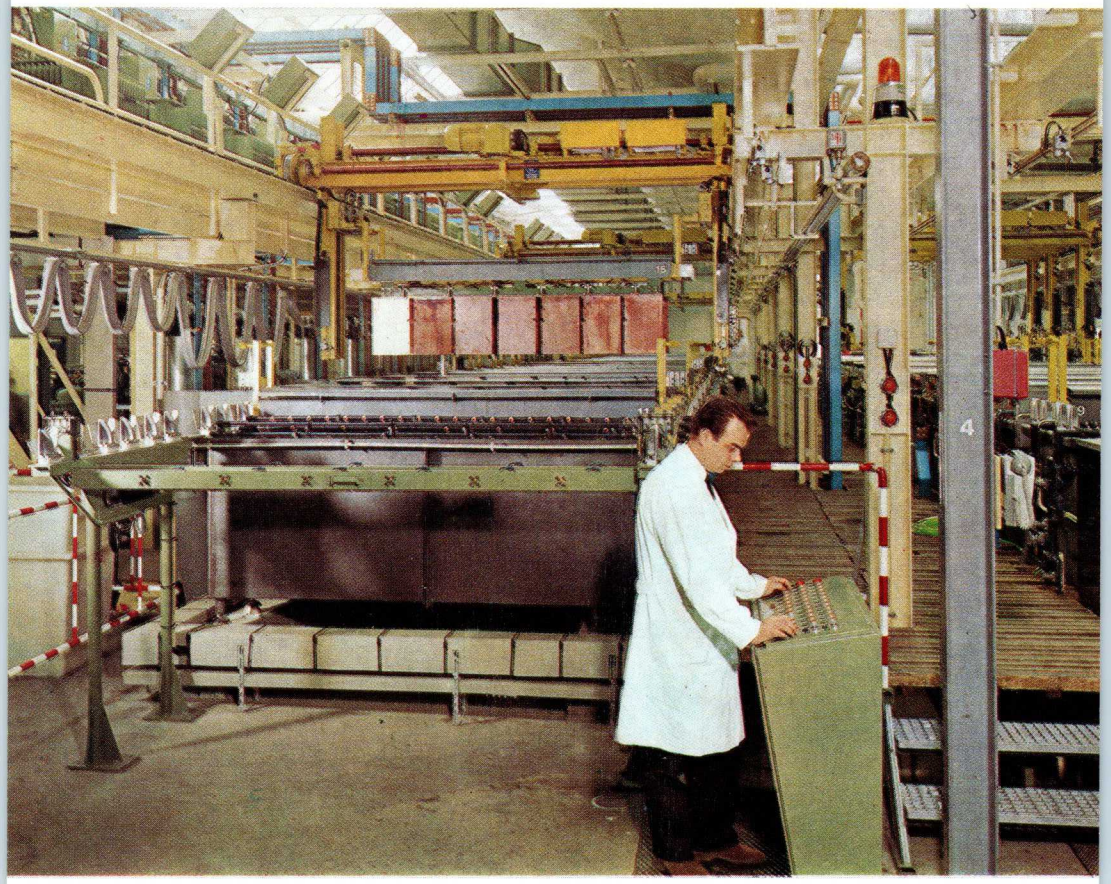
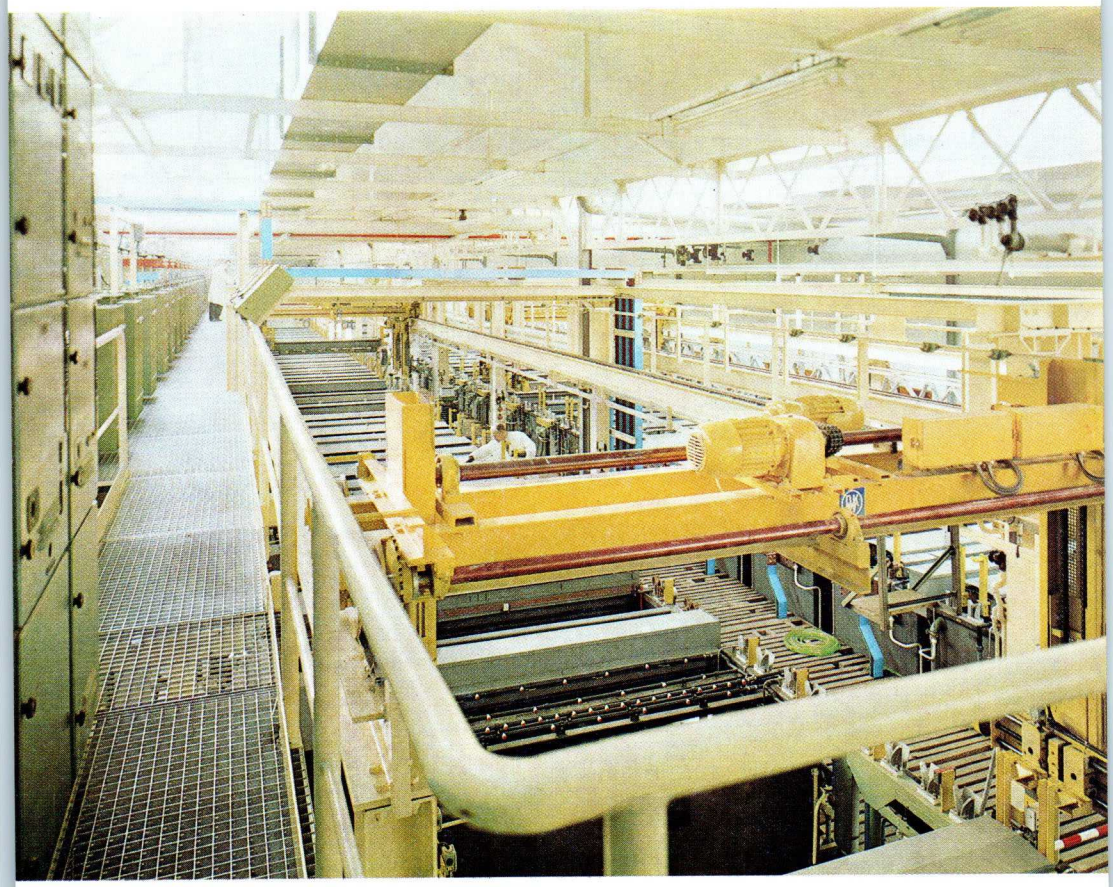


Fig. 5.6. Extension of component lead beyond PCB surface.



Part of the automatic plating installation showing process control console.



General view of automatic plating installation.

6 Coatings and After-Treatments

6.1 Introduction

Brief details are given in this section of the metal plating methods which we employ for PCB's. Mention is also made of some plating methods which we have evaluated but have not used for various reasons. After-treatments and the properties and uses of protective organic coatings are also mentioned.

6.2 Electroplating

A variety of metallic deposits are available for printed circuit applications, and it is important to select the most suitable. The properties which have to be considered are as follows:

Mechanical: hardness, resistance to wear, ductility.
Electrical: electrical conductivity, contact resistance.
Physical: thermal conductivity, solderability.
Chemical: corrosion resistance.
Cost considerations: relating to the metal itself and also to bath preparation and control.

The properties of the more popular plating metals are described in the following paragraphs. Those which we employ are listed in 6.2.1. Those which we have not adopted but which are nevertheless in widespread use are given in 6.2.2 for comparison.

6.2.1 Approved plating metals

Copper

Copper possesses a number of properties which make it eminently suitable for PCB applications. For example, it provides good electrical and thermal conductivity, good ductility and relative ease of cleaning, pickling and etching. It will readily accept further plating. The latter is required on the walls of the board holes which have to be plated-through, where an approximately 20 μm copper layer is required. The plating thickness depends on the "throwing power" of the bath. By "throwing power" is

meant the ability to plate a more or less uniformly thick deposit on an irregularly shaped surface. Various plating baths are used, and of these we employ sulphate copper and pyrophosphate copper. The baths possess certain qualities which indicate their use for differing applications.

The pyrophosphate copper bath has a better throwing power than the sulphate copper bath and therefore is more suitable for miniature PCB's where the tolerances on hole diameter, terminal area diameter, and conductor width are closer. However, it requires more careful inspection and control than the sulphate copper bath.

The sulphate copper bath produces a thick deposit at a deposition rate higher than that of the pyrophosphate copper bath.

Another important consideration is the relative hardness. This is expressed in units based on the Vickers Pyramidal Number System. Pyrocopper has a hardness of 150-200 Vickers. Sulphate copper normally has a hardness of approx. 70 Vickers, but this can be increased to approx. 150 Vickers by the use of addition agents. These raise the levelling power, or the ability to deposit in recessed areas (scratches, etc.) to give a smoother, harder surface.

Nickel

The hardness and wear resistance of nickel make it a very suitable undercoat for gold plated edge-connectors. When the boards require nickel and gold plating in the contact area and a tin-lead finish in the other areas the nickel undercoat can be applied overall.

For most applications, a nickel layer of approximately 6 μm will suffice. For special applications this is sometimes increased to approximately 10 μm. Depending on the requirements for wear resistance and hardness of the nickel layer, addition agents may be included in the plating solution. The following orders of hardness can then be obtained: 200 Vickers with matt nickel solutions; 300 to 400 Vickers with semi-bright nickel solutions; 500 to 600 Vickers with bright nickel solutions.

Gold

The very high corrosion and wear resistance, excellent conductivity and low contact resistance of gold make it the most frequent choice as a finish on switching or contact areas. For normal applications, gold is deposited on nickel to a thickness of approximately 2.5 μm. This, however, does not guarantee a completely impervious surface. Hence, for certain industrial

applications (i.e. sulphur dioxide atmosphere), a thicker and virtually pore-free deposit of 5 μm is used. A nickel undercoat is not used in such cases since it is severely attacked by this type of environment.

Tin-lead

Tin-lead is a soft, ductile, and solderable alloy which can be electroplated in a tin-lead ratio close to the eutectic (63/37) composition. The plating thickness can vary as required from 5 to 50 μm. From the aspect of soldering, a thin layer provides the best heat transfer.

Since our fabrication process utilises the tin-lead plate as an etch resist, a minimum layer thickness of 6 μm must be applied in the holes. With our present tin-lead plating baths, a plate of at least 15 μm is deposited on the surface. This is sufficient to withstand the specified humidity and ageing tests. In the fabrication process, thinner layers are preferred because they enable the specified conductor widths and spacings to be adhered to more accurately. However, where components or leads have to be soldered to the board without the addition of tin-lead solder (i.e. by the reflow soldering method), the specified conductor width and lead diameter and the desired shape of the solder joint may require a thicker layer of 20, or 25 μm (with a tolerance of +100%).

6.2.2 Other commonly used plating metals

Tin

In recent years, tin, electro-deposited from a bright acid solution, has found wide acceptance for printed circuit applications for the following reasons:

- it gives excellent solderability
- sodium hydroxide treatment and/or cleaning after etching in a chromic acid and sulphuric acid solution is not required.
- control of the plating bath is relatively simple.
- the throwing power of the bright tin plating bath is better than that of existing tin-lead baths.

Tin-nickel

Tin-nickel alloy, deposited in a tin-to-nickel ratio of 65/35, possesses great hardness and good wear resistance and is therefore used as a finish in

switching and contact areas. It can also be used as an alternative finish to tin-lead. As an etch resist, tin-nickel is as good as tin-lead, but it compares less favourably when used as a solderable finish.

A useful advantage is that, when contacts are to be gold-plated, the gold can be deposited directly onto the tin-nickel without the need for etching and then re-depositing a nickel undercoat, see Figs. 6.1 and 6.2.

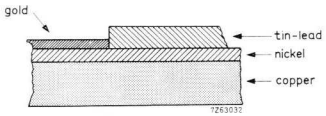


Fig. 6.1. Gold and tin-lead combination on a nickel undercoat.

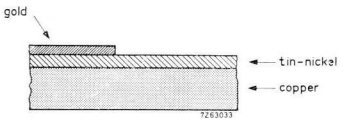


Fig. 6.2. Tin-nickel overall with gold in contact areas.

Tin-nickel plate with gold flash

If a gold flash of approximately 0.1 μ thickness is deposited on the tin-nickel plate, the solderability is ensured for a long period of time. A thicker gold plate may be deposited on the switching areas if required, see Fig. 6.3.

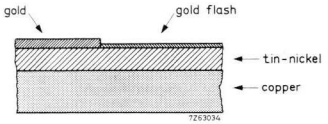


Fig. 6.3. As in 6.2. but with gold-flash overall.

6.3 Plating other than by Electro-Deposition

6.3.1 Approved method

Copper

From a solution containing cupric sulphate, copper is deposited by reduction on a carefully pre-treated conductive or non-conductive surface. This type of deposit provides an excellent basis for electrical interfacial connections in double-sided PCB's. It will also provide for better component attachment on single and double-sided PCB's made by subtractive, additive, or semi-additive methods.

An electroless-plated copper layer of approximately 0.1 to 2 μm offers excellent electrical characteristics and good heat conductivity. An additional factor which favours its use is that we have a particularly well-controlled process for electroless-plating of ductile copper.

6.3.2 Other commonly used methods

Nickel

Nickel can be deposited on conductive and non-conductive surfaces by reduction from a warm solution. Unfortunately it will nearly always contain a high phosphor content (5-14%) and its electrical conductivity is consequently poor.

Tin

(a) Immersion tinning

Tin can be electroless-plated on copper and tin lead surfaces by immersion in a tin salt solution. This will produce a maximum layer thickness of approx. 0.5 μm. As a finish on copper and tin-lead it possesses good solderability but only for a short period of time. As an etch resist on copper it is not satisfactory.

(b) Roller coating

Prepared copper surfaces can be coated with tin by means of a roller rotating in a bath of molten tin. This method produces a surface of excellent solderability but a disadvantage is that layer thickness varies from a few μm to, locally, some hundreds of μm.

The roller coating method is unsuitable for PCB's with plated-through holes as some holes are not wetted while other are filled in.

Tin-lead

The roller-coating method is also employed to provide a coating of tin-lead (60/40). The advantages and disadvantages are as stated for roller-coated tin.

Gold

Gold in its pure form can be electroless-plated on metal substrates such as copper, nickel, and nickel alloys. The electroless-plating method is used almost exclusively when very thin gold plates of, say, 0.1 μm are required. For thicker layers, electroplating is employed.

6.4 After-treatment of Metallic Coatings

6.4.1 Re-flow

This is a process, applied to electroplated tin-lead, where the plating is momentarily melted. The necessary heat can be applied by conduction (e.g. immersion in a heated liquid), by convection (e.g. passing a heated gas over the heated board), by radiation (e.g. infra-red radiation), or by a combination of these.

Any tin-lead overhang resulting from the electroplating and/or etching operation is removed by the re-flow operation and thus a better pattern definition is obtained. The re-flow operation produces a denser and smoother metallic coating and improves its solderability. A disadvantage is that with miniature PCB's, contraction of the molten solder may cause hole filling. This restricts the applications of the re-flow method.

6.4.2 Hydrosqueegee

A liquid heated to approximately 220 °C is sprayed with force onto boards which have previously been tin-lead plated. This melts the tin-lead and removes the excess quantity so that only a very thin film of 1 to 2 μm is left. Boards which are to be given the hydrosqueegee treatment are solder plated by an electroless method, or possibly dip or wave-soldered, so that the holes are completely filled with solder. The treatment eliminates the solder overhang which results from electroplating

and/or etching so that a better pattern definition is obtained. The solderability is improved because a smoother and thinner tin-lead layer is formed. Experiences, concerning the solderability after a prolonged period of time or after humidity tests, vary from good to bad. We are currently evaluating the hydrosqueegee method and the results will be published in due course.

6.5 Organic Coatings

6.5.1 Temporary protective coating on copper

Cleaned, photo-etched boards may be given an organic coating of colophony resin as a temporary protection for the copper against oxidation, finger prints, etc. The resin is dissolved in white spirit and applied by spraying. After drying, a tack-free resin layer is obtained which can act as a flux during soldering. After soldering, it may either be retained or removed by means of an organic solvent.

6.5.2 Permanent protective coating, insulating coating or solder resist on copper and tin-lead

A permanent protective organic lacquer coating is applied to the board by a screen-printing process. It is arranged to cover the entire surface, apart from the terminal and contact areas, and is applied before the components are mounted. It is removed only in the event of repairs to the printed circuitry being needed. The function of the coating is to protect the conductors and the conductor spacings from environmental contamination. Without a protective coating, the conductor spacings would be contaminated to an indefinable degree, with a possible deterioration of the tracking resistance. This could create difficulties, particularly with miniaturized boards.

On the soldering side of the board, the lacquer coating acts as a solder resist i.e. during dip and wave soldering the base material and metal covered by the lacquer do not come into contact with the solder. Thus there is no risk of solder-bridging when the conductor spacings are small and there is less tin-lead consumption in the bath. Properties sought for in an insulating coating are:

- ease of application
- electrical characteristics close to those of the base materials (to ensure the combined properties are not worse than those of the base material alone)
- a low curing temperature
- non-porous, and non-corrosive
- resistant to thermal shock, moisture, and solvents
- removable to permit repairs.

Lacquers which meet these requirements usually consist of two constituents, the base being an epoxy, polyamide, polymethane, silicone, or polystyrene resin.

We test the suitability of a lacquer by means of a specially designed test panel. This is illustrated in Fig. 9.3.6.

We have found one of the epoxy-polyamide types satisfactory for coating both copper and tin-lead plating on the soldering side of the board. A lacquer coating which acts as a solder resist, must not exhibit deformation, cracks or blisters during the soldering process. In this respect the epoxy-polyamide resin lacquer has proved satisfactory as a solder resist on a copper surface.

Tin-lead electroplate under the lacquer may melt during the soldering process and thus tend to contract in places. This may cause deformation and damage in various places of the lacquer mask.

An investigation is being carried out to find a lacquer which is fully satisfactory as a solder resist on electroplated tin-lead.

7 Solderability

7.1 Terms and Definitions

Solderability is the ability of a metal to be wetted by solder (wetting).

Dewetting is a condition where the solder, having wetted the metal, contracts before solidification leaving a thin, dull solder film in places.

Nonwetting is a condition where a metal surface has contacted molten solder, but none has adhered to it.

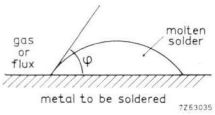


Fig. 7.1. Soldering contact angle.

A criterion for the solderability of a metal is the contact angle φ formed by

1. molten solder,
2. metal to be soldered,
3. air, protective gas or flux, after thermodynamic equilibrium has been reached.

In practice, angle φ will not approach zero, because thermodynamic equilibrium is not attained during soldering. Normally the soldering time is too short, the molten solder having solidified before equilibrium is attained. This is particularly so with plated-through holes, where the temperature falls rapidly below the solder solidification point due to such factors as pattern effects, metal layer thickness and applied flux quantities.

The criteria for wetting and dewetting agreed upon in practice are:

$\varphi < 75°$: wetting
$75° < \varphi < 180°$: dewetting

7.2 Solderability of Metal Finishes on PCB's

Our PCB's have copper, tin-lead and/or gold plated finishes. Where the solderability requirements are most stringent, tin-lead is recommended for PCB's with plated-through holes and tin-lead or copper for those with non-plated holes.

7.2.1 TIN-LEAD

Solderability

The solderability of electroplated tin-lead, in plated-through holes and on surfaces, is guaranteed for 6 months after the date of delivery, provided that the PCB's are stored in a room that satisfies the ambient conditions specified in IEC publication no. 68, namely:

- temperature between +15 °C and +35 °C.
- relative humidity between 45% and 75%.
- atmospheric pressure between 860 and 1060 mbar.

Electroplated tin-lead, subjected to a reflow process or a hydrosqueegee process will exhibit enhanced solderability. This is because the surface is smoother and hence less oxides have to be eliminated during soldering. In addition, the hydroqueegee process provides a thinner tin-lead layer, which also has a favourable effect on soldering. However, both methods are subject to certain restrictions (see paras 6.4.1 and 6.4.2).

Solderability test (see also para 5.3.1)

(a) *IEC solderability test.* The solderability of a batch is tested as per IEC-proposal 52/WG4 (secr.) 25. In this test the solderability of both the conductor surface and the holes is checked. However, prior to the solderability test on the holes, the board is processed to eliminate the pattern effect on the solderability of the holes. This consists of removing or interrupting the conductors to the terminal areas on the component side. It is justified since it is not the solderability of a certain pattern that is guaranteed (see para 4.8.4), but the solderability of the tin-lead deposited on the conductor surface and in the plated-through holes. The test is carried out with the aid of a Solderability Test Machine. The test may be briefly described as follows. The board under test (measuring 30×30 mm) is dried for one hour at a temperature of 105(+5-0)°C and then coated

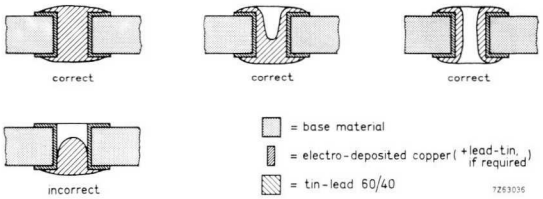


Fig. 7.2. Wetting of plated-through holes.

with activated flux (a non-activated flux is used only at the request of and by agreement with the customer). It is next suspended over a solder bath containing 60/40 tin-lead at 235 °C and arranged to contact the solder for a pre-set period.

To pass the test the following requirements must be satisfied:

- The metal surface and the holes must be properly wetted with solder within 3 seconds *.
- Within 5 seconds no dewetting or other imperfections may occur which are in excess of those illustrated as "acceptable" in IPC-A-600. This requirement is described by IEC as follows:
  "The soldered areas shall be covered with a smooth and bright solder coating showing not more than traces (approximately 5 %) of scattered imperfections such as small pinholes, unwetted or dewetted areas. These imperfections shall not be concentrated in one area".

(b) *Process control with the aid of special test panels.* Daily tests are made on the copper and tin-lead plating baths where special test panels are put through the plating processes. After final processing these panels are soldered. The panels contain 100 holes which exhibit different degrees of processing difficulty, the degree varying from "very simple" to "very difficult" (see para 9.3.1). The daily number of poorly soldered holes (which invariably are the holes possessing a high degree of processing difficulty) are counted and recorded. If, over a couple of days, the number of poorly soldered holes varies, indicating a variation in the fabrication process, action will be taken to improve the solderability. This always applies although the requirement of the solderability test may still be amply satisfied.

* This means that the holes shall be or shall have been filled completely with solder as shown in Fig. 7.2.

7.2.2 Copper

Copper without a protective coating

Electroplated copper initially possesses a very high solderability, comparable to that of tin-lead 60/40. After storage its solderability is reduced, unless an activated flux is used. A treatment in a solution of chromic and sulphuric acids will restore the solderability for a longer period.

Copper with a protective coating

The method we employ to protect the copper of, so-called, "photo-etch" boards against oxidation and finger prints, is to spray a solution of polymethacrylate resin and colophony over them. Immediately after spraying-satisfactory wetting to the copper under the coating will be obtained. After 6 months storage the solderability of the PCB's will have deteriorated slightly but still remains satisfactory.

7.2.3 Gold

Electroplated

Newly deposited gold of a normal 2.5 μm thickness possesses excellent solderability. After storage this will deteriorate slightly. The solderability of bright gold is generally less than that of matt gold. Gold diffuses very easily in a tin-lead solder, especially at high temperatures, which may result in brittle soldered joints.

Electroless-deposited

The solderability is less than that of electroplated gold and deteriorates with time.

7.2.4 Tin

Electroplated

When deposited in an acid bright dip, tin possesses excellent solderability, comparable to tin-lead. After storage or life tests the solderability remains satisfactory.

Hot tinning (roller coating)

Hot tinned PCB's possess excellent solderability. Slight deterioration occurs after long periods of storage.

Electroless-deposited

When newly deposited on copper, tin possesses good solderability. This deteriorates rapidly with time.

7.2.5 Nickel

Both electroless-deposited and electroplated nickel possess good solderability but only for a short period of time. Hence, nickel is not suitable as a finish on boards which must retain their solderability.

7.2.6 Tin-nickel

Electroplated tin-nickel possesses better solderability than pure nickel. However, the solderability is far less than that of tin-lead, no matter whether newly deposited or after storage.

7.2.7 Tin-nickel with a thin gold layer

Tin-nickel with an electroplated gold layer of approx. 0.1 μm possesses excellent solderability which is comparable to that of tin-lead, even after storage.

8 Conductor Width and Conductor Spacing Related To Electrical Requirements

8.1 Conductor Width

The top section of the graph Fig. 8.1 represents the relationship between the current through a conductor of a given cross-section and the resultant temperature rise in the conductor. The bottom section provides a means for relating the conductor cross-section to the conductor width of the master pattern (scale 1 : 1) according to the thickness of the basic copper. The sum of the maximum ambient board temperature and the permissible temperature rise resulting from the current flow, must not exceed the maximum permissible operating temperature of the base material, as quoted in the material specification. The values are derived on the basis of a 35 μm copper foil thickness.

The cross-section of a finished PCB conductor will, of course, be greater than the cross-section based on a 35 μm thickness of the basic copper, due to the plating. The total reduction in cross-section, due to conductor width tolerance and undercut, is always less than the increase in cross-section due to plating. Thus there is no need to apply a correction to the conductor width given in Fig. 8.1.

8.2 Conductor Spacing

8.2.1 General

The specified conductor spacing is the minimum distance between two conductors as measured on the base material. The required conductor spacing depends on:

- the potential difference between current carrying parts (operating voltage)
- the limit voltage and the limit-to-operating voltage ratio
- the possibility of the occurrence of peak voltages
- the tracking resistance of the insulating material (IEC publ. 112)
- whether or not the circuit is directly connected to the mains
- the environmental conditions affecting the board, i.e. dust and moisture
- whether or not the pattern is coated with insulating lacquer.

Specifying the minimum possible conductor spacing is a difficult matter when non-coated boards are to be used in equipment where dust and moisture conditions are not defined. In such cases it is recommended that the minimum conductor spacings should only be taken as a guide. Larger spacings should be used wherever possible.

8.2.2 Calculating minimum conductor spacing

In the graphs Figs. 8.2 and 8.3 the conductor spacings versus the operating voltages are plotted in acordance with the following specifications:

(a) *MIL - STD - 275C "Printed wiring for electronic equipment"*

The continuous lines of the graph in Fig. 8.2 represent the conductor spacings specified in the above MIL-standard. The applicable maximum voltage rating is 1000 V d.c. or a.c. peak.

(b) *IEC publication 326 "General requirements and measuring methods for printed wiring boards"*

The dashed lines of the graph, in Fig. 8.2 represent the conductor spacings specified in the above IEC publication. The applicable maximum voltage rating d.c. or a.c. r.m.s. is:
$3\times$ operating voltage or 500 V whichever is greater, when operating voltage $\leqslant$ 1000 V.
$1.5\times$ operating voltage or 3000 V whichever is greater, when operating voltage $>$ 1000 V.

(c) *IEC publ.-28 (secretariat) 54 "Preliminary draft recommendation on insulation coordination of low-voltage equipment"*

The curve of the graph in Fig. 8.3 represents the conductor spacings specified in the above publication. The maximum voltage rating is as quoted in our specifications (see Appendix) viz. 700 Volts (peak), 50 Hz. Fig. 8.3 is based on insulation category *A* where the creepage distance is $a + b$ according to table 4 of document 28 (secretariat) 54.

Category A (conditions)

contamination	humidity	mildew	effects of short-circuits in case of insulation failure	stress due to over voltage
hardly noticeable	normal	nil	slight	slight (if applicable protective measures are taken)

Inspection of conductor pattern.

8.2.3 Explanatory notes on the graphs figs. 8.2 and 8.3

The graph Fig. 8.2 shows curves for both MIL and IEC conductor spacings on non-coated boards at altitudes up to 3 km and on coated boards at any altitude. Both the MIL Std and the IEC publication specify a minimum conductor spacing of 0.635 mm on non-coated boards and 0.25 mm on boards coated with insulating lacquer.

Where lack of space on non-coated boards makes a conductor spacing of less than 0.635 mm unavoidable, the MIL Std and the IEC publication require a change-over to boards coated with insulating lacquer. However, coating with insulating lacquer introduces a number of problems, as mentioned in para 6.5.2. In practice non-coated boards with conductor spacings of less than 0.635 mm have been widely used for some time, even though a generally accepted standard is not in existence for boards of this description.

Philips' standard NLN-D97 "Air and creepage Paths" quotes creepage paths up to 0.3 mm in group I, section "No danger" but group I is based on circuits fully protected from dust and moisture and this situation can be obtained only in expensive fully-enclosed equipment. An IEC Standard for conductor spacings of less than 0.635 mm on non-coated boards is in preparation, a proposal having been initiated by Committee 28 (Secretariat) 54.

The graph Fig. 8.3 shows the conductor spacings and voltages mentioned in this proposal. It is recommended that these be adhered to for non-coated boards with conductor spacings of less than 0.635 mm unless there are measurements available which offer an alternative.

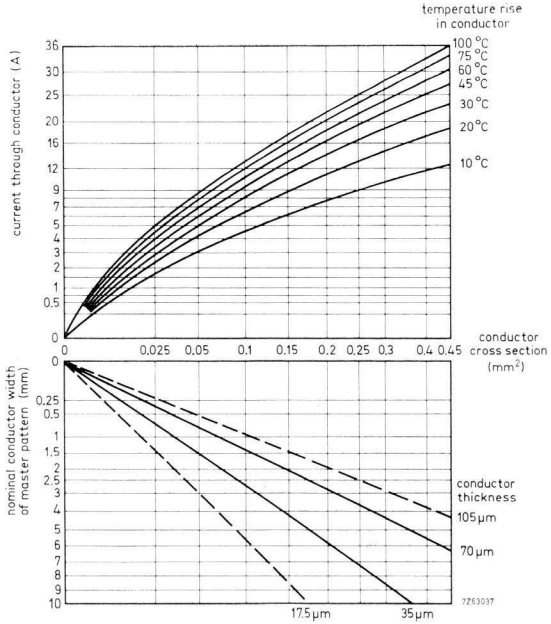


Fig. 8.1. Temperature rise as a function of current through a conductor of given cross-section (upper). Corresponding conductor widths with a given thickness of basic copper (lower).

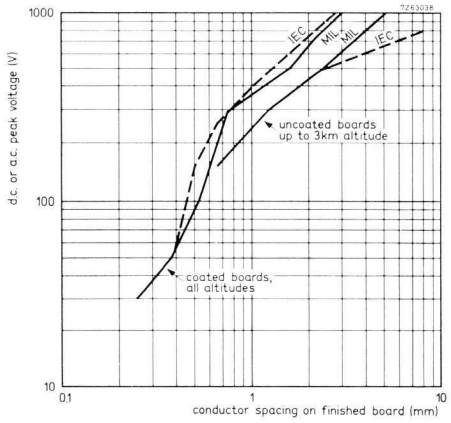


Fig. 8.2. Minimum conductor spacing versus peak operating voltage. The broken line indicates where the IEC publication deviates from MIL spec.

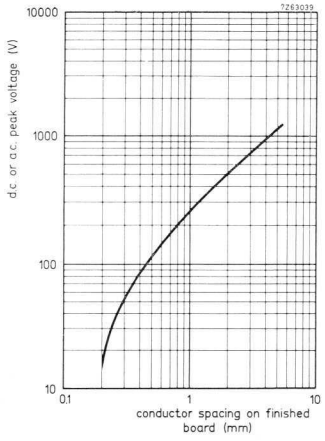


Fig. 8.3. Proposed minimum conductor spacing for noncoated PCB's according to IEC.

9 Test, Operating Conditions, Delivery and Test Boards

9.1 Tests and Operating Conditions

The requirements to be satisfied by PCB's are as stated in the Appendix *A*3 through *A*9. The conditions under which PCB's satisfy these requirements are stated in para *A*2.2. These conditions relate to safe combinations of temperature range and relative humidity.

To establish whether the PCB's satisfy the requirements under these conditions, specimens are subjected to a number of tests as listed in Table 9.1. The temperature limits and relative humidity adhered to in these tests determine the operating conditions. PCB's which are in accordance with our specification will satisfy the tests in para 6 of IEC-publ. 326 "General requirements and measuring methods for printed wiring boards".

The testing procedure given in Table 9.1 is in accordance with IEC-publ. 68 "Recommended basic climatic and mechanical robustness testing procedure for components for electronic equipment". Extreme temperatures are laid down for the temperature tests, appropriate to the base material. These temperatures and the duration of the damp heat test are classified to form climatic categories (see IEC-publ. 68):

for glass-fabric base material (G10 and FR-4):
−55 to +125 °C.
for glass-fibre (polyester) and paper base material:
−40 to +100 °C.

As stated in the Appendix, *A*2.2, the duration of the damp heat test (IEC-publ. 68, test C) is fixed at 21 days (500 hours). A quality laboratory, operating independently of development and manufacturing departments, establishes that the boards satisfy the requirements of our specification, after having been subjected to the tests mentioned in the testing procedure. These tests must be satisfied before a release for production is issued. At this stage, the acceptable quality level, or the maximum permissible percentage defective in a delivery batch, is established. During production, quality is assured by routine in-process inspections on the boards and on the test boards (as mentioned in 9.3). In addition, outgoing inspection is carried out by the Production Inspection Dept. and by the Quality Lab.

The use of test boards permits early detection of small process deviations well before the quality of the production boards is affected.

The testing procedure given in Table 9.1 applies to the pattern classes mentioned in Table *A*2 and is in accordance with para 6 of IEC-publ. 326 "General requirements and measuring methods for printed wiring boards". Table 9.1 only gives the nature of the test. For test performance see IEC-publ. 68. Inspection shall be carried out on at least 6 boards, divided into three groups of two boards.

9.2 Delivery

In the pre-delivery inspection a maximum permissible percentage defective AQL (Acceptable Quality Level) of 1.5% is applicable, unless otherwise stated. This percentage AQL is the average percentage defective which must not be exceeded in a delivered batch — and implies a 95% probability of acceptance provided the sample size and inspection level are in accordance with para 9.2.2.

9.2.1 Complaints procedure

The customer may lodge complaints if:

(a) in a sample size as per Table 9.2 a number of rejects exceeding the maximum permissible percentage defective is found.

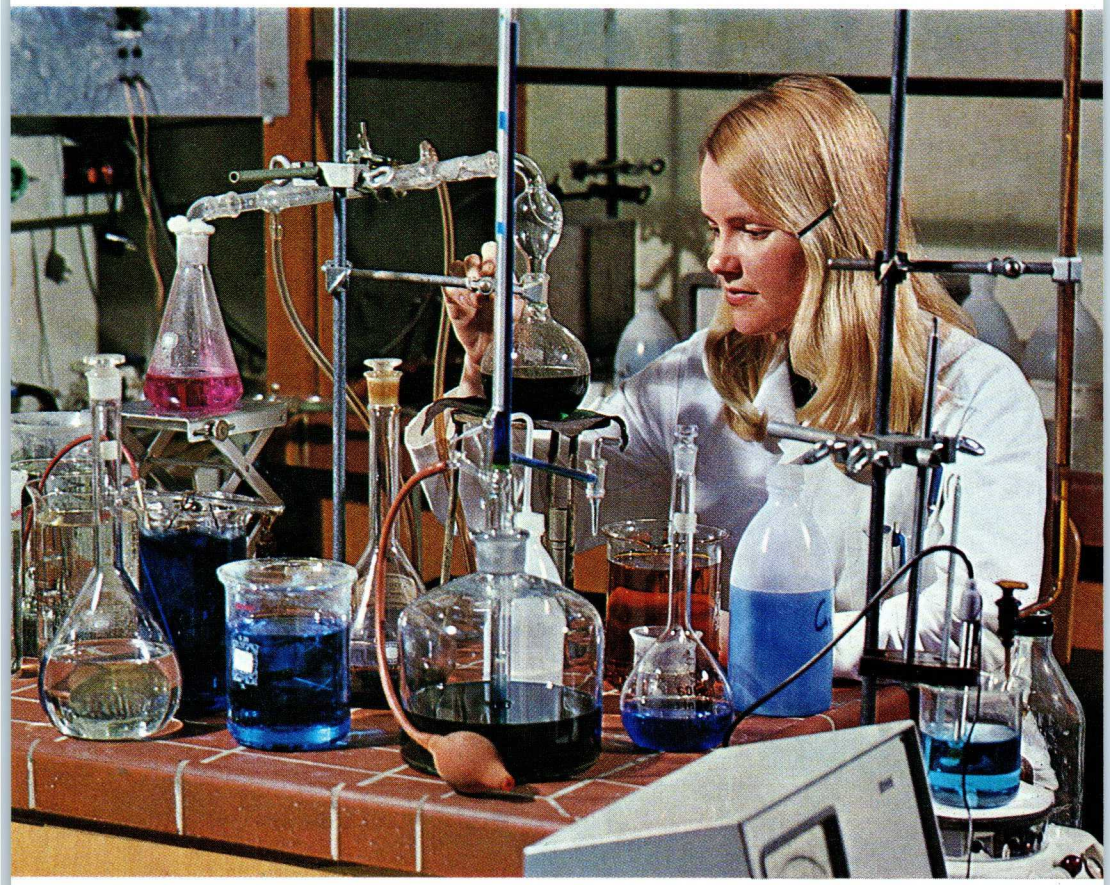
(b) in any other inspection procedure (e.g. a 100% inspection) a defective level exceeding 2% is found.

Conditions (a) and (b) are applicable at any time, irrespective of the average percentage defective of delivery batches inspected over a longer period of time.

9.2.2 Sample size and inspection level

Unless otherwise stated, lot size and sample size are as stated in MIL-STD-105D (table 2A, for level 2). The maximum permissible defective is specified in Table 9.2.

In a batch the maximum permissible number of *A*-faults may occur coincidently with the maximum number of *B*-faults.



Process control laboratory.

Table 9.1 Environmental tests

group	no. of PCB's	test method paragraph in IEC-publ. 68	examination or test	final measurements cross-reference to Appendix
0	6	—	measurement according to *A* 2.2	dimensions *A* 5 electroplating *A* 6 electrical *A* 8
I	2 from group zero		measurement according to *A* 2.2	visual requirements *A* 4 solderability *A* 7
II	2 from group zero	Na	change of temperature, 5 cycles of 6 hours (for temp. limits see para 9.1)	dimensions *A* 5 peel strength *A* 3
		B	dry heat, 1 cycle of 1 hour (for temp. limits see para 9.1)	
		D	damp heat (cyclic), 1 cycle of 16 hours 55 °C / 90-96% R.H.	
		A	cold, 1 cycle of 2 hours (for temp. limits see para 9.1)	
		D	damp heat (cyclic), 1 cycle of 16 hours 55 °C / 90-96% R.H.	peel strength [2] *A* 3 visual requirements *A* 4 dimensions *A* 5.4 electro plating *A* 6 solderability *A* 7 electrical *A* 8 plated-through holes [1] *A* 9
III	2 from group zero	C	damp heat (steady state), 21 days, 40 °C / 90-95% R.H., with 100 volts d.c. at 1 milliamp. applied	peel strength *A* 3 visual requirements *A* 4 dimensions *A* 5.2 electroplating *A* 6 solderability *A* 7 electrical *A* 8 plated-through holes *A* 9

for notes see next page

Table 9.2

lot size	sample size	maximum permissible number of boards exhibiting 1 or more *A*-faults	maximum permissible number of boards exhibiting 1 or more *B*-faults
90	8	0	1
91- 280	32	1	5
281- 500	50	2	7
501- 1200	80	3	10
1201- 3200	125	5	14
3201-10000	200	7	21

9.2.3 Fault classification

Definition of A an B faults

An *A*-fault is one which makes a PCB unusable. A *B*-fault is one which involves the risk of failure.

Fault description

An accurate description of *A* and *B* faults is given in Test Instruction "*L*", used by the quality laboratory. Deviations from the requirements quoted in the Appendix, Sections *A*3 thru *A*10 have been classified into *A* and *B* faults, dependent on the influence of the faults on the usability of the PCB. In principle any deviation from the permissible tolerance is an *A*-fault.

In order to avoid conflicts in the interpretation of the test results, the following limits have been set:

Diameter of plated-through and non-plated holes

A deviation from the maximum or minimum hole diameter by more than 0.05 mm is an *A*-fault, by more than 0.01 and less than 0.05 a *B*-fault.

Notes from table 9.1

[1]) Para *A* 9.2 of the Appendix is applicable only if the conductor pattern comprises at least 8 holes connected in series.

[2]) Measurements on the base material are made in accordance with the relevant material standard. The properties of the base material shall not be changed by the printing process.

Missing metal in a conductor

A deviation from the maximum permissible percentage of missing material, specified in Table *A*2, by 5% or more is an *A*-fault, by more than 1% and less than 5% a *B*-fault.

Conductor spacing

(a) Conductor spacing on finished board < 0.5 mm. A deviation from the maximum permissible dimension by more than 0.02 mm is an *A*-fault, by more than 0.01 and less than 0.02 mm a *B*-fault.
(b) Conductor spacing on finished board > 0.5 mm. A deviation from the minimum permissible dimension by more than 0.05 mm is an *A*-fault, by more than 0.01 and less than 0.05 mm a *B*-fault.

Repair of PCB's

Some of the faults which make PCB's unusable or unreliable can be remedied by repair. These repairs are permissible, provided they have no adverse effect on the quality of the PCB and the appearance remains acceptable. As a rule, we do not carry out such repairs except after prior consultation with the customer. Repairs are also possible after component mounting, without this having any adverse effect on the quality. Our repair methods are based on information derived from the booklet "Suggested Guide Lines for Printed Wiring Board Repairs" issued by the Acceptability and Repairability Committee of the Institute of Printed Circuits.

9.3 Test Boards

9.3.1 Test board to check the solderability

The test board is shown in Fig. 9.1 (Code number: 8222 297 03302). The solderability test is as previously described in para 7.2.1. In addition to the test pattern, the board comprises a group of 40 holes connected in series, which permit the hole quality to be assessed from a continuity test (para 5.3.3) or by metallographic sectioning. The diameters of the terminal areas are 2.5 mm. Holes are usually plated-through and of 0.8 ± 0.1 mm diameter.

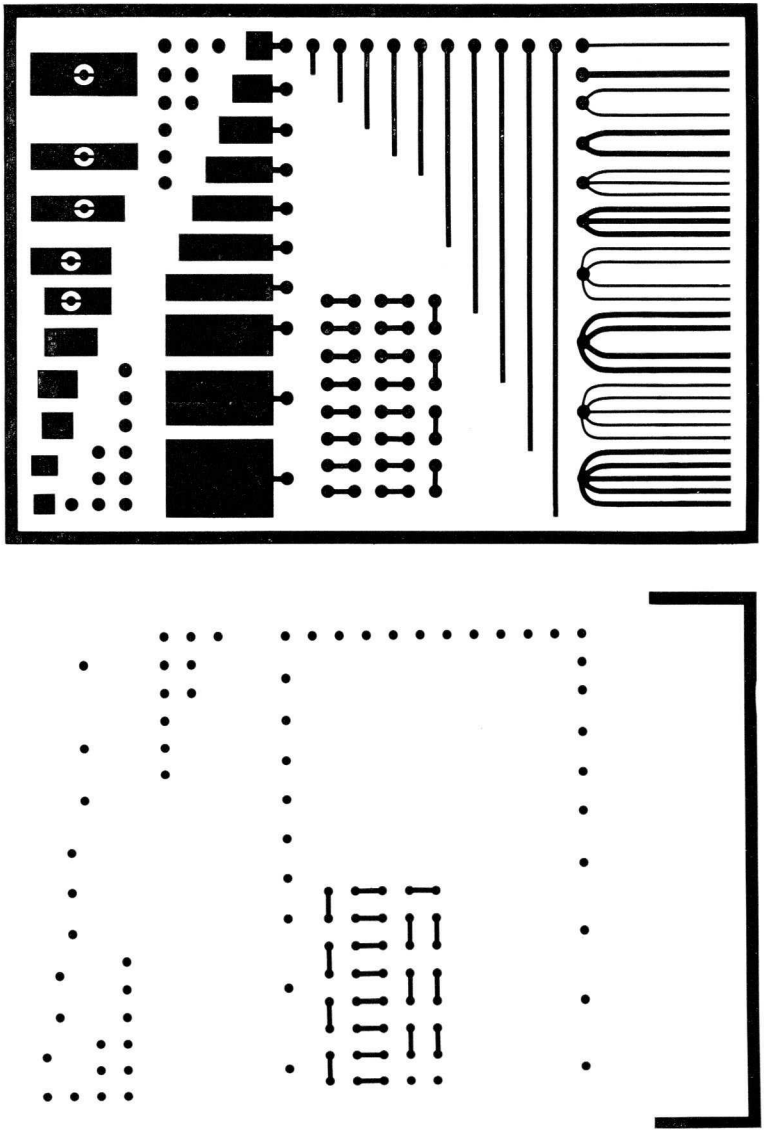


Fig. 9.1. Test board to check solderability.

9.3.2 Test board to check the hole quality by means of the continuity test

The continuity test is as described in para 5.3.3. Two test boards are used as shown in Figs. 9.2 and 9.3.

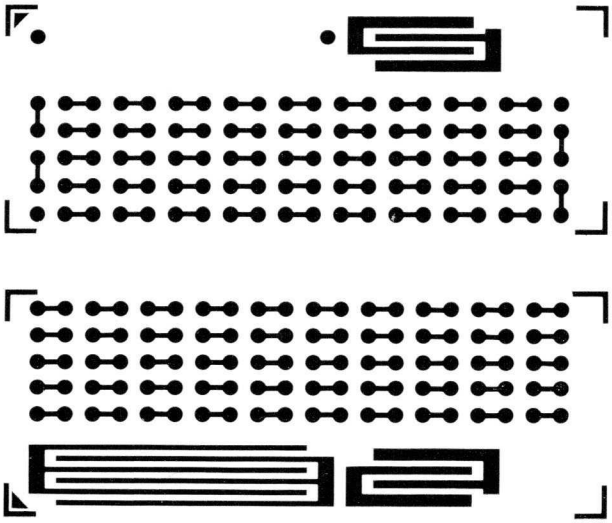


Fig. 9.2. Test board to check continuity.

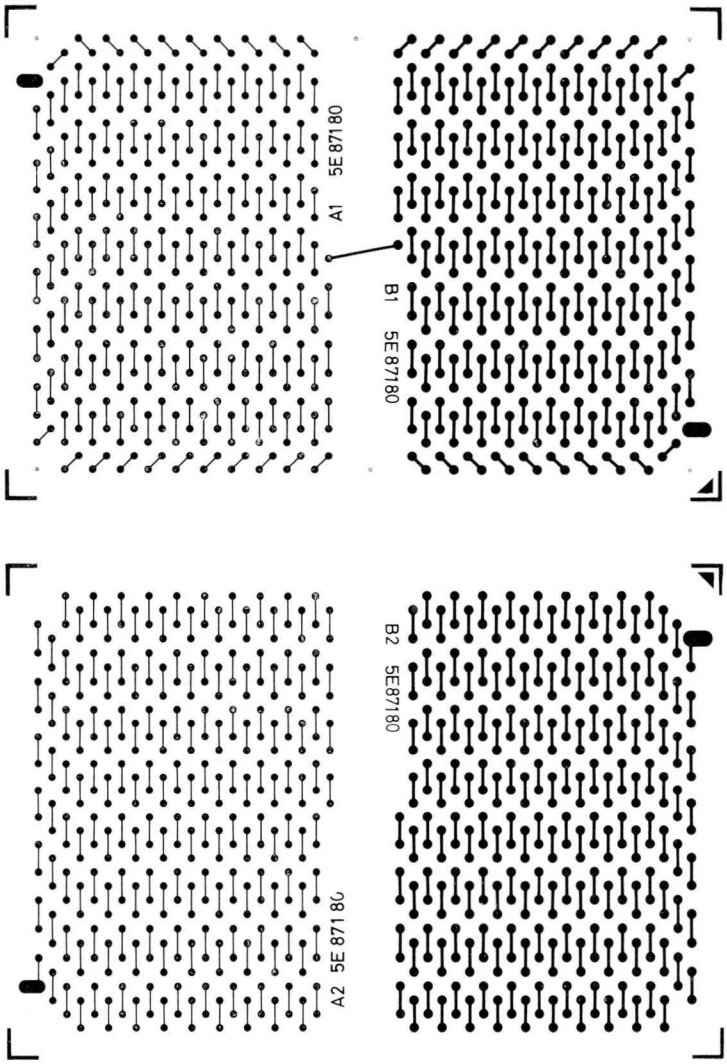


Fig. 9.3. Test board to check continuity.

(a) Test board as shown in Fig. 9.2 (Code number: 5E 890 64). This test board comprises 100 holes connected in series and spaced 0.2″ apart. The terminal areas have a diameter of 3 mm, and are linked in pairs by conductors, 1 mm wide. This type of board is normally used for testing plated-through holes of 1.3 ± 0.13 mm diameter, but other diameters are possible.

(b) Test board as shown in Fig. 9.3 (Code number: 5E 871 80). The test board comprises 2 groups, each of 340 holes connected in series and spaced 0.1″ apart. The holes are staggered, so that the centre-to-centre spacing is $\sqrt{2} \times 2.54$ mm = 3.6 mm. Normally, one group consists of plated-through holes of 1.3 ± 0.13 mm dia in 2.5 mm dia terminal areas, interconnected in pairs by 0.8 mm wide conductors. The other group usually consists of plated-through holes of 0.8 ± 0.1 mm dia in 1.9 mm terminal areas, interconnected in pairs by 0.6 mm wide conductors. Other hole diameters are possible. The test board in Fig. 9.2 is used for in-process inspection, whereas the test board in Fig. 9.3 is generally used for release procedures.

9.3.3 Test Board to Check the Insulation Resistance

The test board is shown in Fig. 9.4 (code number: 5E 871 79/2). It comprises two conductor patterns to determine the surface resistance, and a number of hole patterns to determine the surface and volume resistance (see para 2.2.2). The test board usually has plated-through holes of 1.3 ± 0.13 mm dia in 2.5 mm dia terminal areas, and plated-through holes of 0.8 ± 0.1 mm dia, in 1.9 mm dia terminal areas.

9.3.4 Test Board to Check the Peel Strength

The test board is shown in Fig. 9.5 (code number: 8222 297 0549). It comprises 3 groups of peel strength test conductors. The test is carried out in accordance with IEC-publ. 249-1 para 3.6 "Metal clad base materials for printed circuits". A test is performed on the first group in the state as received; on the second group after thermal shock (simulated soldering); and on the third group after simulated plating. The plating procedure is compatible with our process and is outlined below.

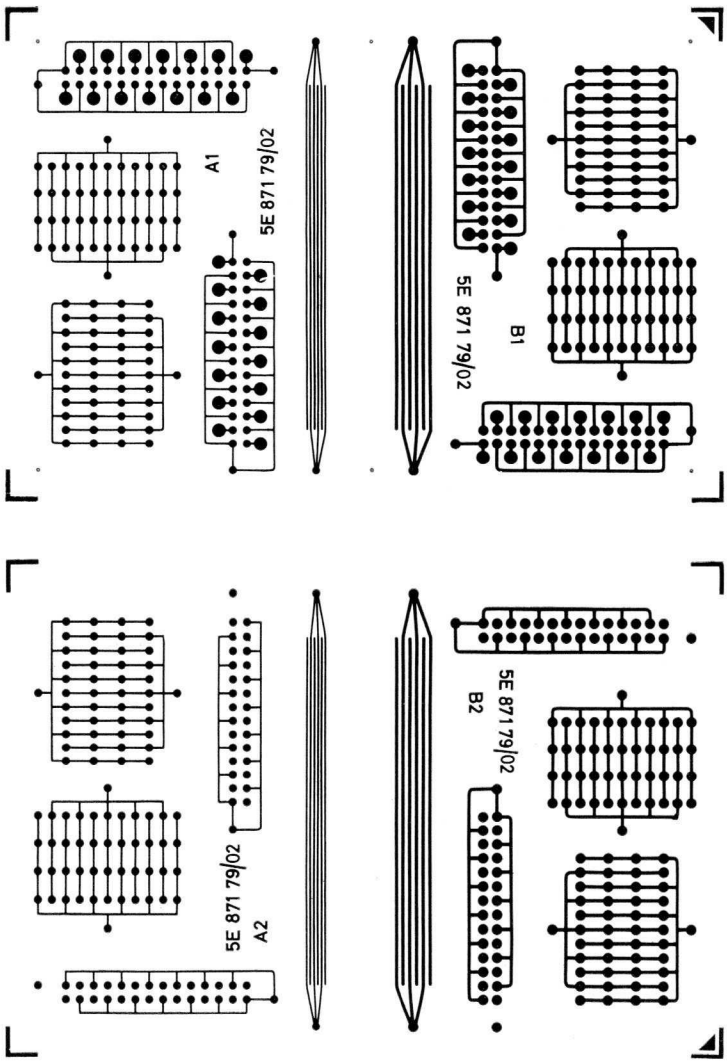


Fig. 9.4. Test board to check insulation resistance.

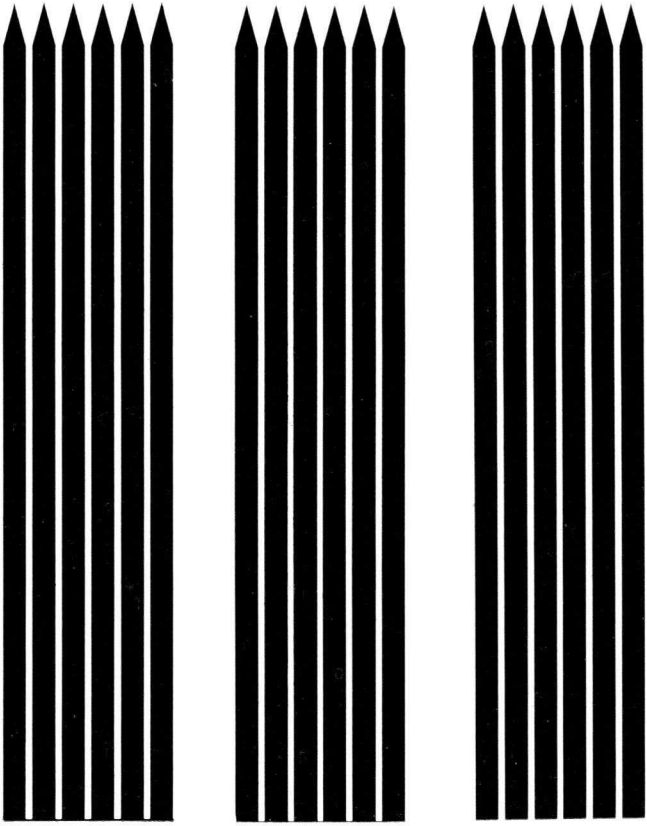


Fig. 9.5. Test Pattern to check peel strength.

Simulated plating procedure

Sequence of operations:

1. Immerse for 5 minutes in a solution of 30 g/l NaOH + 30 g/l Na_2CO_3. Bath temperature: 50 ± 3 °C.
2. Rinse for 1 minute in running tap water.
3. Spray for 1 minute with tap water.
4. Immerse for 30 minutes in a solution of 50 g/l NaCN. Bath temperature: 50 ± 3 °C.
5. Rinse for 1 minute in running tap water.
6. Spray for 1 minute with tap water.
7. Immerse for 30 minutes in a solution of 10 g/l concentrated H_2SO_4 and 30 g/l H_3BO_3. Bath temperature: 50 ± 3 °C.
8. Rinse for 1 minute in running tap water.
9. Spray for 1 minute with tap water.
10. Immerse for 30 minutes in a copper sulphate plating bath solution (without being connected to the current source).
11. Rinse for 1 minute in running tap water.
12. Spray for 1 minute with tap water.
13. Dry in air.

9.3.5 Test Board to Check the Electrical Properties

The test board is shown in Fig. 9.6 (code number: 8222 297 0550). The test pattern is in accordance with the ring and disk method quoted in IEC-publ. 249-1, Fig. 1. This pattern serves to measure dielectric losses (tan δ) and the dielectric constant (ε) according to the method described in IEC-publ. 249-1 "Metal clad base materials for printed circuits".

9.3.6 Test Board to Check Organic Coatings

The test board is shown in Fig. 9.7 (code number: 8222 297 05141). This board is used to test organic coatings (see para 6.5.2). It includes a test pattern for protective lacquer according to MMR-41A "Netherlands military specification of printed wiring boards and their assemblies". In addition to the aforementioned general test boards, our development section make use of a variety of other test boards for special requirements and applications.

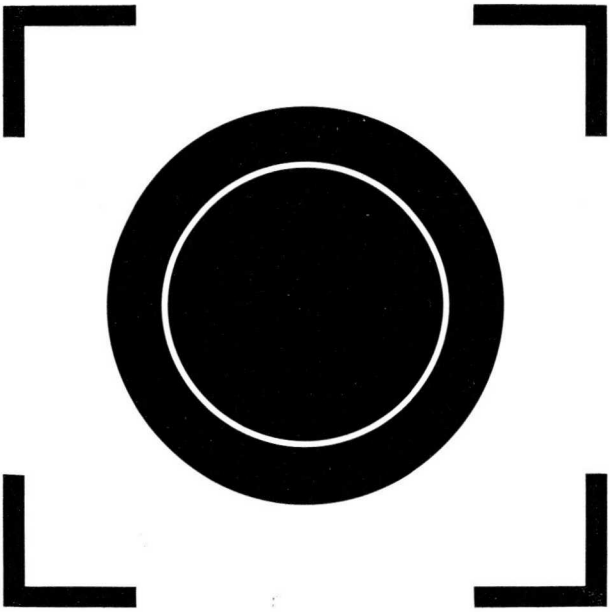


Fig. 9.6. Test board to check electrical properties.

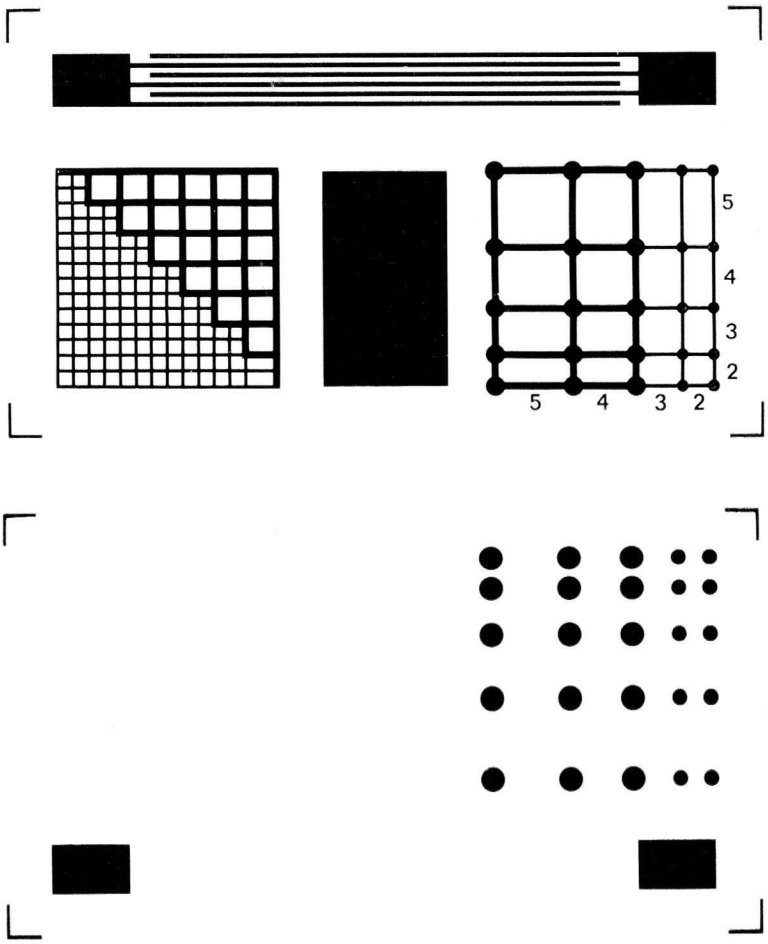


Fig. 9.7. Test board to check organic coatings.

9.4 UL-approval

Printed boards for use in the U.S.A. require a UL-approval, which is issued by the UNDERWRITERS LABORATORIES. The printed boards must be fabricated from a base material which has received UL-approval (see para 2.3.3) and satisfies standard UL-796. In the release testing procedure, which they carry out, only the adhesion of the pattern to the base material is examined. The procedure includes a solderability test, after a dwell in hot air and a dwell in water. The approval is granted on a per plant basis.

10 Master Pattern and Master Drawing

10.1 Master Pattern

10.1.1 Materials

The master pattern (para 4.1) or photo master is a precision reduction of the master drawing reproduced on a photographic film or plate. Its dimensional stability mainly depends on the base, which may be: cellulose tri-acetate, polyester or glass. The dimensional stability of master patterns on a cellulose tri-acetate or polyester base is affected by changes in temperature and relative humidity. Master patterns on a glass base are affected by temperature changes only.

It is not always possible to predict the dimensional change of a master pattern from these influences since they are not linear effects. An additional factor affecting the stability is the hardly predictable influence of the process. In total these influences cause considerably less dimensional changes to a polyester base than to a cellulose triacetate base. The changes are least when the master pattern has a glass base. In view of these effects, the climatic conditions under which the master pattern is made have to be identical to those under which it is used.

The conditions for the PCB fabrication process are the same as those laid down for the inspection in para *A* 2.5.6 of the Appendix (23 $\pm$ 2 °C and 50 $\pm$ 5% R.H.).

As a rule, glass based master patterns are only used for very fine conductor patterns (class III and IV). By contact printing from a glass based master pattern we make a second master pattern on a polyester base. The latter is used in the fabrication process (working master pattern).

When the pattern is difficult and/or fine, we should be consulted regarding the type of master pattern to be supplied.

Types of photographic materials which we have standardized on for PCB work are listed on next page:

Master patterns on a polyester base

For photographing: Kodalith Orthofilm type 3 (Estar thick base) 0.007″-0.18 mm thick. For contact printing: Kodalith Royal Orthofilm (Estar thick base) 0.007″-0.18 mm thick.
Coefficient of expansion:
0.0027% per °C change
0.0015% per 1% R.H. change
Size: 300×400 mm.

Master patterns on a glass base

Gevalith Ortho 08 (Agfa-Gevaert).
Coefficient of expansion: 0.00081% per °C change,
0% per 1% RH change.
Size: 300×400 mm, thickness $5\frac{1}{2}$ mm.

10.1.2 Definitions

A photographic film consists of a base coated with emulsion. The dull and soft side, which scratches easily, is the emulsion. The shiny side is the base. With the image remaining the same, the emulsion may be above (up) or below (down) with respect to the base. The film is negative when the image is transparent and the remainder black. Conversely it is positive when the image is black and the remainder transparent.

To exclude any misunderstanding, the photographic film must always be looked at in the same manner, viz.: the film must be placed so that the pattern, whether negative or positive, corresponds with the pattern on the board or on the master drawing. The emulsion will be above or below the base depending on the adopted process, see Fig. 10.1.

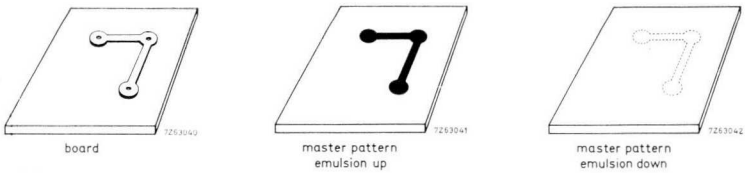
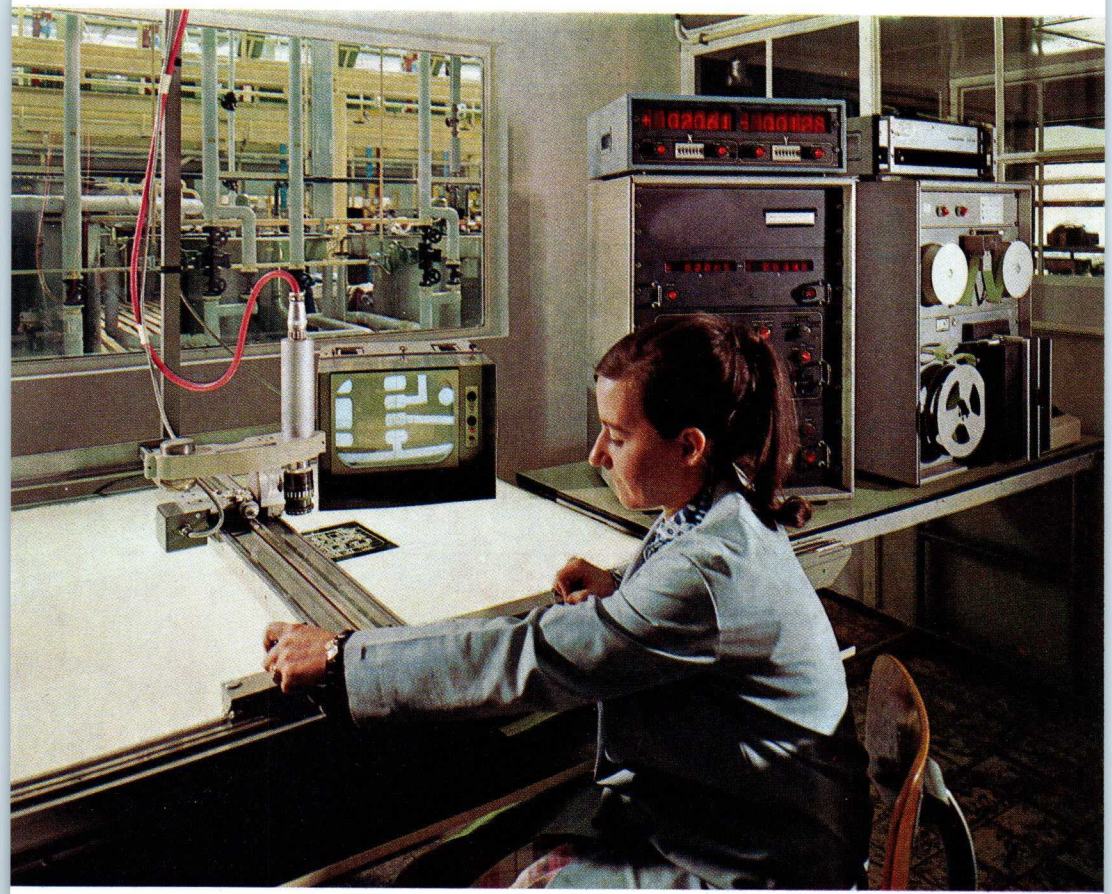


Fig. 10.1. Establishing emulsion direction.



Making tape for numerically drilling machine from co-ordinates on photo master.

Table 10.1 List of master patterns needed for the various processes.

	screen resist (para 1.3.1)		dry film resist (para 1.3.2)		wet photo-resist (para 1.3.3)		
reversed etch method (para 1.3.4)	neg.	pos.	pos.	neg.	pos.	neg.	type
	up	down	down	up	down	up	emulsion
direct method (para 1.3.5)	pos.	neg.	neg.	pos.	neg.	pos.	type
	up	down	down	up	down	up	emulsion
	working master pattern	original master pattern on glass base	working master pattern	original master pattern on glass base	working master pattern	original master pattern on glass base	

Note: When a master pattern is affixed to a glass base, a working master pattern has to be made by contact printing. This is used to produce the PCB (see also 10.1.1)

Master patterns for single and double-sided PCB's should be marked outside the board contour with one of the following codes:

A_0 = to denote film needed for making the tape for the drilling machine (para 3.3.1).
(If the tape for the drilling machine is derived from the tape used to make the artwork, this film is not needed.)
A_1 = Pattern at the component side or top of the PCB.
A_2 = Pattern at the soldering side or bottom of the PCB.

Dimensions

The dimensions of the master patterns in Table 10.1 for the screening method (1.3.1) and the photo resist solution method (1.3.3) are not critical. There must be a margin of at least 20 mm around the robber

enclosing the pattern (see 4.7.3). The master patterns for the photopolymer resist film method (1.3.2) should be of the following dimensions:

- Master patterns A_1 and A_2 shall all be approximately 5 mm larger than the fabrication format, the dimensions of which can be obtained on request.
- Surrounding the master pattern (positive) there shall be a black area of 10 mm width.
- A drill feed tape master pattern A_0 shall at 2 sides be 10 mm and at the other 2 sides be 5 mm larger than the fabrication format.
- All the master patterns shall have 2 registration marks contained within the black area but outside the PCB contour. These marks are to register the master patterns with respect to one another, see Fig. 10.2.

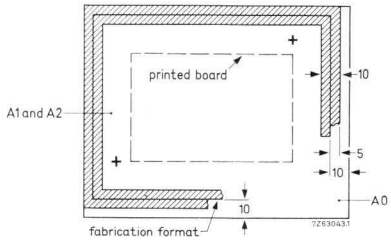


Fig. 10.2. Master pattern dimensions.

10.1.3 QUALITY AND TOLERANCES

Quality

Working master patterns shall be:

a. undamaged, free from finger prints and/or drying spots.
b. flat and capable of being stored and conveyed in a plastic bag.
c. without fog or pin holes when examined under 10× magnification, but may show some retouching on the non-emulsion or base side.
d. of correct exposure and a development density of 3.

$$\text{Density} = \log\left(\frac{\text{intensity of incident light}}{\text{intensity of transmitted light}}\right)$$

Tolerances

The master pattern must be within certain fidelity and registration tolerances. The fidelity tolerance is specified in Table *A* I and defines the limits which the master pattern dimensions may deviate from the design dimensions. The difference between artwork and design dimensions is

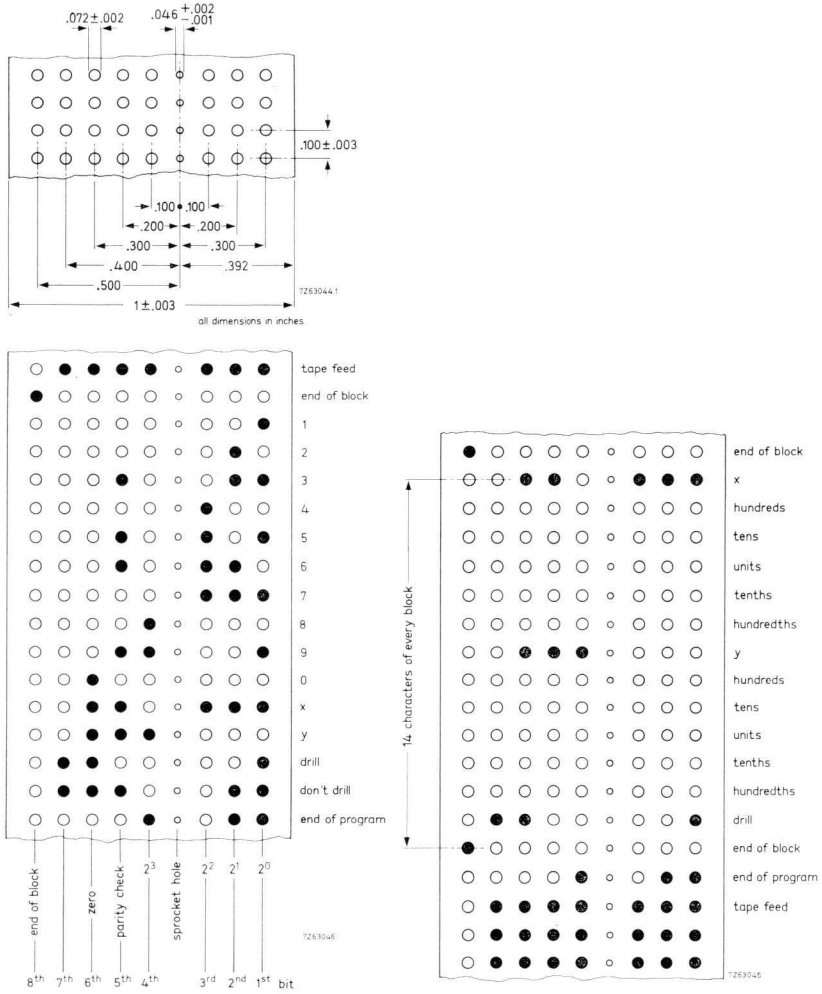


Fig. 10.3. Example of instructions on punched tape.

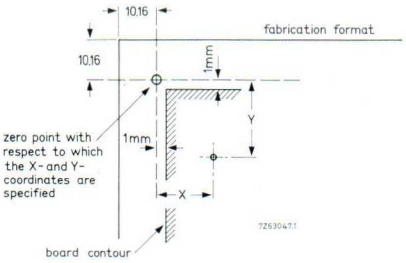


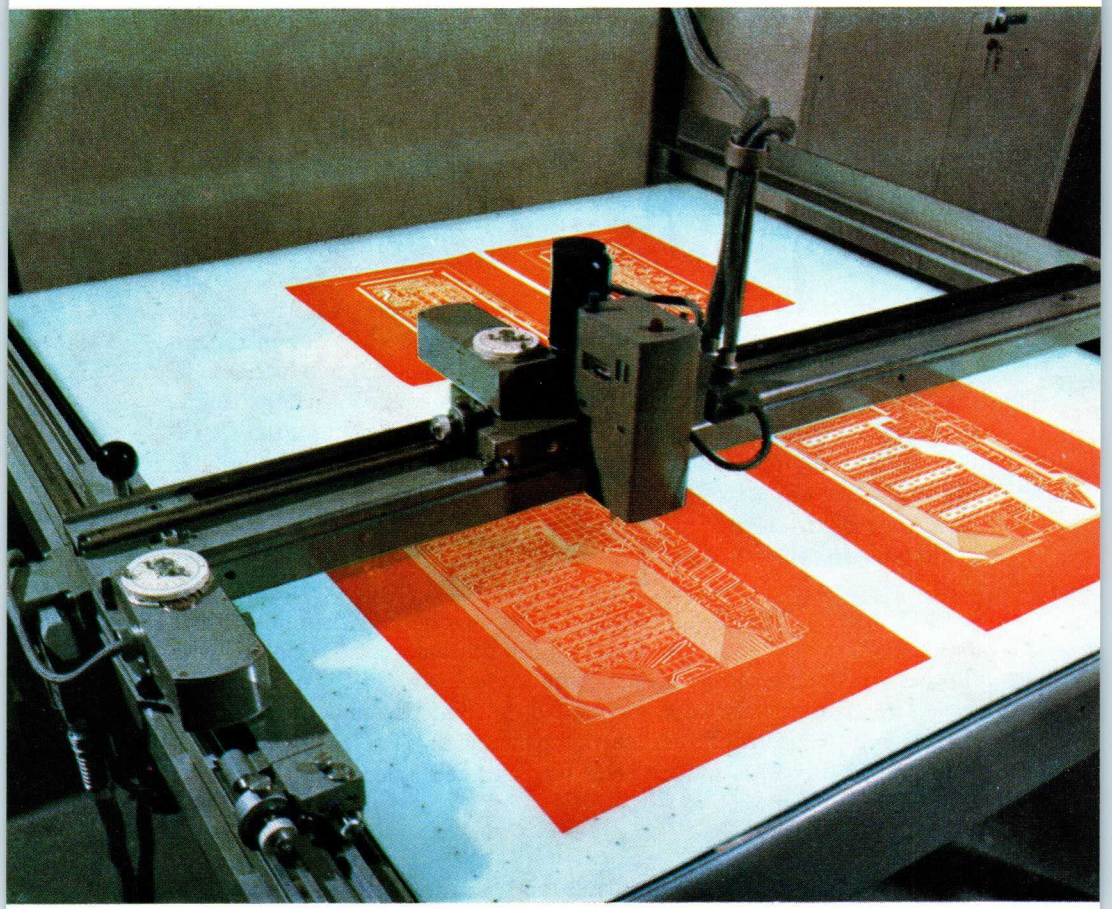
Fig. 10.4. Location of electrical zero.

included in this tolerance. Inspection of the master pattern for this tolerance is only possible when based on the theoretical design dimensions. If the tolerance is exceeded, then the finished PCB cannot be guaranteed to have the minimum conductor width and conductor spacing. When the artwork is prepared by a drawing or taping method, the attainable pattern tolerance is 0.05 mm. A tolerance of 0.025 mm can only be attained when the artwork preparation is by a "cut and strip" method on a drawing machine.

The registration tolerance is as specified in the Appendix and relates to the registration of the drill master pattern A_0 with the master patterns A_1 and A_2. The master patterns of the two board sides and the drill master pattern shall in no place show a deviation in registration one with another which exceeds the tolerance quoted in Table *A* I. To check this, the master patterns are superimposed on a light box and the deviation is measured by means of a measuring microscope (of at least 10× magnification). If the deviation exceeds the specified tolerance, the master patterns are discarded.

10.1.4 PUNCHED TAPE FOR NUMERICALLY CONTROLLED DRILLING MACHINE

Our numerically controlled drilling machine is programmed with a punched tape. The dimensions and coding are as shown in Fig. 10.3. The dimensions of the fabrication format have to be known before the electrical zero point can be determined. These are larger than the board dimensions and may be obtained on request. Fig. 10.4 shows the location of the electrical zero point.



Computer controlled drafting machine (co-ordinate plotter) fitted with head for cutting and stripping film master.

Completing the punched tape instructions for the drafting machine.

10.2 Master Drawing (Engineering Detail Drawing)

10.2.1 Function of the drawing

The drawing must provide all the relevant information required to make the PCB and must be presented in a clear and unambiguous manner. The information furnished by the master drawing may be considered in three groups.

a. The board contour dimensions and cut-outs, if any. The number of holes, their diameter and their locations with respect to the board contour. Board thickness and flatness limits.

b. True image of the pattern on the relevant board sides. The pattern dimensions are determined by the master pattern, as mentioned in para *A* 2.5, and by the process-dependent tolerance quoted in Table *A* 2. Hence, the dimensions for conductor width and conductor spacing need only be specified for information purposes. The pattern dimensions must never be measured on the engineering detail drawing since this drawing is usually not to scale.

c. Specification of the base material and the pattern plating. The base material must be specified in the appropriate place. If the customer requires base material from a certain supplier, this must be stated on the drawing. The plating, of a type and thickness as specified in the Appendix must be detailed on the appropriate part of the pattern. If plating of a non-standard type and thickness is required, this must be arranged beforehand. A general note must be included, stating that the PCB is in accordance with our specifications. If any deviation has been agreed upon, this must be indicated by a further note, including references to the relevant specifications.

10.2.2 Lay-out of the drawing

The views given on the master drawing must be as indicated in Fig. 10.5 and described in the following paragraphs.

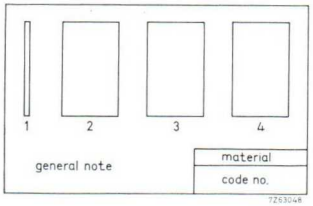


Fig. 10.5. Master drawing schedule.

1. *Board edge view*

This specifies board thickness and flatness limits, if any.

2. *Board top view*

The pattern is not included in this view. It is reserved to give the location, diameter and number of holes in accordance with the drill master pattern A_0 or the punched tape (for numerically controlled drilling machine). Registration and/or mounting holes, not included in the drill master pattern or punched tape, must be indicated here by means of dimensions. In addition, all contour dimensions and the location of holes with respect to the board contour, in accordance with the drill master pattern A_0, must be included.

3. *Board top view* (double-sided boards only)

This is a true image of the pattern on the top side of the board. (Board top side = component side = master pattern A_1.) Dimensions are not included. The location of the pattern with respect to the board contour is determined by the location of the holes. It must take into account the permissible pattern misalignment with respect to the holes, as established by measuring the distance from hole edge to terminal area edge see para 4.4 and Appendix Table *A* 2. The local pattern plating is also specified on this drawing.

4. *Board bottom view*

This is a true image of the pattern on the reverse side of the board. (Bottom of board = soldering side = master pattern A_2.) Dimensions are not included. The local pattern plating is specified on this drawing.

Note

Cross-sections, or enlarged details, may be included in all drawings to give greater clarity. Views 2, 3 and 4 are given identifying titles and these include the master pattern indications A_0, A_1, and A_2, or if there is no A_0 master pattern, the code number of the punched tape.

10.2.3 DIMENSIONING

Dimensions

Virtually complete international agreement has been reached regarding the method of presentation of dimensions on technical drawings. Philips Standard UN-D 34 complies with these.

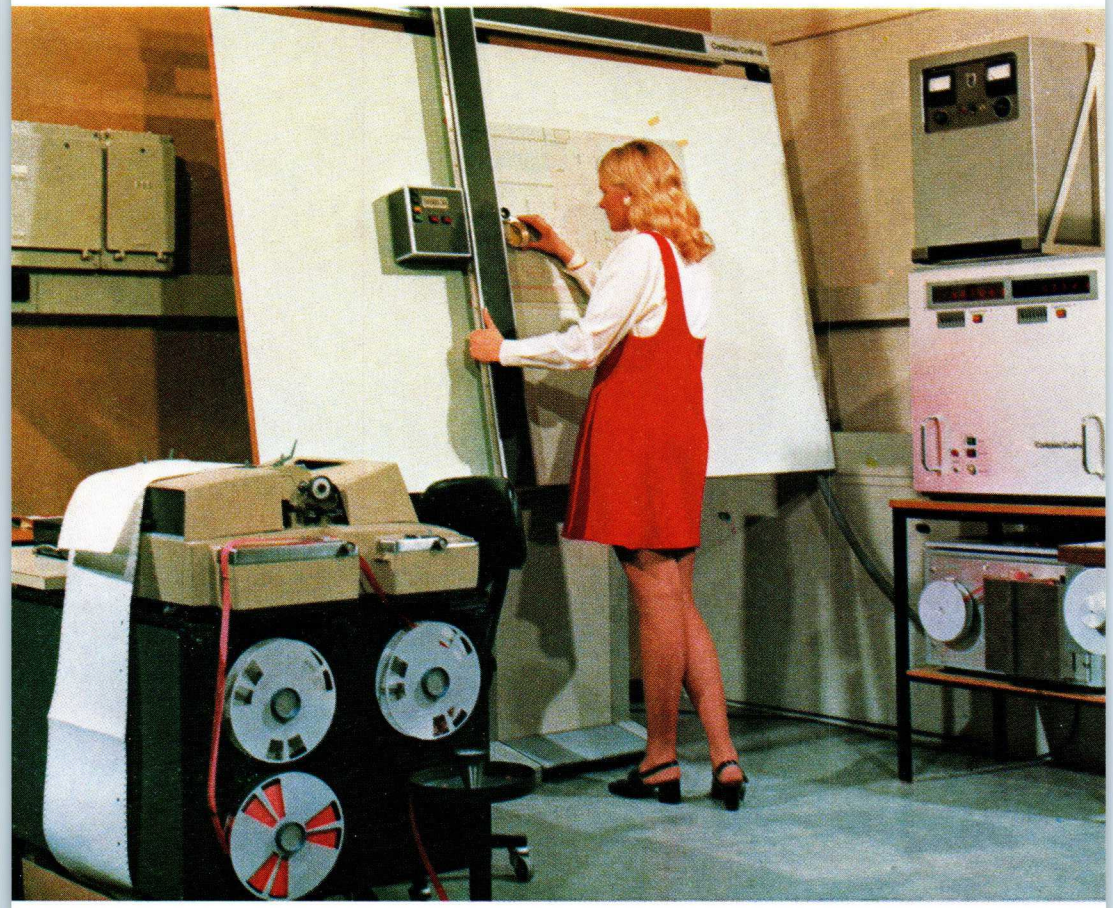
Tolerances

Tolerances necessitated by the printing process are specified in Table *A* 2 and were explained earlier in section 4. As a rule, electroplating has a $+100\%$ tolerance on thickness. The tolerances on contour dimensions, hole size, etc. were mentioned in section 3. Failure to comply with the specified tolerances will in most cases result in a cost increase and, if a special tool has to be made, in a longer delivery time.

Tolerances on position and form

As a result of international agrement, an ISO recommendation will be issued shortly. The Philips Standards UN-D 601, -602, -603 are in agreement with the ISO-recommendation.

Tolerances on position and form must only be specified where strictly necessary. If no tolerances on position or form are specified, the accuracy is determined by the dimensional tolerance, i.e. there may be deviations from form and position provided they are within the dimensional tolerances.



Layout digitiser translates co-ordinates from hand-drawn layout into punched tape code to feed computer controlled drafting machine.

Appendix Specification

A 1 General

These specifications cover rigid single- and double-sided PCB's made from one of the following laminates:

- Glass-fabric base, epoxy resin
- Glass-fibre base, polyester resin
- Paper base, epoxy resin
- Paper base, phenolic.

The conductor pattern is electroplated. The holes may or may not be plated-through. PCB's are classified according to size, pattern fineness and complexity. Hence the classes represent the degree of processing difficulty. PCB's of any class are available in any of the above mentioned base materials.

A 2 Classification and Test Conditions

A 2.1 Classification

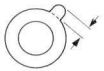
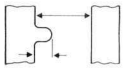
The PCB class is made up from a combination of a max. size and a pattern class as detailed in Tables *A*1 and *A*2.

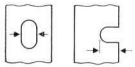
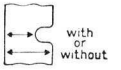
Pattern class
The pattern class is made up from a combination of various extreme minimum values as shown in Table *A*2.

Table A1 Maximum PCB sizes

size no.	max. dimensions of board or multiple board
1	130 × 120 mm
2	130 × 230 mm
3	130 × 270 mm
4	130 × 370 mm
5	200 × 230 mm
6	270 × 370 mm
7	350 × 460 mm

Table A2

PATTERN CLASS →				I		II	III	IV
	nom. hole dia.	tol. plated hole	tol. non-plated hole	nom. dia. of terminal area as measured on master pattern				
For interfacial connection only [1])	0.5	− 0.2	—	—	—	1.0	1.0	1.0
measured on finished board unless otherwise stated ↓	0.6	± 0.1	± 0.05	1.9	1.6	1.2	1.2	1.2
	0.8	± 0.1	± 0.05	2.1	1.8	1.4	1.4	1.4
	1.0	± 0.13	± 0.1	2.3	2.0	1.6	1.6	1.6
	1.3	± 0.13	± 0.1	2.5	2.3	1.9	1.9	1.9
min. distance: from edge of hole to edge of terminal area mm				0.2	0.1	0.1	0.1	0.1
isolated indentations at edge of terminal area mm				0.2		0.1	0.1	0.1
isolated projections at edge of terminal area mm				0.2		0.2	0.2	0.1
tolerance on width of conductors and terminal areas	screen printing method			(+0.1) ± 0.1 [2])		(+0.1) ± 0.1)	(+0.07) $^{+0.1}_{-0.07}$	—
	dry film resist method			—		—	—	± 0.03
isolated projection in % of calculated min. local conductor spacing				$33^1/_3$ max. 0.4 mm	[3]) 0		[3]) 0	0

Indentation or hole in % of calculated min. local conductor width		20	20 max. 0.4 mm	[4]) 10	[4]) 0
min. conductor width (nom. photo dim.) mm		0.6	0.3	0.25	0.25
min. conductor width with/or without indentations mm		0.44	0.22	0.2	0.2
min conductor spacing without blemishes mm		0.75	0.2	0.2	0.2
nom. conductor pitch (photo) mm		1.65	0.76	0.675	0.508
photo tolerance mm — on width of conductor and terminal areas		± 0.05	± 0.025	± 0.025	± 0.02
photo tolerance mm — on conductor pitch		± 0.05	± 0.03	± 0.03	± 0.02
photo tolerance on opposite board side pattern registration mm		± 0.05	± 0.05	± 0.05	± 0.03

[1]) Not used for component mounting.

[2]) With respect to the dimension on the photo master, the finished PCB will exhibit a systematic overhang of 0.1 mm and, in addition, be subject to a screen-printing tolerance of ± 0.1 mm. Hence the combined tolerance is (+0.1) ± 0.1 = (+0.2-0) with respect to the corresponding dimension on the photo master.

[3]) If the calculated minimum local conductor spacing is 0.3 mm or more, the maximum permissible excess metal is $33\frac{1}{3}$% of the spacing, or 0.4 mm, whichever is less.

[4]) If the calculated minimum local conductor width is 0.3 mm or more, the maximum permissible reduction in width is 20% of the width, or 0.4 mm, whichever is less.

Notes

- For further information relative to Table *A*2 see Section 4.
- For finished PCB conductor dimensions relative to the master pattern see Figs *A* 5.2, *A* 5.3 and *A* 5.4. These apply to the screen printing method and to the pattern classes given in Table *A* 2.

A 2.2 Standards of acceptance

Unless otherwise stated, the PCB's shall satisfy the requirements given in this specification.

- Under normal atmospheric test conditions to IEC publication 68: "Recommended basic climatic and mechanical robustness testing procedure for components and electronic equipment".
- After climatic test to para 6.3 of IEC publication: "General requirements and measuring methods for printed wiring boards". Temperature category:
  55/125 for glass-fabric epoxy resin laminate
  40/100 for glass-fibre polyester resin laminate and paper phenolic laminate.
- Humidity classification: 21

A 2.3 Applicable documents (latest issue)

- IEC-publ. 326 "General requirements and measuring methods for printed wiring boards".
- IEC-publ. 68 "Recommended basic climatic and mechanical robustness testing procedure for components and electric equipment".
- IPC-A-600 "Acceptability of printed circuit boards".
- This Publication.

A 2.4 Order of precedence

Where there are differences between the photo, the printed board drawing, and the specification, the order of precedence shall be as follows:

1. photo
2. board drawing
3. specification

A 2.5 Photo Master

- The finished PCB pattern will exhibit a specified maximum allowable deviation from the photo master, the deviation being process-dependent (see Figs *A* 5.2, *A* 5.3 and *A* 5.4).
- A given pattern dimension for the finished PCB can be realised only if, in the corresponding dimension on the photo master, an allowance is made for the specified maximum allowable deviation (see Table *A* 2).
- The pattern dimensions of the finished PCB will be guaranteed only with respect to the corresponding dimensions on the photograph, the maximum allowable deviation having been taken into account.
- When the photograph is supplied by the customer, the accuracy of the photograph, with respect to the circuit and to the pattern dimensions, will be the customer's responsibility.
- When the lay-out and the photograph are prepared by us the responsibility for the pattern dimensions will remain ours.
- The dimensional inspection of the photo shall be performed at 23 ± 2 °C and $50 \pm 5\%$ R.H.
  (For information on lay-out etc. see Section 10.)

A 3 Requirements to be Satisfied by Base Materials

- The PCB's shall be made from one of the laminates listed in Table *A* 3 and covered by the specifications given against them.
- Laminate of a given manufacture will be supplied only if specified explicitly on the master drawing.
- If only the type of laminate is specified, a selection will be made from those that satisfy the applicable specification mentioned below.
- When processed the laminate shall not show any deterioration of these properties.

Laminates other than those listed above can be supplied by arrangement between customer and supplier.

A 4 Visual Requirements for PCB's

A 4.1 Comparison with standard

Where a visual comparison with a standard is required, the quality level "acceptable" illustrated by an example photograph in document IPC-A-600 "acceptability of printed circuit boards" shall apply.

Table A3.

laminate	max. operating temperature	Philips standard	NEMA publ. LI-2	MIL-P 13949	IEC publ. 249-2
glass fabric base, epoxy resin	−55 to +125[1])	NLN-K669	FR-4	GF	EP-GC-Cu-5
glass fibre base, polyester resin	−40 to +100	NLN-K1221	—	GC	—
paper base, epoxy resin	−40 to +100	—	FR-3	PX	EP-CP-Cu-3
paper base, phenol	−40 to +100	NLN-K1197	XXXP	—	PF-GP-Cu-1
paper base, epoxy	−40 to +100	—	FR-2	—	—

[1]) Max. operating temperature UL-approved PCB: 105 °C

A 4.2 General requirements

- Board and pattern shall be free from dirt, stains, corrosion products, and finger prints.
- Laminate shall not show cracks, blisters or delamination.
- Glass-fabric base laminate may show some "measling" and crazing in non-critical areas.
- Pattern and printed characters shall be in accordance with the photo master.
- Non-printed characters shall be in accordance with the master drawing.
- Characters shall be readable.
- No part of the pattern shall be lifted from the base material.
- In any one batch, there shall be no excessive differences in base material colour.
- Contour and cut-outs shall be finished smooth.

A 4.3 Electroplating

General requirements

- Pattern shall not show crazing or cracks when viewed under X10 magnification.
- Pattern shall show no unevenness other than that present on the plain substrate.
- Electroplating may exhibit slight roughness in non-critical areas.
- Electroplating shall show no evidence of burning, unless this is unavoidable owing to the pattern configuration, and, in that case, the requirements on plating thickness (*A* 6.1) and conductor width (Table *A* 2) shall not apply.
- Metallic deposits between conductors are permissible in non-critical areas, provided they are adherent.
- Spurious deposits shall have been removed from critical areas and their removal shall not have resulted in an inferior appearance or reduced insulation resistance.
- When the pattern is viewed from above with X10 magnification, no copper or resist shall be visible along the conductor edges.
- No requirements are made with respect to current distribution aids which are discontinuous to the conductor pattern.
- The side-faces of the conductor and terminal areas will consist of bare copper, except in the case of gold contacts at the edge of the PCB.

Tin-lead plating

- Scratches are permissible, provided the underlying metal is not visible.
- Minor pitting is acceptable, but this shall not cause an inferior appearance.

Gold-plating (contacts)

- Viewed with the unaided eye, the gold-plated contacts shall not show pitting, scratches, or other mechanical damage.
- Pin-holes in the gold-plating are acceptable, provided they do not occur in concentrations greater than 5 and the max. pin-hole size is 0.1 mm or less *.
- On no more than 2 contacts per PCB side there may be one pin-hole, larger than 0.1 and less than 0.25 mm (provided the max. allowable percentage of indentation as quoted in Table *A* 2 is not exceeded) *.
- In the transition area from gold to tin-lead plating, a bare nickel area is permissible which does not exceed 300 μm, measured in the length of the contact.
- The contact shall not be lifted where it extends onto the chamfered edge of the PCB.

A 4.4 UNDERCUT

- With all electroplatings mentioned in Section *A* 6, except nickel and gold, undercut shall not exceed 0.05 mm per edge of conductor.
- With the gold or nickel-gold plating mentioned in Section *A* 6, undercut shall not exceed 0.07 mm per edge of conductor or contact.

Note

Gold-plated contacts for edge connectors will have enclosed edges since they are plated subsequent to etching.

* These requirements do not apply to the areas used for plating-up of the contacts (see Section 8).

A 4.5 PLATED-THROUGH HOLES (inspected under X10 magnification)

With epoxy glass-fabric and polyester glass-fibre laminates (double-sided)

- Voids in holes are permissible provided the requirements of *A* 7.2 and *A* 9 are met.
- After a climatic test (as mentioned in *A* 2.2), the holes shall be examined. No foreign materials shall be present.

With paper base, single-sided epoxy glass-fabric and polyester glass-fibre laminates

- Voids in holes are permissible, provided the requirements of *A* 7.2 are met.

A 5 Dimensional Requirements

A 5.1 CONDUCTOR PATTERN DIMENSIONS

For all dimensions of the finished PCB pattern, the applicable maximum allowable deviation from the photograph, as quoted in Table *A* 2, shall be taken into consideration.

The maximum and minimum conductor width and the width in places where blemishes occur, are indicated on the graph of Fig. *A* 5.3 against the corresponding photograph dimension. (For a definition of conductor width, see Fig. *A* 5.1.)

The graph of Fig. *A* 5.3 applies with the screen printing method and is according to pattern class. For the dry-film resist method dimensions can be derived from sub-section 4.6.

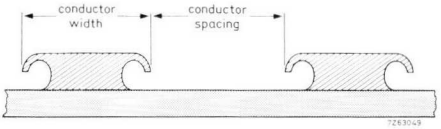


Fig. A 5.1. Definition of conductor width. and spacing.

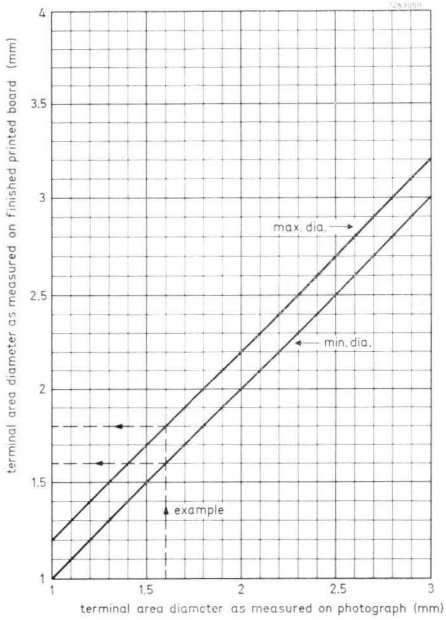


Fig. A 5.2. Tolerance on terminal area diameter.

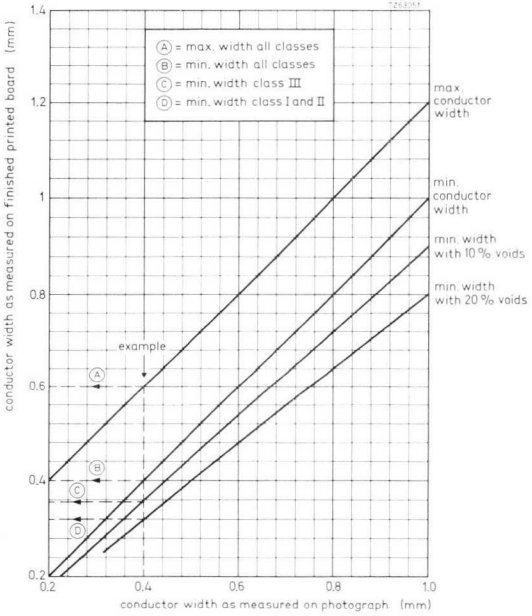


Fig. A 5.3. Tolerance on conductor width.

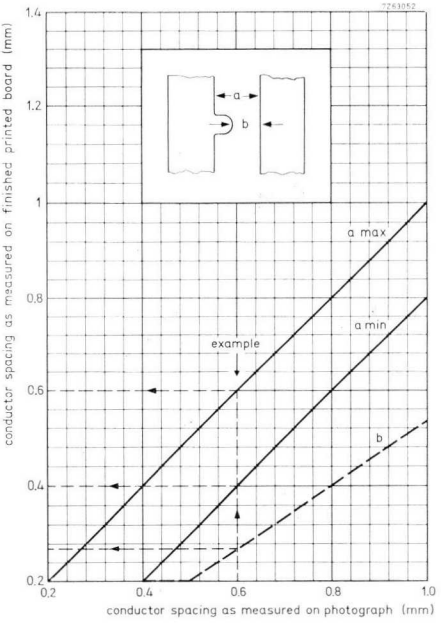


Fig. A 5.4. Tolerance on conductor spacing.

Conductors (and areas) of more than 2 mm width

The projections or identations shall not exceed 0.4 mm.

Length of blemishes

The length of a blemished area (projection or indentation) may be equal to the local conductor width but shall not exceed 5 mm.

Number of blemishes

No limit, as long as the appearance remains satisfactory.

Conductor spacing

The maximum and minimum conductor spacing and the conductor spacing, in places where there are projections, is indicated on the graph of Fig. *A* 5.4 against the corresponding photograph dimension. This graph applies with the screen printing method and is according to pattern class. For the dry film resist method dimensions see subsection 4.6.

Terminal area

The maximum and minimum diameter shall be as indicated on the graph of Fig. *A* 5.2 against the corresponding photograph dimension. This graph is related to the adopted process.

Blemishes in the edges of terminal areas

The maximum permissible blemishes (projections or indentations) shall be as specified in Table *A* 2, provided that the minimum distance from hole edge to terminal area edge is satisfied.

Length and number of blemishes

No limit, as long as the appearance remains satisfactory.

Misalignment of pattern with respect to holes

The smallest distance from hole interface to nearest edge of terminal area shall be equal to or greater than the minimum distance specified for each pattern class in Table *A* 2.

Front to back pattern misalignment

The permissible misalignment of the front pattern with respect to the back pattern is twice the misalignment mentioned above. With double-sided edge-connectors, the maximum permissible misalignment of contact fingers on one side with respect to those on the other side is 0.4 mm. This requirement is only applicable in the contact area.

A 5.2 PCB DIMENSIONS

Contours and cut-outs and their alignment with respect to the plated-through holes

The tolerance on these dimensions shall be in accordance with the master drawing (see Section 3).

This tolerance shall apply unless otherwise arranged between supplier and customer.

Tolerance on hole location

On the finished PCB, each plated-through hole whose location is specified on a certified photo (see *A* 2.5), may have a radial deviation not exceeding 0.08 mm from the location given on the certified photograph.

When the tolerance on the hole spacing (2× radial deviation) is determined, the non-reproducible dimensional change of the base material shall be taken into consideration (see subsection 3.4).

Non-plated through holes shall satisfy the tolerance specified on the master drawing. The master drawing shall be as described in Section 10 unless otherwise arranged between supplier and customer.

Flatness

Flatness shall only be measured when specified on the master drawing. Measurement shall consist of passing the PCB through a thickness gauge made up from two parallel plates of suitable dimensions. The distance (d) between the two plates (see Fig. *A* 5.5) shall be calculated from:

$$d = s + h,$$

where s = max. thickness of finished PCB

and h = specified flatness tolerance.

The tolerance given on the master drawing shall be derived as follows:

$$h = L^2/8r,$$

where L = length of PCB diagonal

r = specified radius of curvature according to IEC-publ.249-2.

Fig. A 5.5. Method of measuring board flatness.

Thickness

Preferred values are 0.8 mm and 1.6 mm for general purpose use and 1.5 mm if direct edge-connectors are required.

Tolerance (double-sided PCB's)

Tolerance of base material +0.1 mm. Where printed edge-connectors are required, the tolerance is ± 0.2 mm.

A 6 Requirements to be Satisfied by Electroplating

A 6.1 Plating material and thickness

Unless otherwise specified on the master drawing the plating shall consist of one or more of the materials as specified below.

Copper

the average layer thickness of electrolytic copper shall be at least 20 μm and nowhere less than 10 μm in a plated through hole. The layer shall continue over the entire pattern, the layer thickness on the pattern being not less than 35 μm.

Tin-lead

The proportion of tin shall be between a minimum of 50% and a maximum of 70%. The layer thickness shall be at least 8 μm in a plated through hole and at least 15 μm on the pattern.

The tolerance on the thickness shall be +100%-0%.

Nickel

Normal dull Watts nickel. Layer thickness 6 (+6-0) μm under gold plating. This layer may be deposited on the entire pattern if part of the pattern is to be gold-plated.

Gold

Soft dull gold or hard bright gold of at least 23.8 carats. Plating thickness of contacts for edge connectors shall be

2.5 (+2.5-0) μm.

A 6.2 Plating thickness measurement

The gold plating thickness is measured by means of a Bêta Back Scatter Gauge. The thickness measurement on other platings is made by means of a micro-ground cross-section.

A 6.3 Plating adhesion

The plating adhesion shall be tested as follows:

- Place a strip of contact adhesive cellulose acetate tape (non-hardening) on a part of the conductor pattern where there is a conductor area of at least 1 cm^2.
- Press the tape firmly onto the surface to eliminate all air bubbles. Leave a tab for pulling. After 10 s, pull the tape off the board with a sharp pull at right angles to the PCB. The test should be repeated at three different locations on each PCB tested, including contact areas, if present.

Test Requirement: There shall be no metal particles adhering to the tape, other than those which derive from overhang.

Note: A suitable tape is Tesa film no. 4104. Adhesive strength measured according to UN-L 1015, method A: $\geqslant$ 185 g/cm.

A 7 Solderability Requirements

A 7.1 PCB surface

PCB's soldered by current conventional methods shall exhibit an even solder coating. Some dewetting in non-critical areas is permissible.

Assessment shall be based on the quality level "acceptable" shown by the example photograph in IPC-A-600 "Acceptability of printed circuit boards".

A 7.2 Plated through holes

All plated-through holes whose solderability is not affected by the pattern, shall show evidence of good wetting. This requirement does not apply to holes which are for interfacial connection only.

A 7.3 SOLDERABILITY TEST

The solderability test shall be in accordance with the additions to IEC publication 326. The tests shall be made with soldering flux 502 (code No. (NLN) 1322 506 86601), containing 0.5% of chloride.

The specimen shall be cut from the PCB under test and may be processed so that the pattern has no effect on the solderability.

A 7.4 SOLDERABILITY AFTER STORAGE

Solderability, to the standards described in *A* 7.1 and *A* 7.2, shall be obtainable six months after delivery, on condition that the PCB's are stored at the ambient conditions stated in IEC publication 68, viz.:

temperature:	from +15 °C to +35 °C
relative humidity:	from 45% to 75%

A 8 Electrical Requirements

A 8.1 INSULATION RESISTANCE

Test

As stated in IEC publication 326 "General requirements and measuring methods for P.W. boards".

Applied voltage:

100 ± 15 V d.c. when conductor spacing is less than 1 mm.

500 ± 50 V d.c. when conductor spacing is 1 mm or more.

The measurement shall be made:

- between 2 conductors where in a length l there is a uniform spacing b and where b/l is less than 1/25
- or between conductors as agreed between supplier and customer.

Requirement

After climatic tests as mentioned in *A* 2.2 the insulation resistance shall be:

$> 10^3$ MΩ for epoxy glass fabric laminate

$> 10^3$ MΩ for polyester glass fibre laminate

> 100 MΩ for epoxy paper laminate

> 100 MΩ for paper phenol laminate

A 8.2 Dielectric strength

Test

Immediately after the insulation resistance test described in *A* 8.1, a potential with a risetime of less than 5 seconds, shall be applied for 1 minute. This will normally be 700 V 50 Hz, unless otherwise specified on the board drawing.

Requirement

After the climatic tests mentioned in *A* 2.2 there shall be no breakdown or flash-over.

A 9 Requirements on Plated-through Holes

These requirements are not applicable to plated-through holes in phenol and epoxy paper base laminates and in single-sided epoxy glass-fabric base and polyester glass-fibre base laminates.

A 9.1 Re-soldering

Test

A tinned wire of diameter approx. 0.2 mm less than the specified minimum hole diameter shall be soldered into the plated-through hole and then subjected to five cycles of unsoldering and soldering.

- Soldering time: 4 ± 1 sec.
- Soldering iron: conventional 60-Watt type, capable of producing a tip temperature of approx. 232-260 °C during soldering.
- Solder: Tin solder 59 cored with soldering flux 524 to NLN-W004.

On completion of the soldering cycles, the PCB's shall be placed in a tensile tester and a straight pull applied to the wire. There shall be no damage visible to the unaided eye. Unless otherwise arranged between customer and supplier, a pull force of 90 Newton shall be applied.

A 9.2 Continuity of interfacial connection by plated-through hole after soldering (IEC publication 326)

Test

After preheating for 1 hour at 125 °C the PCB is subjected to simulated dip soldering i.e. dipping in silicone oil heated to 260 (+5-0) °C
- 20 s for epoxy glass-fabric.
- 10 s for polyester glass-fibre.

The conductor patterns on the two sides of the PCB shall remain electrically connected via the plated-through hole, as evidenced by a resistance measurement.

The resistance measurement shall be made with a current not exceeding 0.1 A on at least eight holes connected in series by the conductor pattern. Measurements are made before, during and after simulated soldering. The value must not increase by more than 200% during simulated soldering and must not be greater than 10% higher than the original value thereafter.

A 9.3 Reliability of interfacial connection by plated-through hole

The electrical connection and the resistance change as stated in *A* 9.2 are tested as follows: Special test panels, which have been processed in the same way as the production boards, each having 100 plated-through holes in series, are subjected to ten simulated dip-soldering operations.

Measurements are made at intervals on a sufficiently large number of holes to provide a valid indication of the failure rate, which is better than 1 in 10^5. This indirect method of testing cannot be taken as a guarantee of plated through hole reliability, but can be considered as a sufficient indication.

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Printed in The Netherlands

8 PQR48 (16) 10-'71

9399 266 00401