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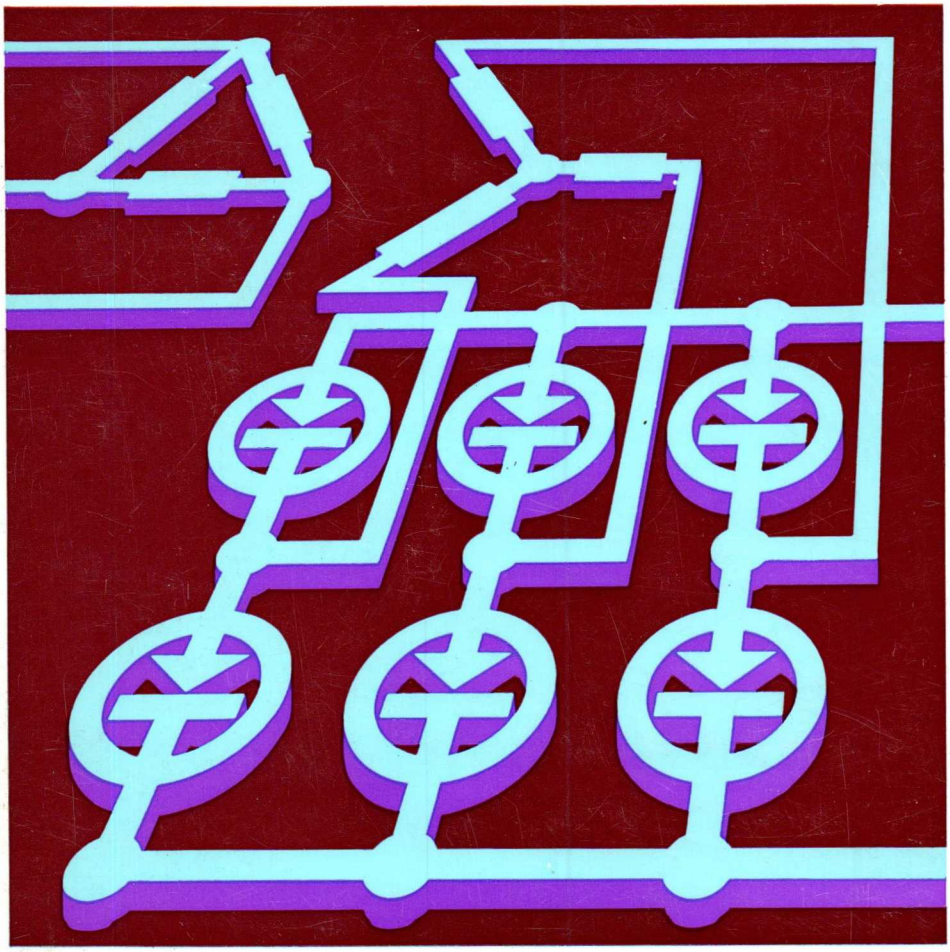
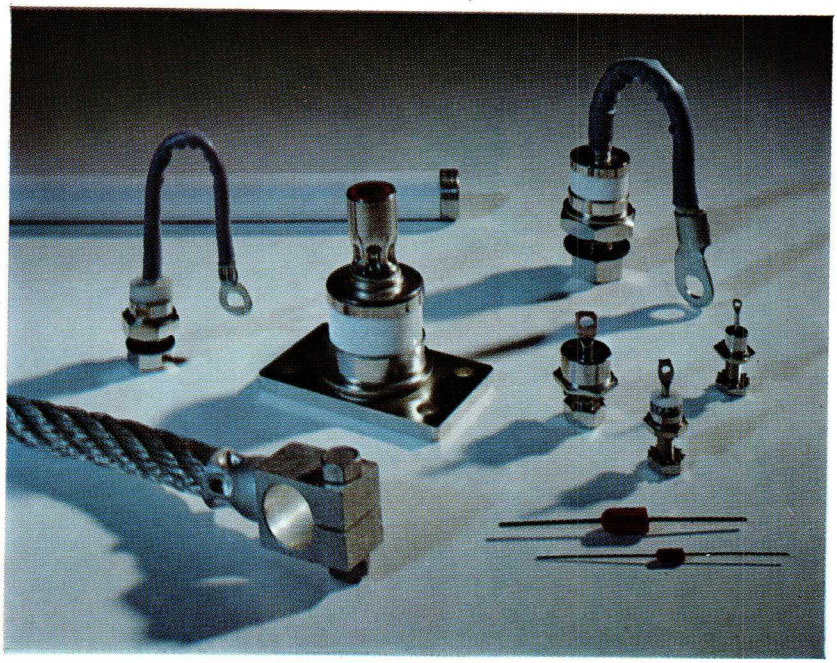
APPLICATION BOOK

ELECTRONIC COMPONENTS AND MATERIALS DIVISION

RECTIFIER DIODES



Rectifier Diodes



Rectifier Diodes

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ELECTRONIC COMPONENTS AND MATERIALS DIVISION

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Contents

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Why this book was written

Semiconductors have solved many of the old problems of power control, but they have also raised new ones with which some engineers are not yet familiar. In the ten years since we began selling rectifier diodes we have encountered most of them, either in the course of our own research and development activities or in working out power control applications for our customers. As a result, we know the answers to most of the questions users are likely to ask and we have tried to put them in this book.

Naturally, we cannot foresee all the applications in which our diodes may be used, and new applications may raise new problems. If they do, we are ready to help you solve them. Not only are the services of our application laboratories throughout the world at your disposal, but of our publications department too. As new applications are developed and new problems solved, it is our policy to publish information about them for our customers. If the answer to your power control problem is not in this book, please ask us about it. You can rely on our help.

IR. P. DE VOS

1 Semiconductor Diodes

1.1 Introduction

Electrical energy is most conveniently transmitted in the form of alternating current. However, there exist numerous uses of electricity (electroplating and other electrochemical processes, welding, traction) which call for d.c. power. It is here that convenient and efficient conversion of electric power from a.c. to d.c. becomes of primary importance. The first answer to the problem was the rotary converter; then, around the turn of the century, the mercury vapour rectifier came into general use. The solid state device made its appearance at a later date, in the shape of the copper oxide (about 1920) and the selenium diode (about 1930).

Weaknesses inherent in these devices were their relatively poor forward current and reverse voltage handling capabilities. After World War II the two-layer pn-germanium and -silicon diodes were introduced. These passed higher current densities, but the reverse voltage limitations remained. These limitations have largely been removed by the advent of three-layer germanium and silicon diodes — devices that might be said to be tailor-made to the requirements of high-power a.c. to d.c. conversion. The introduction of a third weakly doped, almost intrinsic layer greatly enhances reverse voltage handling capabilities without any loss of the current-carrying properties afforded by the heavily doped outer p- and n-layers. These three-layers diodes can pass hundreds of amperes and block hundreds of volts, and thus are ideally suited to employment in present-day high-level a.c. to d.c. conversion systems.

A power diode should:

— offer practically no resistance to current flowing in the forward direction, i.e. have a low forward voltage drop;
— present virtually an open circuit to current attempting to flow in the reverse direction, i.e. have only a small leakage current;
— permit a high current density;
— stand up to a high reverse voltage, and so reduce the need for cascading of devices and elaborate circuitry in high-voltage applications.

In addition, solid-state power diodes should be able to tolerate high junction temperatures, for it is on this that their load-carrying capacity depends.

Figures for the various types of rectifying elements are set out in Table 1-1[11]. It is clear that the three-layer devices most closely approach the ideal rectifying element. The silicon three-layer diode withstands a higher operating temperature and can thus have higher load ratings than its germanium counterpart.

The virtues of three-layer power diodes may be summarized as follows:

— *Minimum power loss*, since forward voltage drop and reverse leakage current are of a vanishing magnitude under normal conditions of operation. In addition, no heater power is required to operate the device.

— *Extreme compactness*, since permissible current density and reverse voltage are high.

— *Extreme reliability*. A virtually unlimited life may be expected, provided the diode is employed within the ratings. This cannot be said of thermionic rectifiers, for the life of the cathode is definitely limited.

In addition to these properties, the recently introduced controlled avalanche type of power diode has greatly simplified the problem of countering voltage surge effects. This device will withstand, bursts of reverse energy that would be apt to destroy conventional diodes by surface breakdown (see Section 2.3).

Table 1-1

rectifier device	forward voltage drop	current density (A/cm^2)	maximum reverse volt. (V)	maximum operating temp. (°C)	efficiency (% approx.)
rotary converter	—	—	—	—	90
mechanical rectifier	—	—	—	—	97
mercury vapour rectifier	15 to 20	–	20.000	≈ 45	95
copper oxide rectifier	~0.6	1	30	70	90
selenium diode	~1	1	50	150	90
germanium diode (three-layer)	0.5	100	~800	120	99
silicon diode (three-layer)	1	100	~4000	200	99

1.2 Semiconductor Material

1.2.1 General

In absolutely pure (intrinsic) silicon or germanium, electrons and holes (electron shortages) are generated by thermal motion. These charge carriers in the intrinsic material are able to move freely within the monocrystalline lattice, and so allow a current to pass through the crystal when a voltage is applied. Since, at thermal equilibrium, the concentration of intrinsic charge carriers is extremely low, the resistivity of the pure material will amount to several thousands of Ωcm, which makes the intrinsic semiconductor unsuited, as it stands, to any practical application. Of course, the intrinsic material has no rectifying properties anyway. The concentrations of thermally generated charge carriers increase with temperature within the normal operational range, and so also does the conductivity of the intrinsic material.

The intrinsic conductivity can be greatly improved by introducing strictly controlled amounts of selected impurities, that is to say, by doping with chemical elements similar to the element forming the crystal lattice. An impurity concentration as low as 1 in 10^8 is enough to reduce the resistivity of the pure material quite appreciably.

1.2.2 Donor and Acceptor Impurities

Phosphorus, for example, is a pentavalent element, and on diffusion into pure silicon or germanium, it will disturb the original lattice, this being built up out of tetravalent atoms. Each intruding phosphorus atom has one electron which will not fit into the lattice, and so becomes a mobile charge carrier. Because it donates negative charge carriers to the intrinsic material phosphorus is called a donor or n-type impurity. Arsenic and antimony are also donors. Almost all built-in donor atoms are ionized at room temperature. Having lost an electron, they acquire a positive charge which is held fixed within the crystal lattice. Silicon or germanium doped with a *donor-type* impurity is called n-type material because it passes a current consisting of *negatively* charged particles.

Amongst the acceptors or p-type impurities are boron, aluminium, indium and gallium, which resemble silicon and germanium, but differ from them in being trivalent. When introduced into intrinsic material, a p-type atom will not fit into the crystal lattice unless it captures an electron, thus leaving an electron shortage or hole. Thermal agitation causes captured electrons to be ejected from their bounds; however, they

are immediately accepted by other nuclei deprived of the corresponding electron. As a result, the electron shortages or holes behave as mobile carriers which are positively charged and which move in a direction opposite to the dislocated electrons. At room temperature almost all acceptor atoms are ionized. On collecting an electron they acquire a negative charge which is tied to the crystal lattice. Silicon or germanium doped with an *acceptor-type* impurity is named p-type material because of the *positive* charge carriers it contains.

When the impurities are evenly distributed over the intrinsic material we have a homogeneous semiconductor with improved current conduction properties. However, such a semiconductor still does not possess rectifying capabilities. It is important to note that electrical neutrality is maintained everywhere in the semiconductor material because the charge of the mobile carriers is fully compensated by the immobile space charge of the ionized impurity atoms.

1.2.3 Manufacture

Fig. 1-1 shows several stages in the manufacture of a diode (in this case a three layer type: see section 2.2). Successive stages of this process are shown schematically, assuming we start with central layers of weakly-doped p- and n-silicon. Formation of the outher n^+- and p^+-layers is a dual operation in which accurately controlled layer thicknesses are created by first depositing the impurity vehicle, and then driving in the impurities at a higher temperature.

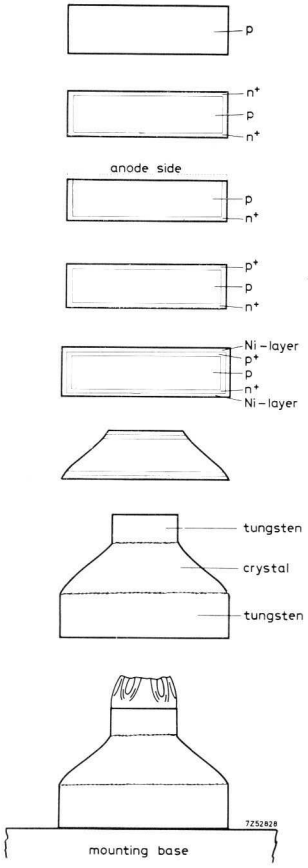
Processing in a superclean atmosphere ensures high electrical and chemical stability. Sandwiching the silicon crystal between molybdenum or tungsten back-up plates, greatly enhances the capability of the finished device to endure thermal fatigue. The solid back-up plates have a coefficient of thermal expansion close to that of silicon; any thermal stresses are thus transferred from the fragile silicon crystal to the joints between back-up plates and leads, enabling the unit to withstand severe temperature fluctuations without suffering electrical or mechanical deterioration. Selection of tungsten or molybdenum as back-up plate material ensures good electric and thermal conductivity. The silicon crystal is coated with rubber or varnish to obviate surface flash-over at rated voltage level and to protect the crystal from chemical attack. After coating the assembly is sealed, together with an inert gas to inhibit chemical action, into its envelope.

The envelope is the most seen and probably the least appreciated part

of any diode whereas it is the result of much development to endow it with the properties needed for it to perform all its functions. These functions include:

(1) protecting the crystal from handling and mishandling, humidity and chemical contamination;
(2) providing electrical and thermal conducting paths;
(3) presenting the diode in a manner convenient for mounting.

(1) These protective properties are obtained by making the envelope



Stage 1. High grade, weakly p-doped silicon crystal.

Stage 2. Deposition of P_2O_5 and diffusion of phosphorus.

Stage 3. Crystal anode-side is lapped to remove n^+-layer.

Stage 4. Deposition and diffusion of boron and anode-side *PeOe* layer at cathode-side prevents boron diffusion here.

Stage 5. Both sides are lapped to remove residual P_2O_5 and boron. Both sides are nickel plated for better contact.

Stage 6. Crystal edges are bevelled and junctions are etched (or and coated).

Stage 7. Tungsten back-up plates are soldered on to create a fatigue-free construction.

Stage 8. One side of entire assembly is brazed to Hexagon mounting base and to the other side the contact is connected.

Fig. 1-1 Power diode manufacturing technique all-diffusion method (crystal cross-sections shown, not to scale).

so robust that the hermetic seal, between the electrodes and glass or ceramic insulator still exists even after the diode has been subjected to all stresses associated with transport, normal handling, mishandling, mounting on a heat sink, and the vibrations or shocks experienced during operational life.

Further, the seal is able to suffer the expansions and contractions caused by different ambient temperatures and loads, and still be effective. All this is actieved with an envelope that is small enough to fit into modern power equipment.

(2) To provide good conductors for current and heat the envelope electrodes are made of copper, usually nickel plated to prevent their corroding in industrial atmospheres. In power diodes one of the electrodes is the mounting base and the cathode (reverse types the anode) is bonded directly to this base to give minimum electrical and thermal resistances between the junction and base. To keep the contact resistances between the base and heat sink as low as possible the mounting base surface is made smooth and flat.

(3) Lower power diodes have a stud type mounting base which makes for easy installation. The higher power diodes, however, have a flat base that can be either bolted or soldered to the heat sink to make the contact resistances even lower.

2 Phenomenology

2.1 Two-Layer Structure

2.1.1 The Unbiased State

An inhomogeneous piece of semiconductor material is obtained by introducing impurities at one side. This may be achieved by a diffusing or alloying process. It is clear that the impurity concentration is maximum nearest to the surface, the amount of impurities decreasing to almost zero with depth. When we diffuse p-type impurity into n-type material, the situation may be as depicted in Fig. 2-1. Near the surface the p-type impurity will predominate. Beyond a certain depth the original n-type material remains virtually unaffected by the diffusion process. At the level where the diffused impurity concentration equals that of the n-type material, i.e. where the net concentration is zero, a pn-junction is formed. As will be shown below, the device thus produced will have rectifying properties, passing a high current in one direction only; when the applied voltage is reversed, only a small leakage current flows.

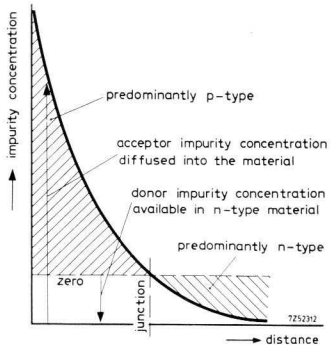


Fig. 2-1 The diffused pn-junction.

Impurity concentrations create mobile charge carriers which tend to diffuse evenly across the semiconductor material, like gas particles in a void space. Charge carriers diffuse away from regions of high density to those of lower densities; that is to say, a diffusion current is set up which is proportional to the concentration gradient (the decrease in concentration per unit length). This diffusion current upsets the electric charge balance within the semiconductor material, although the semiconductor

as a whole remains electrically neutral. The local space charges thus formed set up an electric field which counteracts the diffusion of charge carriers. A state of equilibrium will be attained when the diffusion current and the opposing current set up by the electric field are equal. As many charge carriers will diffuse to regions of lower concentration as are forced back by the opposing field. Clearly, a state of even distribution of charge carriers will never come into existence.

The slice shown in Fig. 2-2 illustrates in simplified fashion the state of equilibrium around the pn-junction. Majority carriers (holes in the p-layer, electrons in the n-layer) migrate across the junction by diffusion, thereupon becoming minority carriers (Fig. 2-2*a*). Their displacement upsets the local charge balance (Fig. 2-2*b*) and creates space charges on both sides of the junction (Fig. 2-2*c*). Thus an electric field is set up (Fig. 2-2*d*), having its maximum strength where the space charge reverses sign, i.e. at the junction. The space charges attract each other across the junction, whereas at the same time a diffusion current will cross the junction. This current is limited by the electric field. Since the storage of majority carriers on one side of the junction equals the excess of minority carriers that have crossed the junction, the two space charges will be of equal magnitude and opposite sign. The shortage of majority carriers and the excess of migrated minority carriers causes the p-layer to assume a negative potential with respect to the n-layer (the p-layer has a shortage of holes and an excess of electrons; conversely the n-layer has a shortage of electrons and an excess of holes), see Fig. 2-2*e*. As a result, the diffusion of mobile charge carriers sets up a potential difference, called the diffusion voltage, between the two regions. The diffusion voltage acts as a potential barrier opposing the migration of majority carriers and upholding the balance between diffusion current and field current. A steeper concentration gradient sets up a stronger diffusion current and thus creates a larger counteracting diffusion voltage to restore the balance between diffusion process and field effect. Thus, independent of the semiconductor material and the type of impurity, the diffusion voltage will be a function of the ratio of hole (or electron) concentrations existing on either side of the junction.

2.1.2 Forward Bias

Forward biasing of a junction makes the p-layer more positive (Fig. 2-3). Applying forward voltage will aid the diffusion or migration of majority carriers across the junction despite the potential barrier. Holes are in-

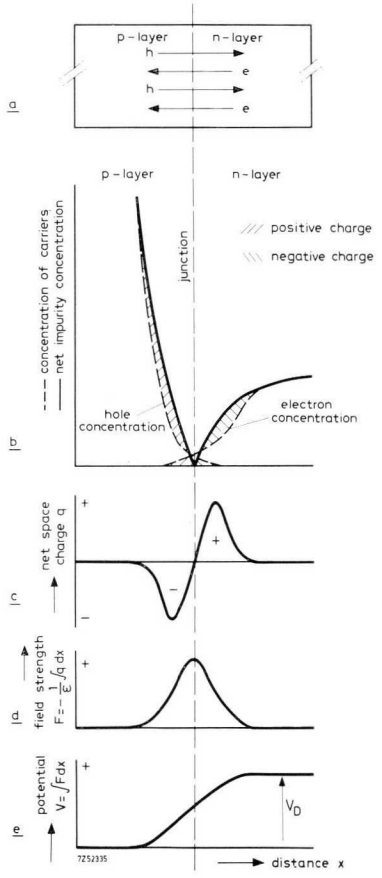


Fig. 2-2 Simplified representation of the equilibrium obtainable around the unbiased pn-junction.

a) slice from pn-diode junction
b) distribution of concentration of impurities and charge carriers
c) space charge distribution (width exaggerated)
d) electric field strength distribution
e) potential distribution

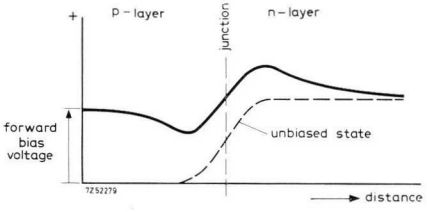


Fig. 2-3 Voltage distribution across forward-biased pn-junction

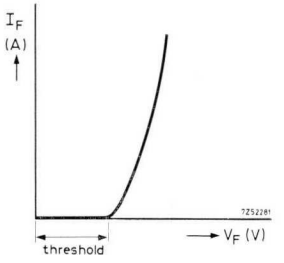


Fig. 2-4
Forward characteristic, pn-junction. (Threshold occurs approximately at diffusion voltage V_D, about 1 V.)

jected from the left, driving the holes already present in the material across the junction. The same applies to the electron current. The movement of carriers across the junction area is occasioned by the concentration gradient. Clearly, a minimum voltage is required to drive the majority carriers across the potential barrier. However, beyond this threshold voltage a small increase in potential difference is enough to push a much larger number of charge carriers across the junction. The forward characteristic of the pn-junction will accordingly be as shown in Fig. 2-4. Below the threshold voltage hardly any current flows, but once this threshold is exceeded a steep rise in forward current will result.

2.1.3 Reverse Bias

A pn-junction is said to be reverse biased when the p-layer is made more negative and the n-layer more positive. A reverse bias opposes the diffusion of majority carriers across the junction by increasing both the height and the steepness of the potential barrier (Fig. 2-5). Holes and electrons are attracted away from the junction area, which, if the reverse voltage is large enough, will be almost completely drained of mobile charge carriers; hence the name "depletion layer". The withdrawal of majority carriers increases both space charges and the width of the layer they occupy, so enabling a strong electric field to build up in response to the applied reverse voltage. Now, while the potential barrier opposes the flow of majority carriers, it acts as an "acceleration precipice" for the thermally generated minority charge carriers (cf. Section 1.2). Holes that have been thermally generated in the n-layer "fall" over the precipice, to be attracted by the negative voltage on the left-hand side; by a similar mechanism, electrons which have been thermally generated in the p-layer move across the junction into the n-layer.

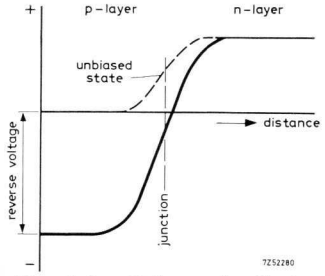


Fig. 2-5 Voltage distribution across reverse-biased pn-junction.

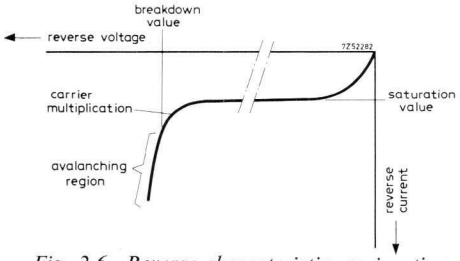


Fig. 2-6 Reverse characteristic, pn-junction.

These thermally generated minority carriers cause a reverse current to flow which is very much smaller than the forward current. The reverse current reaches a saturation value at a quite moderate reverse-bias voltage (Fig. 2-6) for there is a definite limit to the rate at which minority carriers can be generated thermally.

At very high reverse voltage levels the thermally generated minority carriers are strongly accelerated, thereby acquiring enough energy to enter into ionizing impacts. The resultant carrier multiplication increases the reverse current when the reverse voltage is raised to the "breakdown" level, the carrier multiplication factor is high enough to initiate an unlimited current rise. Avalanche breakdown will now occur, culminating in the complete destruction of the device if no current-limiting measures have been taken.

2.2 Three-Layer Structure

2.2.1 The Unbiased State

An important particular has been left out of the above simplified account. In reality both layers need heavy doping, so that they can supply an abundance of charge carriers. Besides making the diode suitable for high current densities, the heavy doping cuts down the voltage drop across both the p- and n-layer; but it also creates a strong concentration of both types of impurity in the junction area. There will therefore be a large number of minority carriers available (holes in the n-layer, electrons in the p-layer) to sustain a high saturation current, substantially lowering the voltage at which breakdown occurs. It would seem that high current densities are not compatible with a high blocking voltage — at least, in the simple two-layer diode structure. A way out of the dilemma is provided by the three-layer diode, which has a lightly doped central layer sandwiched between heavily doped p- and n-type outer layers. The central layer ensures a high breakdown voltage, the outer (contact) layers supply copious quantities of charge carriers, allowing high current densities to be sustained.

In effect the three-layer diode under forward bias, acts as a heavily doped 2 layer (p^+n^+) device, and under reverse bias as a highly doped 2 layer (pn^+) device.

In a three-layer device the semiconductor material has for example boron added as p-type impurity to one side of the crystal, forming a

p^+-layer. The other side is heavily doped with phosphorus, a donor which turns it into an n^+-layer. Sandwiched between these heavily doped layers is a central one which is scarcely affected by the diffusion process, and which retains the slightly p-type or slightly n-type character conferred on the purified silicon by evenly distributed residual impurities. The central layer must be thick enough to cope with a high reverse voltage, but still thin enough to be completely swamped with charge carriers originating from the outer, heavily doped p^+- and n^+-layers when a forward voltage is applied. Given the correct physical proportions, the intrinsic central layer, which normally has over 100 Ωcm resistivity, will be made highly conductive by the injected charge-carriers. The overall forward voltage drop across the structure is then reduced to a minimum. The required thickness of the central layer depends on the penetration depth (diffusion length) of the injected majority carriers, that is to say, on the average effective distance over which these carriers will travel before they recombine with charge carriers of opposite polarity.

With p-type silicon the situation prevailing in the unbiased state is depicted in Fig. 2-7. Majority carriers migrating from the heavily doped layers across the junctions, as shown in Fig. 2-7*a*, set up space charges on both sides of these junctions (Fig. 2-7*b*). (To simplify matters, we shall ignore the majority carriers migrating from the central layer; their concentration is much lower anyway.) The space charges create electric fields (Fig. 2-7*c*), which have their maximum strength at the junction interfaces and which restore the balance between diffusion effects and field current. The resulting build-up of potential barriers across the junctions hinders the migration of majority carriers (Fig. 2-7*d*). In the central p-layer the hole concentration is in excess of the electron concentration. Thus, as the concentrations of majority carriers in the outer p^+- and n^+-layers must be equal, the hole concentration gradient across the p+p-junction must be smaller than the electron concentration gradient across the n+p-junction. In consequence, the lowest diffusion voltage will develop across the p+p-junction (cf. Section 2.1.2).

2.2.2 Forward-Bias

Low-level injection

Injection is considered to be at a low level so long as the concentration of the injected carriers is less than the thermal-equilibrium value for majority carriers in the central layer. This situation prevails when the

diode is operated at moderate current densities (up to 10 A/cm^2). The low-level injection of holes from the p$^+$-layer will have no great effect on the concentration of majority carriers (holes) in the central layer, and the voltage drop V_{D1} across the p$^+$p-junction will scarcely change. (Fig. 2-8.)

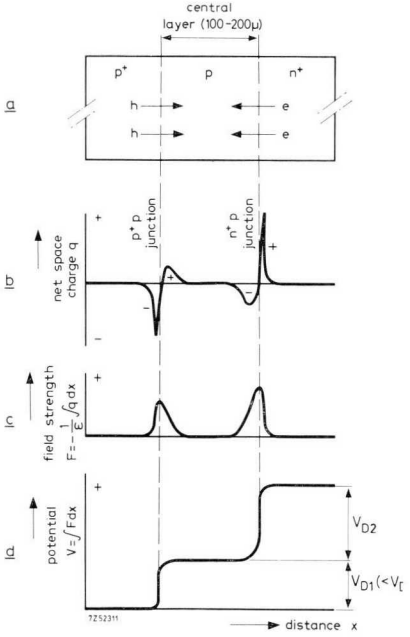


Fig. 2-7 Simplified representation of three layer diode: a) slice through diode perpendicular to plane of junctions, b) space charge, c) field strength, d) potential.

On the other hand, the injection of electrons from the n$^+$-layer substantially increases the concentration of minority carriers (electrons) in the central layer, causing the voltage drop across the n$^+$p-junction to diminish. It can be said that low injection levels do not appreciably alter the potential distribution through the central layer; in particular, the situation across the p$^+$p-junction remains almost unaffected. This implies that a zero voltage drop is maintained through the central layer, as in the unbiased state, while the properties of the diode are largely determined by the n$^+$p-junction. The device functions in fact as a two-layer diode.

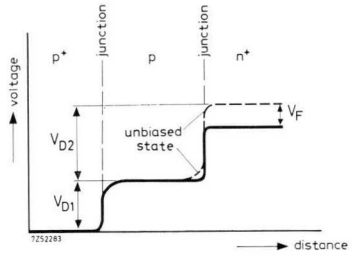


Fig. 2-8 Voltage drop across moderately forward biased three-layer diode (low-level injection). V_F = forward bias voltage.

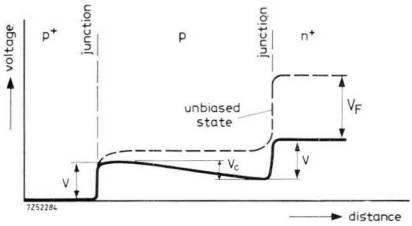


Fig. 2-9 Voltage drop across strong forward-biased three-layer diode (high-level injection).

High-level injection

Injection is said to be at a high level when the concentration of the carriers injected from both heavily doped layers exceeds the concentration of majority carriers in the central p-layer. This situation will arise when the diode is operated at higher current densities (10 to $>$ 100 A/cm^2), to beyond full steady-state load. The central layer is virtually swamped with carriers and becomes highly conductive, so that the low thermal-equilibrium carrier concentrations cease to play any part. Majority carriers are injected at the same rate from either side, so evening off the voltage drops across the two junctions (V in Fig. 2-9). Between the two junctions a voltage drop V_c develops, of a magnitude sufficient to drive large quantities of carriers through the central layer. This voltage drop must be compensated by an increase in forward voltage if the forward current is to remain at the same level. Under these conditions the number of majority carriers originally available in the central layer diminish and the device operates as a diode with an intrinsic central region (PIN-diode). As Fig. 2-10 shows the slope of the I_F-V_F curve falls off at high injection levels.

2.2.3 Reverse-Bias

The situation prevailing in the reverse-biased state is depicted in Fig. 2-11, and the effect of reverse biasing at various levels up to the maximum permissible level is shown in Fig. 2-12. A moderate reverse bias gives rise to internal voltage drops (Fig. 2-11) very similar to those arising in the case of low-level injection in the forward biased state (cf. Section 2.2.2). On increasing the reverse bias a more or less thorough clean-up of the central layer occurs caused by charge carriers at the junctions being

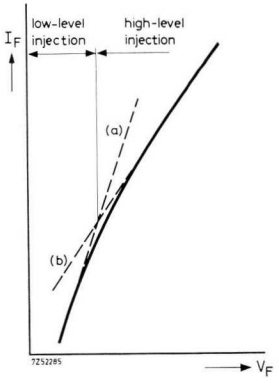


Fig. 2-10 Forward characteristic of three-layer diode compared to those of (a) 2-layer diode, and (b) PIN diode.

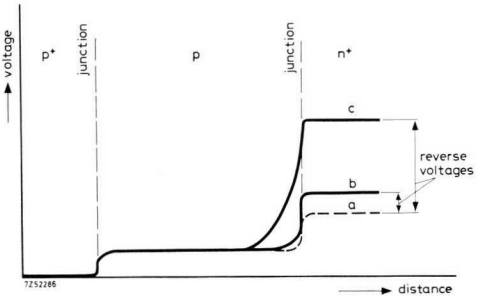


Fig. 2-11 Voltage drop across moderately reverse-biased three-layer diode: (a) unbiased state, (b) reverse bias — some tenths of a volt, (c) reverse bias — some volts.

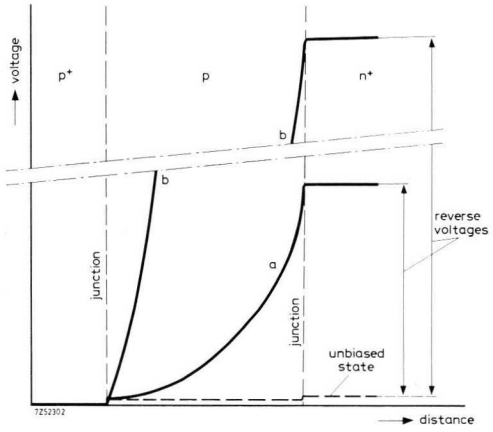


Fig. 2-12 Voltage drop across strongly reverse-biased three-layer diode.

attracted towards, and entering, the outer p^+- and n^+-layers (Fig. 2-12, curve *a*). The central layer is now dominated by acceptor ions which are evenly distributed and so constitute a negative space charge of uniform density. The resulting electric field increases linearly through the central layer so that the potential distribution is roughly parabolic. The negative space charge is unable on its own to support the steeper field gradient required by a further increase in the reverse bias; and in this eventuality, ohmic losses originating from the reverse leakage current, will develop through the central layer, giving rise to a linear potential distribution (Fig. 2-12, curve *b*). As in the high-level injected forward-biased mode of operation, the behaviour of the device under a strong reverse bias is very similar to that described in Section 2.2.2 for high level injection.

In very pure semiconductor material, any junction breakdown will occur as a result of avalanche effects caused by carrier multiplication [2]. The junction is apt to breakdown at lattice imperfections such as dislocations, and substantially higher breakdown voltages can be obtained from dislocation-free material. Hence, in order to arrive at a power diode that will stand up to really severe reverse biasing, the manufacturer must make every effort to avoid the irregularities present in the original crystal lattice and to even out the distribution of impurity concentrations. The junctions must be regular in structure and extend right up to the edge of the crystal.

It has been found that for silicon, provided the central layer has a thickness not less than that of the space-charge layer, at breakdown the following relationship exists between the breakdown voltage $V_{(BR)R}$ and impurity concentration N_1 in the central layer: [1]

$$V_{(BR)R} \propto {N_1}^{-0.75}.$$

Thus, with the purest material obtainable, in which N_1 is less than 10^{13} atoms/cm^3 (about 1 impurity atom for every 5×10^9 silicon atoms!) it is possible to achieve breakdown voltages of several thousand volts (Fig. 2-13). However, the carrier lifetime in the finished device is more difficult to control. Though silicon crystals can be produced with high carrier lifetimes, these are drastically reduced during diffusion processes. The relationship between breakdown voltage and carrier lifetime is shown in Fig. 2-14, for equal central layer thickness and carrier diffusion length.

In the case of p^+p-diodes the relationship above is not strictly true. In fact the breakdown voltage is lower, but carrier lifetime in the finished device is still of major importance. The reverse mode performance of power diodes has been stepped up by minimizing lifetime degradation

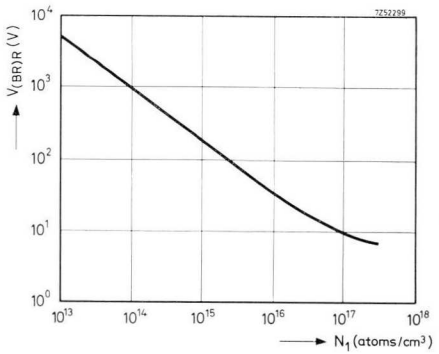


Fig. 2-13 Reverse breakdown voltage $V_{(BR)R}$ as a function of impurity atom concentration N.

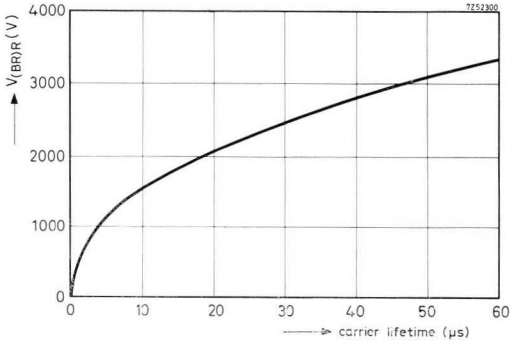


Fig. 2-14 Reverse breakdown voltage as a function of carrier lifetime.

during manufacture; however, if lifetimes of 1000 μs could be maintained, it should be possible to operate diodes at voltages between 5 and 10 kW.

The three-layer diode constitutes a major step forward as compared to earlier devices, and is nowadays widely accepted as a valuable tool in high-power rectification.

2.3 Controlled Avalanche Diodes

2.3.1 What does "Controlled Avalanche" mean?

Normally diodes are capable of momentarily absorbing hundreds of watts in the *forward* direction. However, in the *reverse* mode they may be damaged by only a few watts of power dissipation, occurring for example during a brief voltage transient. The reason for this contrast lies in the fact that, in the forward direction, the heat generated is distributed evenly across the crystal, whereas in the reverse mode, heat production is strictly

local. At high reverse voltage levels breakdown will occur at weak spots close to the junction-surface interface rather than across the whole crystal. Breakdown causes hot spots due to power dissipation within a minute volume; the structure of the semiconductor may be disrupted at these points. The energy that can be absorbed in this manner is extremely difficult to predict, though it is definitely less than the amount that can be dissipated through the full crystal cross-section.

In controlled avalanche diodes, however, the local electric field is kept under control by carefully contouring the semiconductor surface. Body breakdown will occur rather than surface breakdown.

As always, it is important that the crystal lattice should possess extreme regularity, and that the impurities should be evenly distributed, in order that a uniform and true avalanching effect may be obtained across the entire junction area. Such avalanching, when kept within acceptable energy limits, is of a non-destructive nature.

The voltage at which avalanching occurs is predetermined during manufacture by accurately dosing impurity concentration in the junction areas, and by careful attention to the geometry of the diode.

Controlled avalanche diodes are characterized by the following properties:

— rigidly specified maximum and minimum avalanche characteristics with overlapping voltage regions from type to type;
— within the ratings laid down in the data sheets, power surges in the avalanche region are absorbed without damage;
— sustained avalanche is possible without damage.

2.3.2 Effect of Bevelled Edges

The geometry of the diode plays a very important part in determining the characteristics of the controlled-avalanche diode. The effect of a large reverse bias on a p^+n-junction with bevelled edges is shown in Fig. 2-15,

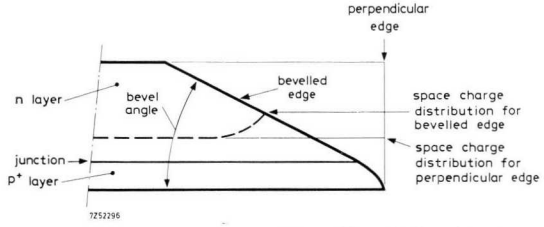


Fig. 2-15 Strongly reverse-biased bevelled pn-junction.

from which it will be seen that the space charge layer bends upward near the bevel. Consequently the width across which the potential barrier develops will be much larger at the edge than deep in the interior, giving rise to a reduced electric field intensity at the bevelled edges. Clearly, when the reverse voltage is raised, the diode will breakdown internally, leaving the edge of the crystal unaffected. This action excludes the highly unpredictable and unreliable phenomena which take place at the edges at high reverse voltage levels. In fact, the breakdown is transferred towards the interior of the crystal, where its properties can be accurately kept under control during manufacture.

The maximum field strength occurring along the bevel of the crystal will reduce as the bevel angle is decreased; however, technological considerations set a lower limit to the bevel angle.

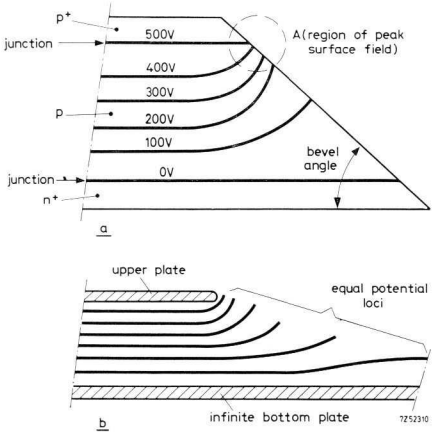
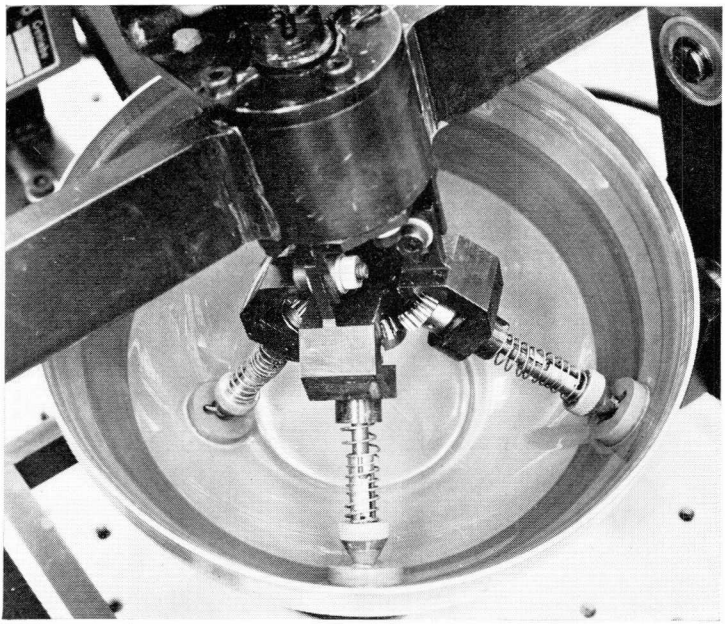


Fig. 2-16 (a) Strongly reverse-biased bevelled three-layer diode, and (b) the capacitor equivalent.

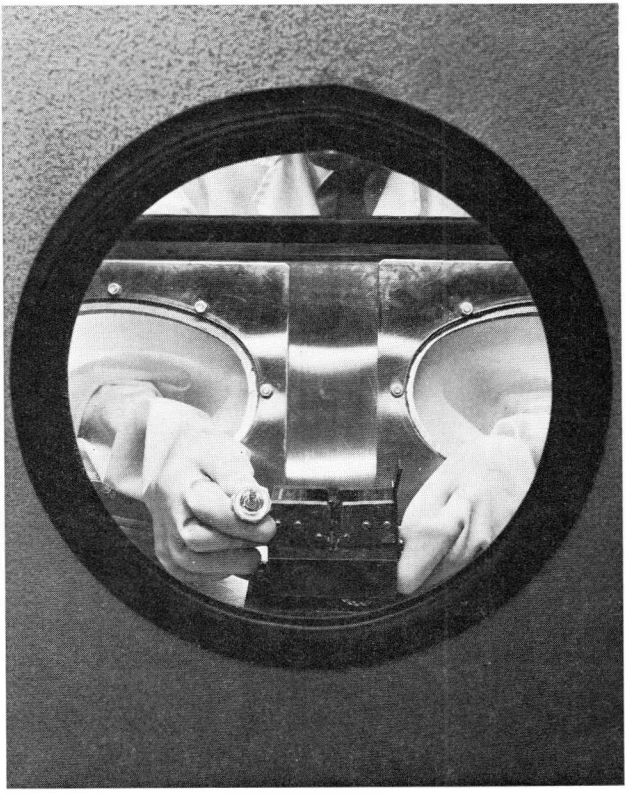
The effect of bevelling a three-layer diode is illustrated in Fig. 2-16, together with its capacitor equivalent (plate of restricted dimensions facing infinite plate). At low reverse bias, when the depletion layer has not yet extended into the p^+-layer (cf. Section 2.2.3), the system acts as a simple bevelled n^+p-junction. At a high reverse bias, however, the space charge reaches the p^+-layer, and the voltage distribution will crowd around the p^+p-junction edge (area *A*). (At a low reverse bias the maximum space charge develops just above the n^+p-junction, as in a diode with a single

junction, but as the reverse bias increases, the peak in the field strength shifts towards the p^+p-junction.) In fact, the field configuration resembles that around the edge of a finite capacitor plate placed opposite a plate of infinite dimensions. This local field is controlled by the edge radius. Similarly, the maximum field strength at the edge of the p^+p-junction is governed by the bevel angle. By careful choice of the bevel angle, the maximum field at the edge can be significantly reduced, though not to the same extent as in a two-layer diode.

Having a built-in mechanism for handling voltage surges, the controlled avalanche diode greatly simplifies circuit protection and other design problems. It is quite capable of absorbing bursts of power due to abrupt switching, fuse blowing and the like, and of doing so within its ratings. Unlike other diodes, controlled-avalanche diodes do not invariably require the protection of voltage-sharing resistors and capacitors when connected in series. Thus the main advantage they offer is enhanced circuit reliability with simplified design.



Bevelling the wafer edge of controlled avalanche diodes.



Diode assembly in clean work cabinets filled with inert gas.

3 Characteristics and Thermal Considerations

3.1 Power Diode Characteristics

Power diode data sheets usually give current versus voltage curves in both the forward and the reverse directions, as well as power dissipation versus average forward current. These graphs, in conjunction with the non-repetitive ratings, indicate the optimum operating conditions for the devices and keeping within the limits laid down ensures the highest reliability. In the case of continuous duty, limiting factors are maximum average forward current and crest working reverse voltage. For sinusoidal operation between 50 and 400 Hz, the forward and reverse losses largely determine the overall dissipation, the forward losses being the major contributor. However, reverse losses are by no means negligible, since they tend to increase with temperature, and may thus cause thermally unstable operation (junction temperature run-away). Beyond 400 Hz, switching transient dissipation due to reverse recovery may reach significant levels.[3]

Non-repetitive or surge ratings are determined by the diode ability to absorb power surges, and these ratings are the ones which may even dictate the choice of diode.

3.1.1. Forward Characteristics

The operation of the three-layer diode in the forward-biased state has been considered at some length in Section 2.2.2. Figs 3-1 and 3-2 show, in schematic form, forward characteristics of such a diode under steady and surge load conditions. At low power levels, where the current flow is essentially injection-limited, the diode operates as a single-junction device. With increasing forward bias (high-level injection) the conductivity of the central layer improves and starts to resemble that of a PIN-diode. (Fig. 3-1.) Within the continuous load region up to about 100 A/cm^2 the slope of the $\log I_F$ versus V_F characteristic may be expressed as q/akT, where $1 < a < 2$, average 1.6. In the region that includes the repetitive peak values and extends right up to the maximum surge limits, carrier concentrations in the central layer approach those in the p^+- and n^+-layers (very high level injection) and it becomes increasingly difficult to extract, across the central layer, carriers from the heavily doped outer

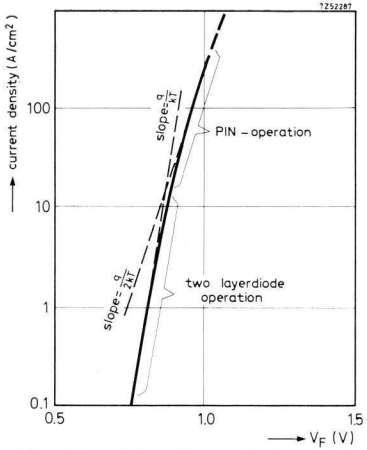


Fig. 3-1 Three-layer diode steady state forward characteristic.

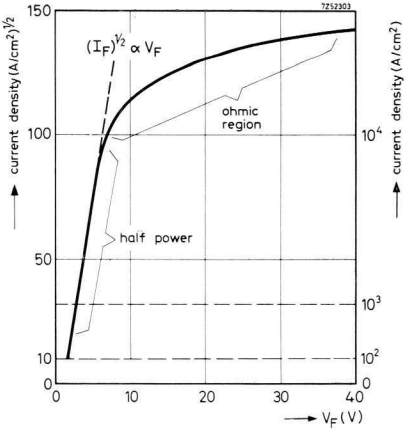


Fig. 3-2 Forward characteristic of three-layer diode under surge conditions.

layers. At these levels the current flow becomes space-charge limited,[4] and will be governed by the half-power law.[1],[5],[6],[7] Beyond this region the diode seems to behave as an ohmic device and no significance should be attached to measured results since they are highly dependent on conditions.

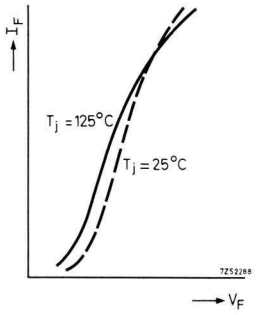


Fig. 3-3 Influence of junction temperature on forward characteristics of power diode BYX14.

Fig. 3-3 shows forward characteristics for the 150 A power diode Type BYX14 at two different junction temperatures. It will be seen that a rise in operating temperature reduces the forward voltage drop for currents

within continuous load ratings (up to 150 A average). This temperature-dependent phenomenon is turned to good account when the rise in junction temperature due to pulse loading is determined by monitoring the forward voltage drop at an extremely low standing forward current (cf. Section 3.2.3).

The forward characteristic is independent of time in the sense that the dynamic and static forward characteristics do not differ.*

The forward current, in conjunction with the forward voltage drop, occasions a loss of power within the diode which raises the junction temperature. The maximum permissible junction temperature determines the maximum forward power dissipation (the reverse losses being almost negligible). This in turn sets a limit to the average forward current,

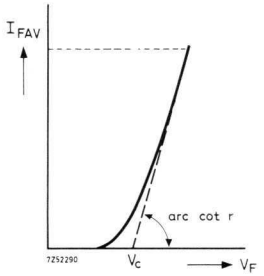


Fig. 3-4 Determination of forward power loss.

though the diode is capable of carrying currents far in excess of this value. The forward power loss can be determined from Fig. 3-4 with the aid of the formula:

$$P_{FAV} = V_c I_{FAV} + I_{F(\mathrm{rms})}{}^2 r_{\mathrm{diff}}, \qquad (3\text{-}1)$$

where P_{FAV} = average forward power dissipation,
I_{FAV} = average forward current,
$I_{F(\mathrm{rms})}$ = r.m.s. forward current,
V_c = voltage given by the intercept of the tangent with the abscissa,
r_{diff} = differential (a.c.) resistance determined by the average forward current level.

Taking as an example diode Type BYX14, operating at full rating, with

* This not entirely true in switching circuit applications, where recovery effects are likely to occur (cf. Section 3.1.3).

180° conduction angle, we find $V_c = 0.9$ V, $I_{FAV} = 150$ A, $I_{F(\text{rms})} = 1.57 \times 150 = 235$ A, $r_{\text{diff}} = 1.2$ mΩ, which gives

$$P_{FAV} = 0.9 \times 150 + 235^2 \times 0.0012 = 201 \text{ W}.$$

The actual power dissipation versus average forward current characteristic is shown in Fig. 3-5. It will be noted that a significant amount of power may be dissipated across the diode junctions, so cooling is necessary to keep the junction temperature within safe limits.

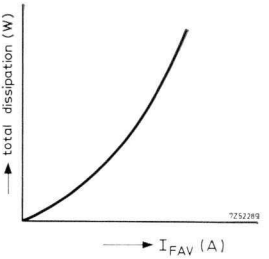


Fig. 3-5 Forward power dissipation as a function of average forward current (BYX14 series).

3.1.2 Reverse Characteristic

When the diode is reverse-biased, a leakage current flows. The leakage current has two components. One component is the saturation current, which is made up of thermal equilibrium carriers freed in the depleted central layer and which reaches a maximum at a relatively low reverse voltage (cf. Section 2.1.3); the saturation current is negligibly small in silicon. The other component is the "generation" current, due to carriers captured and released at trapping centres within the space charge region of the junction. The ratio between the currents generated inside and outside the junction space charge layers is 0.1 for a typical germanium junction; it can be as high as 3000 for silicon.[11] Clearly, the generation current is by far the major contributor to the overall leakage current in silicon diodes.

A generalized curve for reverse-biased junctions, plotted on a log-log scale, is shown in Fig. 3-6. In the generation current range, I_R is a half-power function of the reverse voltage.[11] At higher reverse voltage levels carrier multiplication will occur, giving an appreciable increase in reverse current. Avalanching, resulting in general breakdown, will ensue if the reverse bias is further raised.

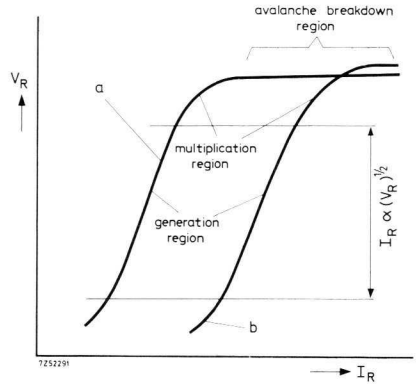


Fig. 3-6 Influence of temperature on generalized reverse-bias characteristic: (a) room temperature, (b) high operating temperature.

As shown by Fig. 3-6, the reverse current is strongly temperature-dependent and will rise by a factor of about 2 for every 10 to 15 degC increase in temperature. The relation between leakage current and temperature is expressed as:

$$i_1 = i_0 \cdot \exp\{c(T_1 - T_0)\}, \tag{3-2}$$

where i_0 = leakage current at junction temperature T_0,
i_1 = leakage current at junction temperature T_1,
c = temperature coefficient (0.03 to 0.07 per degC).

The reverse losses are proportional to the leakage currents; thus, from eq. (3-2):

$$P_1 = P_0 \exp\{c(T_1 - T_0)\}, \tag{3-3}$$

where P_0 = reverse losses at T_0
P_1 = reverse losses at T_1.

The temperature dependence of reverse losses may cause thermal instability (cf. Section 3.2.1) in badly designed circuits.

Fig. 3-7 shows the reverse characteristic for the BYX27 series of controlled avalanche diodes at a junction temperature of 25 °C. Besides being subject to production spread, the avalanche breakdown voltage has a temperature coefficient of about 0.001. The formula is:

$$V(T) = V_{T=25}\{1 + 0.001(T - 25)\}, \tag{3-4}$$

where $V(T)$ denotes the avalanche voltage at a junction temperature of T °C.

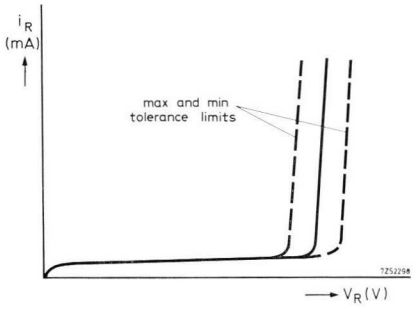


Fig. 3-7 Reverse characteristic at 25 °C of controlled avalanche diode series BYX27.

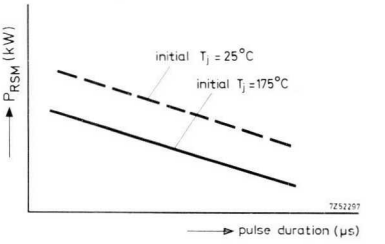


Fig. 3-8 Non-repetitive peak reverse power as a function of pulse duration, BYX27 series.

Though the controlled avalanche diode, in contrast to other diodes, can safely operate close to or within the breakdown region, a crest working reverse voltage rating is specified in the data sheets in order to ensure that it can withstand the full reverse voltage during steady-state operation, at minimum avalanche voltage and at lowest rated junction temperature (−55 °C).

The non-repetitive power surge curve for the same series is shown in Fig. 3-8 for two initial junction temperatures, and various pulse durations (rectangular pulses). It will be seen that in the reverse mode, by virtue of even heat distribution across the crystal, power bursts can be absorbed which are approximately equal to those the device can cope with in the forward-biased state. The power dissipated in the reverse mode is expressed as: [8]

$$P = A(T_{jNR} - T_j)t^{-1/2}, \tag{3-5}$$

where A = diode constant,
T_{jNR} = non-recurrent rated peak junction temperature due to the power surge,
T_j = junction temperature before application of the power surge,
t = duration of the rectangular pulse.

Since T_{jNR} is well above the steady-state rating, the reverse power surges implied by Fig. 3-8 are essentially of a non-repetitive nature.

3.1.3 Recovery Effects

When a power diode is switched from the conducting to the non-conducting state or vice versa, it does not immediately settle down to steady-state operation. The switching action of the diode sets up transients which, provided electric parameters do not vary, give rise to a constant amount of energy loss per switching cycle. Under these circumstances the transient power loss will increase in proportion to the switching frequency, and may become a significant contributor to overall power dissipation at high frequencies, making derating of the diode necessary.

Forward recovery

The situation that arises when the diode switches to the conducting state is illustrated in Fig. 3-9. A finite time will be required to swamp the central layer with minority carriers so that it will become highly conductive. Thus the rate of current growth will not be infinite and a voltage in excess of the steady-state value will develop across the diode. The peak value of this forward recovery voltage depends both upon the rate of current growth as determined by the external circuit, and the final value of the forward current.

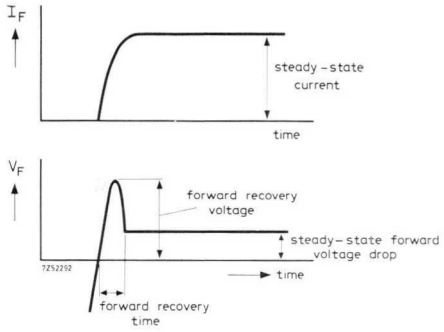


Fig. 3-9. Forward recovery (idealized).

The duration of the transient, termed forward recovery time, is generally small with respect to the reverse recovery time. Normally the power loss during forward recovery is also much lower than during reverse recovery. Thus forward transients do not pose a serious problem.

Reverse recovery

On application of a reverse voltage, the diode is unable to return immediately to the reverse-biased state. The abundance of charge carriers in

the central layer sets up a potential distribution which cannot change instantaneously. The charge in the central layer has to be cleared away by recombination and diffusion of the carriers. Accordingly, during time t_1 (Fig. 3-10) the forward voltage drop is maintained although the diode current has reversed under the influence of the external voltage.). As soon as the charge has been removed, the reverse current decays, allowing the potential barrier to be built up. The full ability to withstand the reverse voltage is not restored until the leakage current has fallen to its steady-state value.

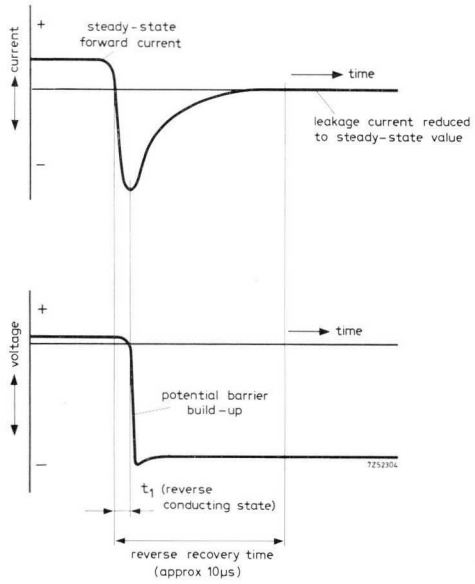


Fig. 3-10. Reverse recovery.

Both the reverse current surge and the reverse recovery time depend on the forward current, rate of decay of forward current, and the reverse voltage. Reverse recovery will be slowed down in the absence of a reverse voltage, since then no potential drop is present across the diode structure to aid extraction of the excess charge carriers. The reverse current surge is a result of two actions: one the removal of excess charge carriers, the other charging-up of the depletion layer capacity.

The reverse current flowing during the build-up of the potential barrier is comparatively heavy, and it is responsible for the greater part of the losses associated with the reverse recovery process. These losses increase

both with forward current and with frequency. Though considerably larger than the forward recovery losses, they can still be neglected at normal line frequencies.

3.1.4 Surge Characteristics

A semiconductor is said to work on a repetitive basis when its maximum junction temperature does not exceed the rating laid down for continuous duty. It works on a non-repetitive basis when the junction temperature exceeds the maximum (continuous) rating for a brief instant, i.e. when it is "overloaded" within the ratings laid down by the manufacturer. This mode of operation covers unusual phenomena such as inrush currents, fault currents due to shorts, heavy switching and lightning strokes on power lines. It is on this kind of role that the power diode comes into its own as a rectifying device capable of absorbing power bursts well beyond continuous ratings. In many instances, in fact, selection of a particular diode is governed not so much by continuous load considerations as by the power surges that are expected to occur in the application.

Non-repetitive operation is subject to the following provisos:

— the diode must always be operated within the relevant ratings as specified in the data sheets;

— the load levels implied by the specified non-repetitive ratings must occur only a limited number of times during the life of the diode;

— the permitted overloads must not occur in quick succession. The junction must have an opportunity of cooling down to at least the maximum temperature permissible for continuous duty before it is again overloaded up to the permitted overload level. This proviso caters for the case were power surges — due for example to shorting — have to be absorbed by a diode that is already working under full steady-state load conditions.

Adherence to the above rules will prevent any deterioration in diode characteristics, and so ensure reliable operation.

Ratings for non-repetitive duty are determined by the surge current curve and the I^2t diagram. A typical surge current curve is shown in Fig. 3-11, in which the maximum permissible peak (half sine wave) forward current is plotted against the number of half sine waves at 50 Hz operation. The current pulses are assumed to have the same amplitude and to be separated by half cycle "off" times. Suppose a short-circuit persists over 5 cycles (duration 0.1 s); the diode will be able to absorb

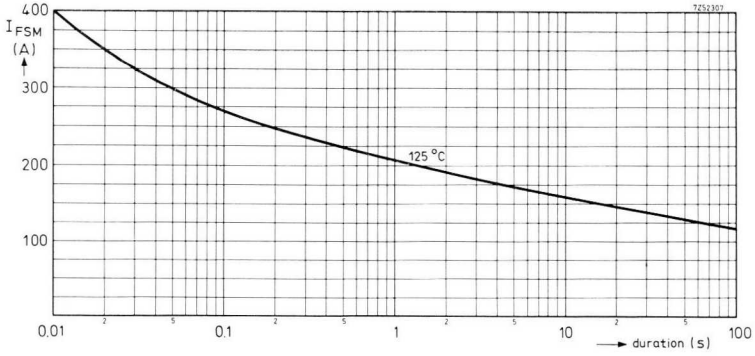


Fig. 3-11 Surge current curve for BYX13 series, allowing for maximum rated junction temperature prior to the surge.

5 half sine waves having a peak value of 270 A (T_{mb} = 125 °C) and a duration of 10 ms, provided they are separated by 10 ms intervals. Note that this type of surge is permissible under full load conditions.

I^2t-ratings apply to *subcycle* surges, i.e. single surges lasting less than 10 ms. Over such short periods of time the diode behaves essentially like a resistor with a fixed thermal capacity and with no heat bleed-off from the junction area while the surge current is flowing. What is important here is the total amount of transient energy dumped into the junction area; this may be represented in good approximation by the time integral (I^2t) of the square of the forward current. The safe I^2t-value is lower for subcycle surges than for overloads lasting 10 ms and more, because in the latter case the heat has a chance to flow away from the junction during the overload, thus limiting the junction temperature rise. I^2t-ratings are of interest when power diodes are being operated with fuses to protect them (see Chapter 7).

The following formula relates the maximum permissible peak value of a 10 ms half sine wave current surge to the steady-state average current rating. In general:

$$I_{FSM\ max}/I_{FAV\ max} = 16 \text{ to } 20. \qquad (3\text{-}6)$$

3.2 Thermal Considerations

3.2.1 Thermal Stability

The thermal working condition of a power diode is dictated by the simple

law of thermal equilibrium, stating that heat fed into the diode and heat removed must be equal. However, fulfilment of this condition does not necessarily imply thermally stable operation. Even when the cooling system is capable of draining off all heat supplied, a situation of thermal instability can still arise. This is due to the temperature dependence of the reverse losses, which increase with junction temperature (cf. Eq. 3.2). The system becomes thermally unstable when the amount of power supplied to the junction per degree centigrade starts to exceed the amount of heat removed per degree centigrade. Unless arrested, the resulting upward drift in junction temperature will eventually cause the diode to break down. Normally, however, the temperature dependence of the forward losses can be left out of the account. The condition for thermal stability can then be formulated as:

$$dP_{RAV}/dT_j < dP_A/dT_j, \tag{3-7}$$

where P_{RAV} = average reverse power dissipation (heat supplied to the junction),
P_A = power removed from the junction,
T_j = junction temperature.

The removal of heat depends on the overall thermal resistance $R_{th\ j-a}$ of the conduction path from junction to ambient. $R_{th\ j-a}$ comprises the thermal resistance from junction to mounting base and, if a heat sink is used, the thermal resistance from mounting base to heat sink and heat sink to ambient. This thermal resistance may be expressed:

$$R_{th\ j-a} = \Delta T_j/\Delta P_A = (T_j - T_{amb})/P_A. \tag{3-8}$$

With the aid of eq. (3-3) condition (3-7) can be expressed in terms of $R_{th\ j-a}$. Substitute P_{RAV} for P_1 and T_j for T_1 in eq. (3-3):

$$P_{RAV} = P_o \exp c(T_j - T_o).$$

Differentiating with respect to T_j gives:

$$\frac{\mathrm{d}P_{RAV}}{\mathrm{d}T_j} = cP_o \exp c(T_j - T_o),$$

and so:

$$\frac{\mathrm{d}P_{RAV}}{\mathrm{d}T_j} = \frac{1}{cP_{RAV}}.$$

Now, for thermal stability, using eq. (3-7):

$$\frac{dP_{RAV}}{dT_j} \leqslant \frac{dP_A}{dT_j},$$

thus:

$$cP_{RAV} \leqslant \frac{1}{R_{th\ j-a}},$$

or

$$R_{th\ j-a} \leqslant \frac{1}{cP_{RAV}}. \tag{3-9}$$

This condition for thermal stability must be met at maximum junction temperature and at the highest anticipated leakage current with the diode subjected to the crest working reverse voltage. The maximum permissible external thermal resistance can be derived from the data sheet.

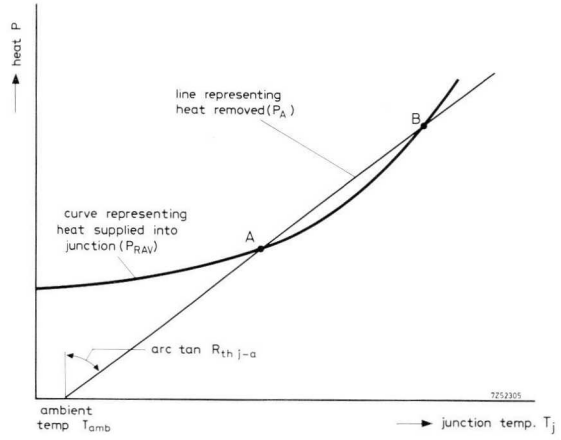


Fig. 3-12 Thermal stability: (a) unconditional, (b) conditional.

The thermal behaviour of a diode is illustrated graphically in Fig. 3-12. The relevant curves intersect at two working points, *A* and *B*, meaning that at these points the heat generated equals the heat removed. At *A*, condition (3-6) is satisfied, ensuring unconditionally stable performance of the diode; the system will return to point *A* after any disturbance of

the thermal equilibrium. At point B the system does not satisfy condition (3-6). Operation at this point will be stable only on condition that the heat balance is not disturbed. Any slight increase in power dissipated will cause thermal runaway, since beyond this point the heat cannot be removed at the same rate as it is produced. There will be no limit to the rise in junction temperature, and the diode is apt to be destroyed by an avalanche effect.

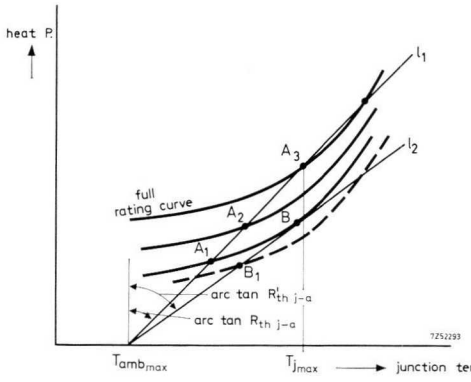


Fig. 3-13 Effect of a cooling system on thermal instability. l_1 = correctly designed system, l_2 = inadequate cooling system.

The practical situation is depicted in Fig. 3-13. Diode heating is represented by a plot of curves relating to different values of forward current. Straight lines l_1, l_2 represent the cooling effect provided by two different heat sinks. The cooling system represented by l_1 will stabilize the junction temperature at points A_1, A_2, A_3 under various loads, and at the maximum anticipated ambient temperature $T_{amb\ max}$. Even at full rating (point A_3) unconditionally stable performance is ensured. With inadequate cooling, however, stable operation is possible only up to point B. Such conditions will preclude full utilization of the diode, the excessive resistance of the external thermal path having pushed the junction temperature up to a point close to the rated maximum. Indeed, operation at point B, where l_2 is tangent to the heating curve, will involve the risk of thermal runaway, so strictly speaking the diode should be derated (dashed line) to guard against this.

Above a certain temperature the crystal begins to lose its semiconductor properties. However, the safe upper limit to junction temperatures

Table 3-1. Comparison of electrical and thermal quantities, symbols and units.

electrical			thermal		
quantity	symbol	unit	quantity	symbol	unit
time	t	s	time	t	s
voltage	V	V	temperature difference	ΔT	degC
current	I	A	power (1 kW /= 860 kcal/h)	P	W
resistance	$R = V/I$	Ω	thermal resistance	$R_{th} = \Delta T/P$	degC/W
conductance	$G = I/V$	Ω^{-1}	thermal conductance	$G_{th} = P/\Delta T$	W/degC
power	$P = VI$	W			
charge	$Q = It$	C	energy (1 kWh = 860 kcal)	$W = Pt$	Ws
capacity	$C = Q/V$	F	heat storage capacity	$C = W/\Delta T$	Ws/degC
impedance	$Z = V(t)/I$	Ω	transient thermal impedance	$Z_{th} = \Delta T/(t)/P$	degC/W
specific quantities					
resistivity	$\varrho = RA/l$	Ωm	thermal resistivity	$\varrho = R_{th}A/l$	mdegC/W
conductivity	$\gamma = 1/\varrho$	$(\Omega m)^{-1}$	thermal conductivity	$\gamma = 1/\varrho$	W/mdegC
			specific heat storage capacity:		
			per unit mass m*	$c = C/m$	Ws/gdegC
			per unit volume v	$c = C/V$	Ws/m^3 degC
			heat transfer coefficient (= thermal conductance to cooling medium per unit area)	$h = G/A$	W/m^2degC

* often termed "specific heat"

is usually set by the manufacturer at a much lower level, with a view to ensuring thermal stability. Commonly the upper limit is at 190 °C; if this and other limits are observed, the diode can be expected to operate reliably over a very long period. It is permissible for the maximum junction temperature to be exceeded occasionally, as a result of surge phenomena, provided the surges keep within the non-repetitive ratings laid down for the diode. It should be borne in mind that non-repetitive ratings are based on the assumption that the permitted overloads will not occur more than a few hundred times during the lifetime of the diode.

3.2.2 Thermal Resistance

Tabled against electrical quantities and units in Table 3-1 are the analogous thermal quantities and units. The electrical analogy requires that solid material (or indeed any conductor of heat) be seen as a thermal resistance through which heat (or power) flows as a result of a temperature difference set up across its ends; just as a difference of potential causes a current in a conductor of electricity. On introducing the notion of thermal capacity one can go on to treat physical systems as *RC*-networks, cascaded as necessary. The variation in temperature of a point in the physical system is calculated as a voltage variation at the same point in the equivalent circuit.

Once thermal equilibrium has been established, i.e. in the steady-state mode, all heat storage capacities have been "charged" to their final temperature, and only the overall thermal resistance will be of importance. This overall thermal resistance may be utilized to determine the permissible power loss in a device passing pure d.c., with ambient temperature and maximum permissible junction temperature given. Under pulsating loads (in which steady-state a.c. operation must be included) no temperature balance will be achieved and transients will occur in the power flow. The influence of the heat storage capacities is taken care of by defining transient thermal impedances, which have no electrical analogue.

In accordance with Table 3-1, in the steady state:

$$\Delta T = PR_{th}. \tag{3-10}$$

This law will govern the removal to ambient of heat generated within the device under operational conditions. Rewriting eq. (3-10) for the practical case, we obtain:

$$P = (T_{j\,\max} - T_{amb\,\max})/(R_{th\,j-mb} + R_{th\,mb-h} + R_{th\,h-a}), \tag{3-11}$$

where P = overall power dissipation (forward and reverse)
$T_{j\ max}$ = maximum rated junction temperature,
$T_{amb\ max}$ = maximum anticipated ambient temperature,
$R_{th\ j-mb}$ = maximum rated thermal resistance from junction to mounting base,
$R_{th\ mb-h}$ = thermal resistance from mounting base to heat sink,
$R_{th\ h-a}$ = thermal resistance from heat sink to ambient.

The overall power dissipated depends on the average forward current, the mode of rectification and the crest working reverse voltage. Since the maximum junction temperature and the thermal resistance from junction to mounting base are inherent in the diode under consideration, the maximum permissible average forward current will depend on the resistance of the external thermal path $R_{th\ mb-h} + R_{th\ h-a}$ and on the anticipated value of $T_{amb\ max}$.

Conversely, if the diode is to operate at its maximum ratings, the resistance of the external thermal path must be reduced by providing adequate cooling. The method will be explained with reference to Fig. 3-14.

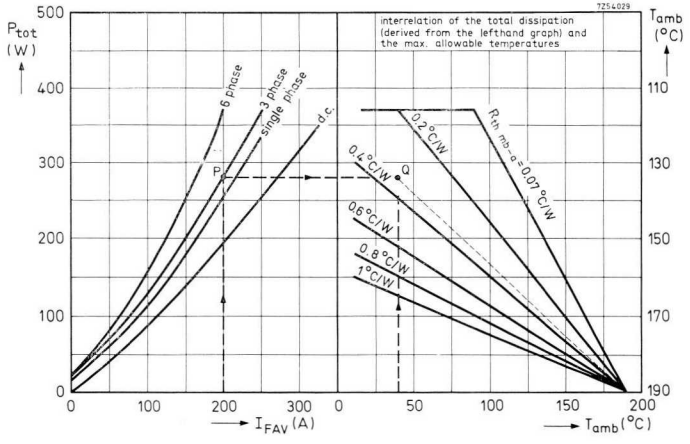


Fig. 3-14 Determination of heatsink thermal resistance.

Assume a three-phase bridge rectifier is required to supply 400 V at 600 A, at 40 °C ambient temperature, the transformer having a capacity of $1.05 \times 400 \times 600 = 252$ kVA.

The average current per diode is clearly 600/3 = 200 A. A type will therefore be selected from the BYX33 series (maximum average forward current 250 A). The crest working reverse voltage is $1.05 \times 400 = 420$ V, so diodes rated for 600 V will be required. The broken lines in Fig. 3-14 show how the graph is used in this particular case. An average forward current of 200 A yields 280 W overall power dissipation per diode (point P). In order not to exceed the rated maximum junction temperature, the thermal resistance $R_{th\ mb-a}$ must not exceed 0.33 degC/W (point Q). Assuming that the thermal resistance from mounting base to heat sink, $R_{th\ mb-h}$, amounts to 0.07 degC/W, the thermal resistance of the heat sink to ambient, $R_{th\ h-a}$, should not exceed 0.26 degC/W.

The graphical solution may be easily verified by applying eq. (3-11):

$$T_{j\ \max} = P(R_{th\ j-mb} + R_{th\ mb-h} + R_{th\ h-a}) + T_{amb\ \max}$$
$$= 280(0.20 + 0.07 + 0.26) + 40 = 188\ ^\circ\text{C},$$

the rated value of $R_{th\ j-mb}$ being 0.20 degC/W for the BYX33. The rated maximum junction temperature is 190 °C. from which it may be seen that the value found above for the thermal resistance of the heat sink is correct. The mounting base temperature can be obtained from:

$$T_{mb} = P(R_{th\ mb-h} + R_{th\ h-a}) + T_{amb}$$
$$= 280(0.07 + 0.26) + 40 = 132\ ^\circ\text{C},$$

which is in close agreement with the graphical solution (the intercept of the horizontal broken line on the right-hand vertical scale is 134 °C).

3.2.3 Transient Thermal Impedance

Fig. 3-15 is a schematic representation of a power diode plus heat sink system whose heating cycle is not unduly long. The temperature T_j of the junction rises in consequence of the dissipated power fed into its thermal capacity C_1. Some power is absorbed by the body of the diode, so there is a difference in temperature between T_j and T_{mb} (the mounting base temperature, measured at the centre of one of the hexagonal faces). The heat flows into the heat sink via the thermal resistance from mounting base to heat sink. The temperature difference $T_h - T_{amb}$ between the heat sink and ambient is responsible for the removal of heat to atmosphere (or to another coolant). As long as the heat supplied to the system and the heat removed to atmosphere differ, no steady-state mode will exist.

The thermal time constant of the diode is very small compared to that of the heat sink (typical values are a few seconds and 10 minutes respec-

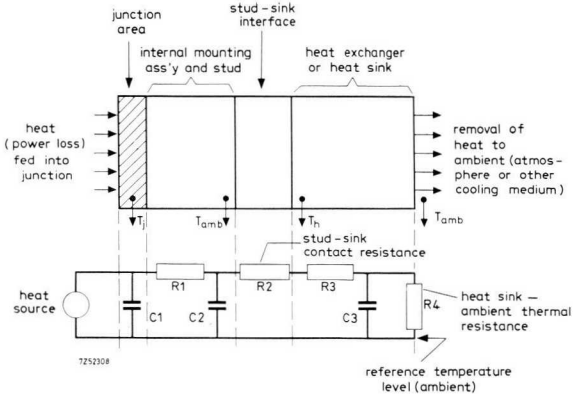


Fig. 3-15 Electrical analogy of heat flow (power flow) junction to ambient, for fairly short heating cycles.

tively) because the heat storage capacity of the power diode is low. For example, a crystal can have a heat storage capacity C_1 of 10 mWs/degC, and an overall heat storage capacity $C_1 + C_2$ of 5 Ws/degC, compared to $C_3 = 56$ Ws/degC for a 100 mm $\times$ 100 mm copper heat sink of 1.6 mm thickness.

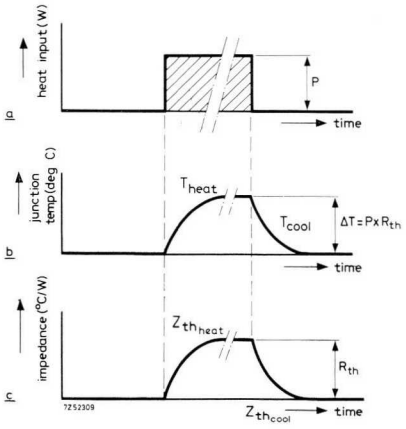


Fig. 3-16 Reponse of the junction to a square power pulse.

The response of the juncton to a step pulse of heating power is illustrated in Fig. 3-16. It may be seen that a definite time elapses before a

steady-state is attained. The heating curve is the inverse of the cooling curve.[3] Hence, at equal time lapses:

$$T_{\text{heat}} + T_{\text{cool}} = \Delta T. \tag{3-12}$$

Dividing by the power pulse P yields an equation expressed in terms of degC/W:

$$Z_{th\ \text{cool}} = R_{th} - Z_{th\ \text{heat}}. \tag{3-13}$$

Clearly in this expression R_{th} is the thermal resistance already mentioned in Section 3.2.2, while $Z_{th\ \text{cool}}$ and $Z_{th\ \text{heat}}$ are transient thermal impedances which determine the state of thermal unbalance. The impedance and temperature curves are congruent (Fig. 3-16*b*, *c*).

For a circuit with a single time constant, $Z_{th\ \text{heat}}$ and $Z_{th\ \text{cool}}$ may be expressed as:

$$Z_{th\ \text{heat}} = R_{th}\,\{1 - \exp(-t/RC)\}, \tag{3-14}$$

and

$$Z_{th\ \text{cool}} = R_{th}\exp(-t/RC). \tag{3-15}$$

These formulae are fair approximations for a heat sink of reasonable thickness having a uniform surface temperature, i.e. exhibiting a thermal efficiency approaching unity (cf. Chapter 5). This assumes that the thermal capacity of the heat sink is large with respect to that of the device. The transient thermal impedance of the heat sink, either measured or calculated with eq. (3-14), can then be added to the thermal resistance of the device to find the overall thermal response of the complete system as illustrated in Fig. 3-17. It appears from this plot that the heat sink has no effect on the thermal system during the first second that elapses

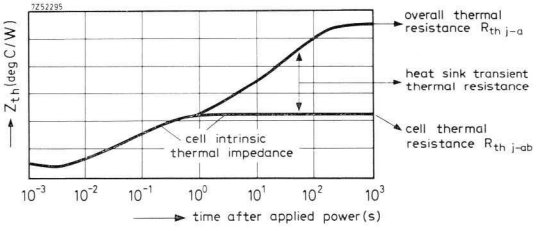


Fig. 3-17 Transient thermal impedances. BYX14 power diode mounted on heat-sink type 56 283.

following injection of the power pulse; thereafter it starts to play a part in the removal of heat. After about 300 s the heat sink thermal capacity is no longer effective in restricting the junction temperature rise, and the ultimate junction temperature will be dominated almost exclusivily by the thermal resistance of the heat sink.

As was shown above, the thermal capacity of the crystal is very low. This is particularly true of the junction area. The junction heats up very rapidly under load, and thus the junction temperature may fluctuate during the power cycle. Still, its very small thermal capacity may be efficient in arresting the rapid rise of junction temperature at subcycle load durations. In addition, the time constant of the heat sink is so large that for surges the temperature of the envelope may be regarded as constant. Under these conditions pulses with amplitudes many times in excess of the continuous ratings may be handled by the diode under consideration.

The transient thermal impedance of the crystal is found by measuring the junction temperature. Since the junction area is inaccessible the junction temperature cannot be measured directly. However, it was shown in Section 3.1.1 that the forward voltage drop is a function of temperature. The rise in junction temperature is determined by monitoring the anode-to-cathode voltage drop at a low standing current, say 10 mA, immediately after application of a pulse load of exactly known magnitude. The forward voltage drop versus junction temperature has been carefully calibrated by placing the diode under investigation in an oven with thermostatically controlled temperature: the anode-to-cathode voltage drop is measured at different temperatures, while keeping the low-level standing current constant. The variation of forward voltage drop due to the applied pulse load, as displayed on an oscilloscope, is shown in Fig. 3-18. The transitory voltage due to heating up of the junction is designated ΔV_F (the transition is very rapid and can be detected only on a greatly

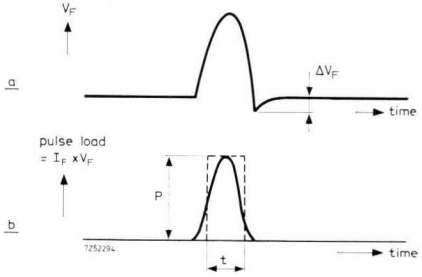
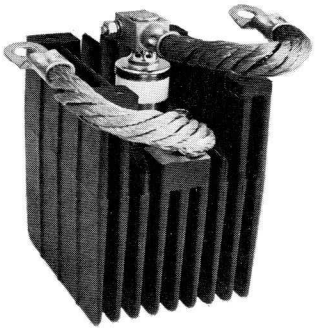


Fig. 3-18 Method of determining junction temperature rise.

expanded time base). Curve b is obtained graphically by multiplying the forward voltage drop and forward current. The duration t and power dissipation P of an equivalent square-wave pulse are shown in broken line. The junction temperature rise is found with the aid of the calibration curve from the decrease ΔV_F in the forward voltage drop as measured on the trace. The transient thermal impedance can be plotted by observing the forward voltage drop as a function of time, following application of the surge. Since the thermal impedance of the crystal, $Z_{th} = \{T_j(t) - T_{mb}\}/P$, the mounting base temperature must be accurately known.



250A diode on its heatsink.

4 Pulse Loading Considerations

4.1 Introduction

If a power diode is to operate reliably under repetitive pulsatory loads, care must be taken that its maximum permissible junction temperature is not exceeded. Pulse loading causes junction temperature fluctuations, and is not permissible unless the resulting peaks are within the temperature limit laid down in the data sheet. Peak junction temperature in turn depends on the transient thermal impedance (cf. Section 3.2.3) of the diode and its associated cooling system.

Thus, the magnitude of the pulses that can be handled safely is determined by the rating of the diode, its heat dissipation and the use or otherwise of a heat sink. Fitting a heat sink permits short trains of pulses with amplitudes exceeding the continuous ratings to be alternated with moderate loading, as the relatively large thermal time constant delays the rise in junction temperature. The thermal time constant of the diode crystal itself is too small to prevent the occurrence of junction temperature fluctuations, even under steady a.c. operation.

Calculations of junction temperature can be made by means of a graph showing transient thermal impedance v.s time, plotted for the diode in combination with its heat sink. The method will be explained below. The following symbols are used:

ΔT = temperature difference,
w = duration of square power pulse (pulse width),
τ = power pulse repetition time,
δ = duty factor of repetitive square power pulse ($= w/\tau$),
P = amplitude of square power pulse.

4.2 Heating and Cooling Curves

When a diode is subjected to a step function of heating power, its (exponential) junction temperature rise is governed by the various time constants present in the thermal system (Fig. 4-1). As explained in Section 3.2.3, the transient thermal impedance $Z_{th}(t)$ is measured by injecting a

unit power pulse and determining the resulting change in junction temperature after a specified time. After infinite time, junction temperature will stabilize at a steady-state value, while transient thermal impedance will equal thermal resistance.

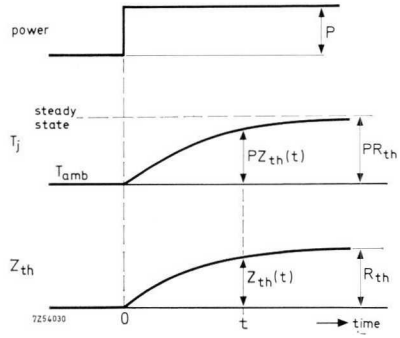


Fig. 4-1 Heating curves for a step function of electrical input power.

From Fig. 4-1 we derive the following formula:

$$T_j(t) = T_{amb} + PZ_{th}(t), \tag{4-1}$$

where $T_j(t)$ denotes the junction temperature at any instant t. The steady-state junction temperature is:

$$T_{jss} = T_{amb} + PR_{th}. \tag{4-2}$$

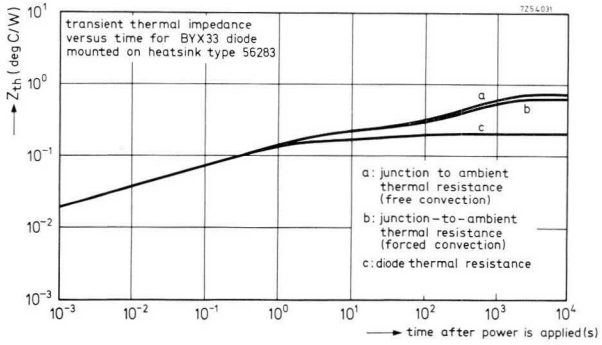


Fig. 4-2 Transient thermal impedance of BYX33 diode on heatsink type 56283, as a function of time.

Example

Fig. 4-2 is a plot of transient thermal impedance vs. time for power diode BYX33 when mounted on a heat sink Type 56283. Assume a step function of 150 W is applied to this diode at 40 °C ambient temperature at free convection. Find the junction temperature 1 s after application of the power, and at infinite time.

From Fig. 4-2 it can be seen that $Z_{th}(1s) = 0.145$ degC/W and $R_{th} = 0.72$ degC/W (at 10^4 s). From eq. (4-1) the junction temperature after 1 s is:

$$T_j(1s) = 40 + (150 \times 0.145) = 62\ ^\circ C,$$

and from eq. (4-2) the junction temperature at infinite time:

$$T_{jss} = 40 + (150 \times 0.72) = 148\ ^\circ C.$$

Upon removal of the applied power, the junction temperature will gradually drop to the ambient level as illustrated in Fig. 4-3. If the junction temperature has stabilized to a steady-state value before the input of power is stopped, the cooling curve will be the inverse of the heating curve, since an abrupt stoppage of the power input is equivalent to superimposing a step function of "negative" power having the same magnitude.

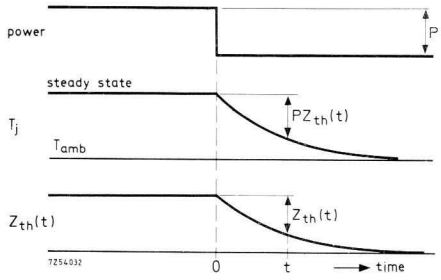


Fig. 4-3 Cooling curves for a step function of power.

Consequently the cooling curve may be readily found from eq. (4-1) by substituting the steady-state junction temperature ($T_{amb} + PR_{th}$) for T_{amb}, and $-P$ for P. Thus we find for the cooling curve, for steady-state operation:

$$T_j(t) = T_{amb} + P\{R_{th} - Z_{th}(t)\}. \qquad (4\text{-}3)$$

Example

Find the junction temperature for power diode BYX33, 20 s after termination of 150 W step function, at 40 °C ambient temperature (steady-state operation before removal of power).

From Fig. 4-2 it is seen that $R_{th} = 0.72$ degC/W and $Z_{th}(20s) = 0.25$ degC/W. According to eq. (4-3):

$$T_j(20s) = 40 + 150(0.72 - 0.25) = 111\ ^\circ C.$$

4.3 Loading with a Single Square Power Pulse

In practical applications a power pulse will decay before stabilization of junction temperature occurs (Fig. 4-4). The heating curve is determined by the magnitude of the power pulse P, the cooling curve by the peak junction temperature T_{jp} occurring when the applied power is cut off. In these circumstances the heating and cooling curves will not be conjugate, and eq. (4-3) is not applicable.

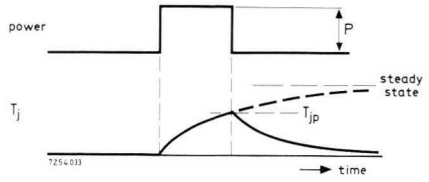


Fig. 4-4 Effect of brief power pulse on junction temperature.

The instantaneous junction temperature can be calculated by resolving the applied power pulse into a positive- and a negative-going step function, in the manner shown in Fig. 4-5. In fact, the pulse of duration w, is regarded as equivalent to a positive step P occurring at the onset of the pulse, and an equal negative step $-P$ applied at $t = w$. These step functions yield heating curve a and cooling curve b. The actual cooling curve (after termination of the square power pulse) will be the algebraic sum of a and b. From Fig. 4-5 the instantaneous junction temperature at time t during cooling down may be derived:

$$T_j(t) = T_{amb} + P\{Z_{th}(t) - Z_{th}(t - w)\}. \tag{4-4}$$

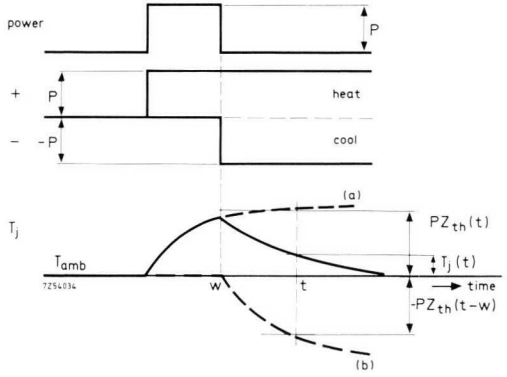


Fig. 4-5 Graphical method of finding instantaneous junction temperature.

Example
Find peak junction temperature for diode BYX33 and junction temperature 5 s after onset of 200 W power pulse of 2 s duration, at $T_{amb} = 40$ °C.

From Fig. 4-2 it is seen that:

$$Z_{th}(t) = Z_{th}(5s) = 0.20 \text{ degC/W},$$
$$Z_{th}(t - w) = Z_{th}(5 - 2s) = Z_{th}(3s) = 0.185 \text{ degC/W},$$
$$Z_{th}(w) = Z_{th}(2s) = 0.17 \text{ degC/W}.$$

The peak junction temperature at termination of the pulse is, from eq. (4-1):

$$T_{jp} = T_{amb} + PZ_{th}(2s) = 40 + 200 \times 0.17 = 74 \text{ °C}.$$

The junction temperature 5 s after onset of the power pulse is, from eq. (4-4):

$$T_j(5s) = 40 + 200(0.20 - 0.185) = 43 \text{ °C}.$$

4.4 Loading with Repetitive Square Power Pulses

4.4.1 Pulses of Equal Magnitude

When power is applied in the form of repetitive square wave pulses with duty factor δ, the variation in junction temperature takes on a sawtooth shape, as illustrated in Fig. 4-6. The average junction temperature exhibits an exponential rise, tending to a steady-state value when the square wave is sustained for a sufficiently long time. On the analogy of eq. (4-2), the average steady-state junction temperature follows from:

$$T_{jss\ av} = T_{amb} + \delta P R_{th}. \tag{4-5}$$

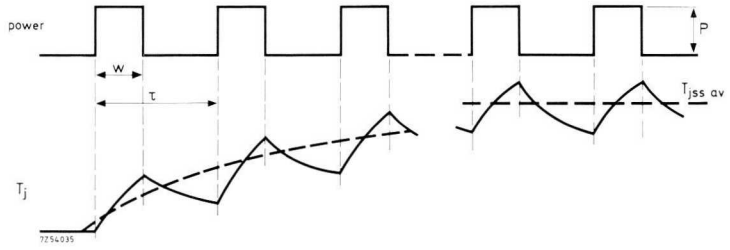


Fig. 4-6 Time function of T_j at repetitive pulse loading.

Example
Find the steady-state average junction temperature for power diode BYX33 when loaded by 40 W (P_c) continuous duty with superimposed 200 W (P_p) pulses: $w = 2$ s, $\delta = 0.4$ (repetition time $t = 5$ s), $T_{amb} = 40$ °C.

Fig. 4-2 shows that $R_{th} = 0.72$ degC/W. The junction temperature rise due to P_c is, from eq. (4-2):

$$\Delta T_{jc} = P_c R_{th} = 40 \times 0.72 = 28.8\ ^\circ\text{C}.$$

The junction temperature rise due to P_p is, from eq. (4-5):

$$\Delta T_{jp} = \delta P_p R_{th} = 0.4 \times 200 \times 0.72 = 57.6\ ^\circ\text{C},$$

(this T_{jp} is the *average* rise due to P_p)
which gives:

$$T_{jss\ av} = T_{amb} + 4T_{jc} + 4T_{jp} = 126\ ^\circ\text{C}.$$

Care must be taken not only to keep the average junction temperature within the ratings of the diode, but also to ensure that the permissible peak junction temperature is not exceeded, especially where the train consists of large pulses having a low duty factor. The calculation of peak junction temperature due to three equidistant pulses of equal magnitude is worked out below (Fig. 4-7).

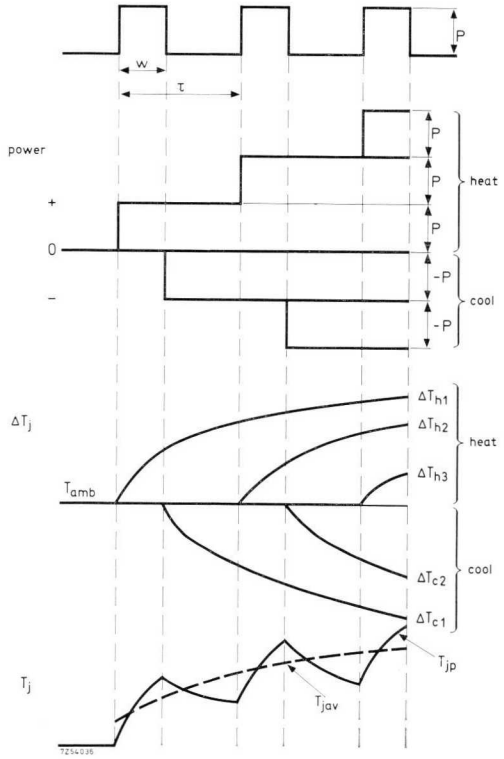


Fig. 4-7 Heating effect of three equidistant equal magnitude pulses.

As explained previously, the pulses can be replaced by heating and cooling step functions giving rise to conjugate heating and cooling curves, shifted in time. Maximum junction temperature will be reached at the end of the third pulse:

$$T_{jp} = T_{amb} + \Delta T_{h1} - \Delta T_{c1} + \Delta T_{h2} - \Delta T_{c2} + \Delta T_{h3}, \qquad (4\text{-}6)$$

(this T_{jp} is *peak*)

where:

$$\begin{aligned} \Delta T_{h1} &= PZ_{th}(2\tau + w), & \Delta T_{c1} &= PZ_{th}(2\tau), \\ \Delta T_{h2} &= PZ_{th}(\tau + w), & \Delta T_{c2} &= PZ_{th}(\tau). \\ \Delta T_{h3} &= PZ_{th}(w), \end{aligned} \qquad (4\text{-}7)$$

Hence:

$$T_{jp} = T_{amb} + P\{Z_{th}(2\tau + w) - Z_{th}(2\tau) + \\ + Z_{th}(\tau + w) - Z_{th}(\tau) + Z_{th}(w)\}. \qquad (4\text{-}8)$$

Similarly, for n equidistant pulses of amplitude P:

$$T_{jp} = T_{amb} + P\left\{\sum_{a=0}^{a=n-1} Z_{th}(a\tau + w) - \sum_{a=1}^{a=n} Z_{th}(a\tau)\right\}. \qquad (4\text{-}9)$$

Example

Find the maximum junction temperature for diode BYX33, mounted on a Type 56283 heat sink, immediately after it has passed five 900 W pulses of 0.5 s at 1 s repetition time; $T_{amb} = 40\ ^{\circ}C$.

From eq. (4-9):

$$T_{jp} = T_{amb} + P[\{Z_{th}(4.5s) + Z_{th}(3.5s) + Z_{th}(2.5s) + Z_{th}(1.5s) + \\ + Z_{th}(0.5s)\} - \{Z_{th}(4s) + Z_{th}(3s) + Z_{th}(2s) + Z_{th}(1s)\}].$$

Consulting Fig. 4-2 we find:

$$T_{jp} = 40 + 900\{(0.196 + 0.19 + 0.18 + 0.16 + 0.12) - \\ - (0.193 + 0.185 + 0.17 + 0.145)\} = 178\ ^{\circ}C.$$

This load (450 W average during 5 s) can be carried by the diode, which is rated for a maximum junction temperature of 190 °C. Note, however, that only about 250 W average can be handled continuously, even if the diode is mounted on a heat sink of lower thermal resistance (e.g. Type 56283 having a thermal resistance of about 0.50 degC/W.

Eq. (4-9) can be utilized to calculate the peak value of the ripple in junction temperature occasioned by a pulsatory load. However, a large number of terms has to be dealt with because the junction temperature takes

a relatively long time to attain the steady state. A less laborious method, an approximation that is of sufficient accuracy for all practical purposes, is suggested in Section 4.5.

4.4.2 Pulses of Differing Magnitude

Fig. 4-8 shows how junction temperature reacts to a train of power pulses differing in magnitude. Since the maximum temperature is not necessarily reached at the end of the last pulse, the peak junction temperature at the

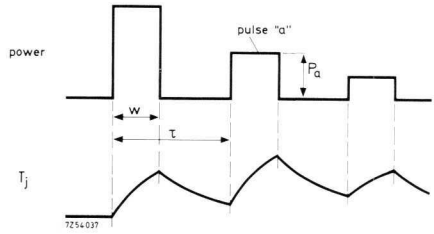


Fig. 4-8 Heating effect of three equidistant, unequal magnitude pulses.

end of each pulse must be checked against the maximum rating by means of the formulae set out below. Basing the argument on eq. (4-6), we can write:

$$T_{jp} = T_{amb} + \{\Delta T_{h1} - \Delta T_{c1}\} + \{\Delta T_{h2} - \Delta T_{c2}\} + \ldots + \\ + \{\Delta T_h(n-1) - \Delta T_c(n-1)\} + \Delta T_{hn}. \qquad (4\text{-}10)$$

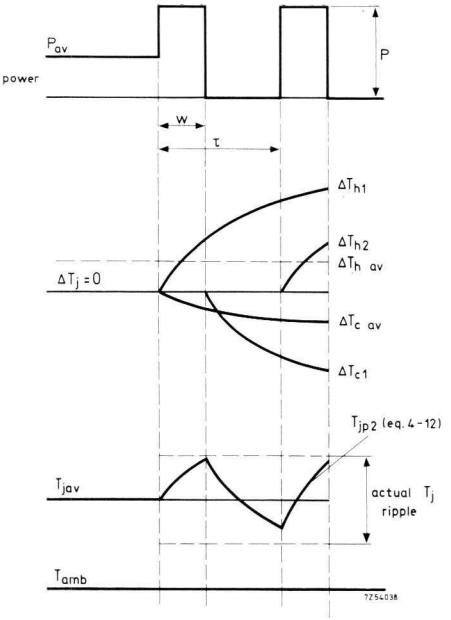
Hence, the junction temperature immediately after n pulses have been passed, can be expressed by:

$$T_{jp} = T_{amb} + \sum_{a=1}^{a=n} P_a Z_{th}\{(n-a)\tau + w\} - \sum_{a=1}^{a=n-1} P_a Z_{th}\{(n-a)\tau\}. \qquad (4\text{-}11)$$

4.5 Two-Pulse Approximation

Fig. 4-9 illustrates an approximate method of finding the final peak junction temperature of the diode subjected to a steady pulsatory load. Firstly assume the average load to be immediately followed by *two* of the actual square power pulses. The junction temperature at the end of the second pulse is then:

$$T_{jp} = T_{amb} + \Delta T_{h\,av} - \Delta T_{c\,av} + \Delta T_{h1} - \Delta T_{c1} + \Delta T_{h2}.$$



$$\Delta T_{h1} = P \times Z_{th}(\tau + w),$$
$$\Delta T_{h2} = Z_{th}(w),$$
$$\Delta T_{av} = \Delta T_{h1} - \Delta T_{c1} = \delta P R_{th}$$
$$\Delta T_{c1} = P\, Z_{th}(\tau + w) = \delta P Z_{th}(\tau + w),$$
$$T_{j\,av} = T_{amb} + \tau P R_{th}.$$

Fig. 4-9 The two-pulse approximation method for finding peak steady-state junction temperature.

Expressing this formula in terms of thermal impedances gives:

$$T_{jp2} = T_{amb} + P\{\delta R_{th} - \delta Z_{th}(\tau + w) + Z_{th}(\tau + w) - Z_{th}(\tau) + Z_{th}(w)\}. \tag{4-12}$$

Now, if *three* of the actual power pulses are assumed to follow the average load, the maximum peak junction temperature becomes:

$$T_{jp3} = T_{amb} + P\{\delta R_{th} - \delta Z_{th}(2\tau + w) + Z_{th}(2\tau + w) - \\ -Z_{th}(2\tau) + Z_{th}(\tau + w) - Z_{th}(\tau) + Z_{th}(w)\}. \tag{4-13}$$

Clearly, the general expression based on n pulses is:

$$T_{jp} = T_{amb} + P(\delta R_{th} - \delta Z_{th}\{(n-1)\tau + w\} + \\ + \sum_{0}^{n-1} Z_{th}\{(n)T + w\} - \sum_{0}^{n-1} Z_{th}(nT)]. \tag{4-14}$$

If these formulae are compared with eq. (4-1) it will be seen that the terms between brackets represent the "composite" transient thermal impedance for repetitive pulse loading, with duty factor 0, pulse duration w and repetition time τ.

The closeness of approximating the final peak junction temperature improves as one increases the number of pulses on which calculation is based; but the two-pulse approximation is sufficiently accurate for most practical purposes, as evident from the following example.

Example

Power diode BYX33, mounted on heat sink Type 56283, is loaded with 400 W pulses of 10 s duration and 50 s repetition time. Ambient temperature is 35 °C. Find average junction temperature, and also peak junction temperature by the two- and the three-pulse methods.

From eq. (4-2):

$$T_{j\,av} = T_{amb} + \delta P R_{th} = 35 + 0.2 \times 400 \times 0.72 = 92.6\ ^\circ\text{C}.$$

According to the two-pulse method, from eq. (4-12) and Fig. 4-2:

$$T_{jp2} = T_{\text{amb}} + P\{0.2R_{th} - 0.2Z_{th}(60\text{s}) + Z_{th}(60\text{s}) - Z_{th}(50\text{s}) + Z_{th}(10\text{s})\} = \\ = 35 + 400\{0.2 \times 0.72 + 0.8 \times 0.29 - 0.285 + 0.225\} = 161\ ^\circ\text{C}.$$

According to the three-pulse method, from eq. (4-13) and Fig. 4-2:

$$T_{jp3} = 35 + 400(0.2 \times 0.72 + 0.8 \times 0.33 - 0.32 + 0.29 - 0.285 + 0.225) = 162\ ^\circ\text{C}.$$

These solutions suggest that the two-pulse method is sufficiently exact. The "composite" transient thermal impedance for the pulse loaded system amounts to 0.32 degC/W.

4.6 Overload Following Continuous Duty

4.6.1 Pure D.C. Overload

The situation of a pure d.c. overload P_{ov} of duration t is depicted in Fig. 4-10, from which we derive:

$$T_j(t) = T_{amb} + P_c R_{th} + (P_{ov} - P_c)Z_{th}(t). \qquad (4\text{-}15)$$

Example

A BYX33 diode, operating at 60 W continuous duty, takes 5 s d.c. overload of 300 W. Ambient temperature is 50 °C. Determine maximum junction temperature.

From Fig. 4-2 and eq. (4-15):

$$T_j(5\text{s}) = T_{amb} + P_c R_{th} + (P_{ov} - P_c)Z_{th}(5\text{s}) \\ = 50 + (60 \times 0.72) + (240 \times 0.20) = 141\ ^\circ\text{C},$$

which is within the ratings of the diode (190 °C).

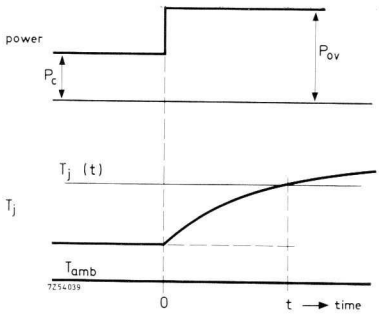


Fig. 4-10 Effect of steady d.c. overload on T_j.

4.6.2 Square-Wave Pulsatory Overload

The situation of an overload consisting of a burst of square pulses P of total duration t_{ov} is depicted in Fig. 4-11. The resulting peak junction temperature based on the two-pulse approximation is:

$$T_{jp} = T_{amb} + P_{av}R_{th} - P_{av}Z_{th}(t_{ov}) + \delta PZ_{th}(t_{ov}) - \\ -\delta PZ_{th}(\tau + w) + P\{Z_{th}(\tau + w) - Z_{th}(\tau) + Z_{th}(w)\}. \qquad (4\text{-}16)$$

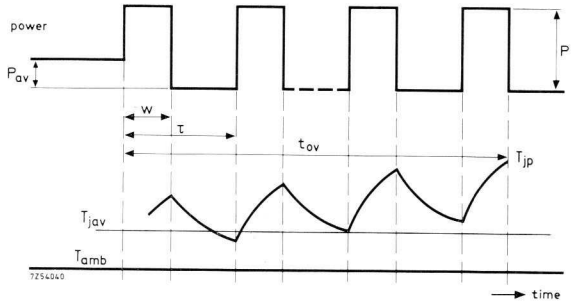


Fig. 4-11 Square wave pulsatory overload effect on T_j.

Example

Diode BYX33, dissipating 50 W average power at 85 °C ambient temperature, is subjected to a burst of three 2500 W semi-sinusoidal pulses of 10 ms duration and 20 ms repetition time; the duty factor is 0.3 (approximate value for sinusoidal currents). Calculate the peak junction temperature at the end of this overload.

The overload time is

$$t_{ov} = 2\tau + w = 50 \text{ ms},$$

and the pulse duration

$$w = \delta t = 0.3 \times 20 = 6 \text{ ms}.$$

Substituting the values from Fig. 4-2 in eq. (4-16) gives:

$$T_{jp} = 35 + 50 \times 0.72 - 50 \times 0.058 + \\ + 2500(0.3 \times 0.058 - 0.3 \times 0.049 + 0.049 - 0.046 + 0.032) = 162 \text{ °C}.$$

4.7 Irregularly Shaped Power Pulses

A convenient way of dealing with an irregularly shaped power pulse is to treat it as a cluster of rectangular pulses having the same duration (Fig. 4-12). The junction temperature T_{jp} at the end of the last pulse is not

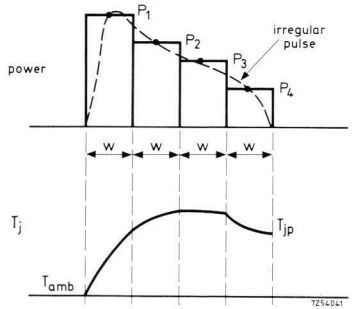


Fig. 4-12 Resolution of an irregular pulse into equal width rectangles to find approximate T_j.

necessarily the highest temperature occurring during the cluster. By breaking down each rectangular pulse into a positive- and a negative-going step function, exactly as before, we arrive at the following expression for the junction temperature at the end of the cluster:

$$T_{jp} = T_{amb} + P_1 Z_{th}(4w) - Z_{th}(3w) + P_2 Z_{th}(3w) - Z_{th}(2w) + \\ + P_3 Z_{th}(2w) - Z_{th}(w) + P_4 Z_{th}(w). \qquad (4\text{-}17)$$

This equation can easily be expanded to cover a cluster of n pulses P_1, P_2, . . ., P_n of equal width w.

A train of irregularly shaped power pulses can be conservatively treated in the manner shown in Fig. 4-13; such waveforms may arise under reactive load conditions. The irregular power pulse is transformed into a single pulse of the same height and energy content. Since S_1, S_2, S_3 are equal in area (S_3 represents the average load), we have $P_{av}\tau = P_p w$. Since $w = \delta\tau$, it follows that:

$$\delta = P_{av}/P_p. \qquad (4\text{-}18)$$

This method is conservative because a rectangular pulse has a shorter duration than any other pulse of the same average power and amplitude. In other words, the rectangular pulse concentrates its heating effect within a shorter period of time, during which the junction has little chance to cool off; so a temperature rise calculated on this basis will certainly be larger than the actual rise in junction temperature.

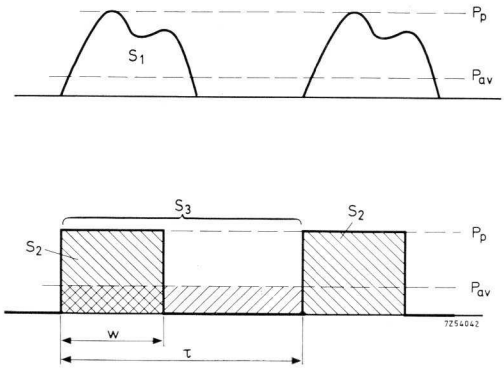


Fig. 4-13 Representation of a regular train of irregular pulses by rectangular ones having the same height and energy (area). Areas S_1, S_2 and S_3 are equal.

Example

Calculate the peak and average junction temperature for a BYX33 power diode mounted on a Type 56283 heat sink and operating as a half-wave rectifier, when loaded with 100 A average current at 40 °C ambient temperature. The supply frequency is 50 Hz. The BYX33 forward voltage drop and power dissipation characteristics are given in Figs 4-14 and 4-15 respectively.

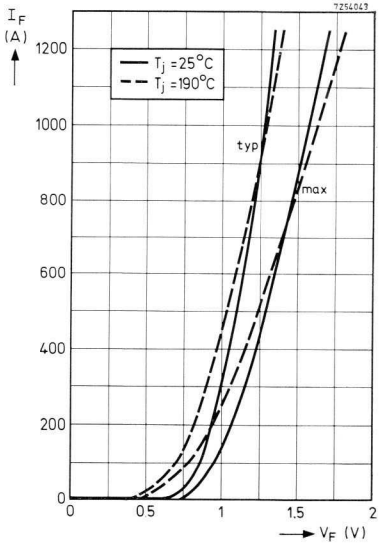


Fig. 4-14 BYX33 forward characteristic

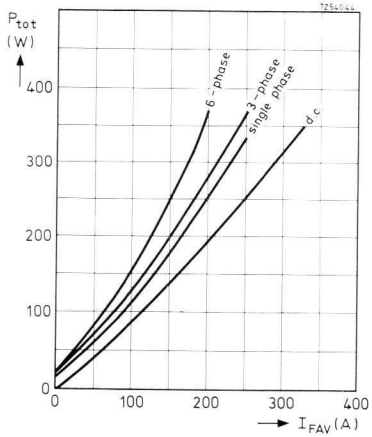


Fig. 4-15 BYX33 load characteristic.

The average junction temperature is calculated as follows. From Fig. 4-15 (single-phase characteristics) P_{av} is seen to be 110 W at $I_{FAV} = 100$ A. From Eq. 4-2:

$$T_{jss} = T_{amb} + P_{av}R_{th} = 40 + 110 \times 0.72 = 119\ ^{\circ}\text{C}.$$

Since

$$I_{FWM} = \pi I_{FAV} = 3.14 \times 100 = 314\ \text{A},$$

we derive from Fig. 4-14 (typical) that, at $T_j = 120\ ^{\circ}\text{C}$, $V_{FM} = 0.95$ V, giving for the peak power:

$$P_p = I_{FWM}V_{FM} = 298\ \text{W}.$$

Thus from eq. (4-18):

$$\delta = P_{av}/P_p = 110/298 = 0.37,$$

and

$$w = \delta t = 0.37 \times 20 = 7.4\ \text{ms}.$$

Consequently, the actual power can safely be replaced by a square pulse having an amplitude of 298 W, a width of 7.4 ms and a repetition time of 20 ms, as shown in Fig. 4-16. According to eq. (4-12) this gives $T_{jp} = 125\ ^{\circ}\text{C}$.

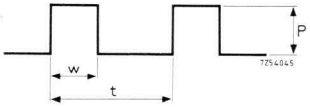


Fig. 4-16 $P = 361$ W, $w = 6$ ms, $\tau = 20$ ms.

Thus the calculated peak junction temperature exceeds the average value by 6 °C. The actual difference between the peak and average junction temperature will, in fact, be smaller because approximation by a square pulse waveform overestimates the junction temperature. However, the above calculation does demonstrate that at 50 Hz operation a junction temperature ripple is present, due to the extremely low junction thermal capacity.

5 Cooling Considerations

5.1 Introduction

Power devices are mounted on heat sinks to remove internally generated heat. Use of a suitable heat sink enables the power device to be operated at heavy loads without the maximum permissible junction temperature being exceeded. Where large power dissipation levels are involved, forced air circulation may become necessary to provide sufficient cooling.

The heat sink has a relatively large thermal time constant, hence it will be effective only in limiting the junction temperature to the rated level in the case of prolonged load cycles (several minutes duration). For short load cycles (from about 1 s to subcycle surge conditions) the rise in temperature of the heat sink will be negligible. Under such conditions, the peak junction temperature will be determined by the thermal time constant of the device itself (a few seconds), or even by the heat storage capacity of the junction area alone (thermal time constant a few milliseconds), depending on how long the load is applied.

For effective heat sink design it is necessary to have the following data: maximum rated junction temperature, thermal resistance of the device, thermal resistance from the device to the heat sink (derived from the data sheets *), power dissipation, and ambient temperature (dictated by the application).

Heat transfer direct from the case of the device to ambient constitutes an important factor in heat sink design, since it materially reduces the power flow via the heat sink path. The graphs given in this section allow for the effect of the envelope thermal resistance, thus ensuring optimum heat sink design.

5.2 Heat Transfer Theory

At temperature equilibrium the total energy supplied per second is equal to the total energy removed per second. The equation for heat transmission is, therefore:

$$P = \eta_h h_t a_t \Delta T \qquad (5\text{-}1)$$

* Where data sheets are mentioned, the reader is referred to our DATA Handbook System.

where P = power dissipation of the device,
η_h = heat sink efficiency,
h_t = total heat transfer coefficient,
a_t = total heat dissipating area,
ΔT = temperature difference.

5.2.1 Total Heat Transfer Coefficient

Heat transfer can take place by free or forced convection, and by radiation. The following heat transfer coefficients may be distinguished:
h_c, the transfer coefficient for free (natural) convection;
h_f, the transfer coefficient for forced convection;
h_r, the transfer coefficient for radiation.
The total heat transfer coefficient, h_t, equals $h_c + h_r$ for free convection and $h_f + h_r$ for forced convection.

5.2.2 Heat Transfer by Free Convection

The term free convection applies when the movement of air is due exclusively to local temperature differences in the vicinity of the heat sink. The heat transfer coefficient h_c, expressed in terms of W/m^2 degC, can be found from the following expression:

$$h_c = 1.4(\Delta T_{h-a}/l_c)^{\frac{1}{4}} f_p f_a = A f_p f_a, \tag{5-2}$$

where ΔT_{h-a} = temperature difference in degC between heat sink and ambient,
l_c = effective length of heat sink in m, see Table 5-1,
f_p = position correction factor, see Table 5-2,
f_a = altitude correction factor, see Fig. 5-1.

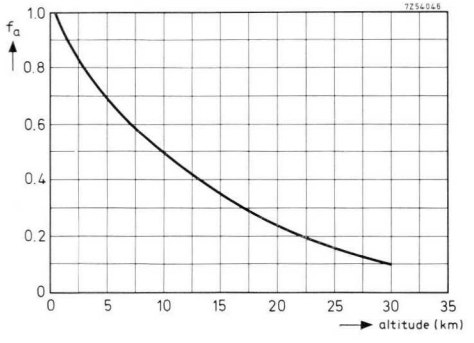


Fig. 5-1 Altitude correction factor f_a vs. altitude.

The factor $A = 1.4(\Delta T_{h-a}/l_c)^{\frac{1}{4}}$ can be found graphically from Fig. 5-2.

Table 5-1. Effective length l_c of heat sink (free convection).

shape	position	effective length l_c
rectangular	vertical	height (max. 0.6 m)
	horizontal	$\frac{\text{length times width}}{\text{length plus width}}$
circular	vertical	$\pi/4$ times diameter
	horizontal	half diameter

Table 5-2. Position correction factor f_p (free convection).

position	side	correction factor f_p
horizontal	top	1.29
	bottom	0.63
	combined effect	0.96
vertical	either	1
	combined effect	1

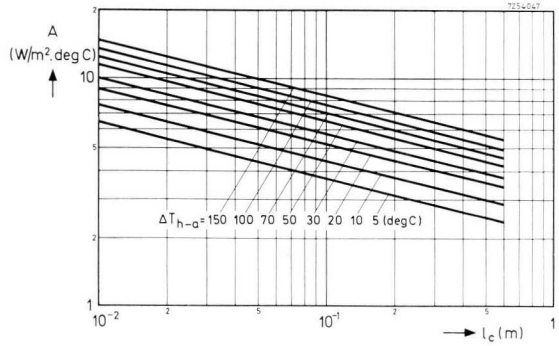


Fig. 5-2 Factor A vs. heat sink effective length l_c.

5.2.3 Heat Transfer by Forced Convection

In the case of forced convection, circulation of the ambient air is caused

by blowers or fans. The transfer coefficient h_f, expressed in W/m^2 degC, can be found from the equation:

$$h_f = \{0.055\gamma_a/(\mu^3/\varrho^3)^{\frac{1}{4}}\} \cdot (v^3/l_f)^{\frac{1}{4}} \cdot f_a, \qquad (5\text{-}3a)$$

which, by putting:

$$0.055\gamma_a/(\mu^3/\varrho^3)^{\frac{1}{4}} = \mathrm{B} \qquad \text{and} \qquad (v^3/l_f)^{\frac{1}{4}} = C,$$

may be written:

$$h_f = BCf_a. \qquad (5\text{-}3b)$$

In these expressions:

γ_a = thermal conductivity of air (W/m^{3}degC),
μ = kinematic viscosity of air (kg/ms),
ϱ = specific density of air (kg/m^3),
v = air velocity in the vicinity of the heat sink (m/s),
l_f = effective length of heat sink at forced convection (m).

The value of l_f depends only on the shape of the heat sink. For a rectangular sink, l_f is the length in the direction of the air flow. For a circular heat sink l_f equals $\pi/4$ times the diameter. The factors B and C have been plotted in Figs 5-3 and 5-4 respectively.

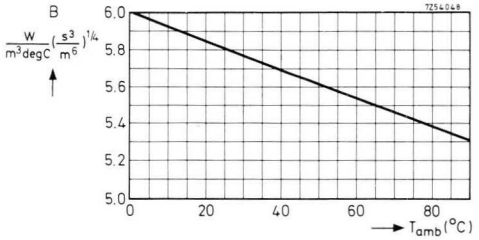


Fig. 5-3 Factor B vs. ambient temperature, T_{amb}.

The thermal resistance of the heat sink can be reduced by painting its surface a dull colour. At air velocities exceeding 3 m/s heat removal by forced convection will, however, be predominant, and the effect of surface coating can then be ignored.

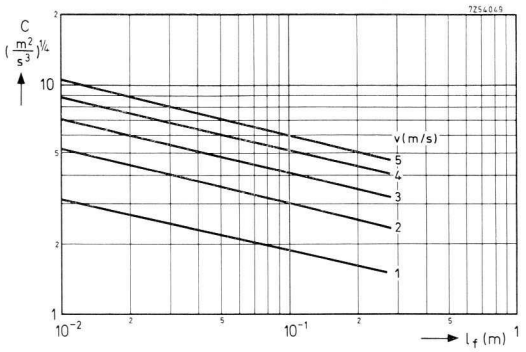


Fig. 5-4 Factor C vs. heat sink effective length, l_f.

5.2.4 Heat Transfer by Radiation

Apart from being transferred by conduction and convection, heat can be radiated. The transmission coefficient for this type of heat transfer, h_r, expressed in terms of W/m²degC, can be found from the equation:

$$h_r = \frac{\sigma(T_h^4 - T_{amb}^4)}{\Delta T_{h-a}} \cdot \varepsilon f_r = D \cdot \varepsilon f, \qquad (5\text{-}4)$$

where σ = Stefan-Boltzmann constant (7.51×10^{-8} W/m²·°K⁴),
T_h = absolute temperature of the heat sink (°K),
T_{amb} = absolute ambient temperature (°K),
ε = emissivity coefficient, see Table 5-3,
f_r = radiation form factor, see Fig. 5-5.

The factor D can be found from the graph plotted in Fig. 5-6.

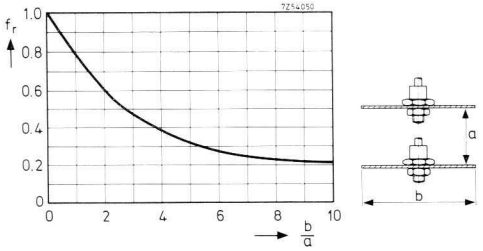


Fig. 5-5 Radiation form factor f_r vs. ratio b/a for each of the facing sides of the heat sinks. The other sides radiate in free space ($fr = 1$).

Table 5-3. Emissivity coefficient ε.*

surface	emissivity coefficient ε
aluminium, polished	0.05
aluminium, oxidized	0.20
copper, polished	0.03
copper, oxidized	0.60
brass, polished	0.10
brass, oxidized	0.60
aluminium paint	0.25 to 0.70
oil paint (all colours)	0.92 to 0.96
lacquer (all colours)	0.80 to 0.95
varnish	0.90

* The emissivity coefficient ε is unity for an ideal black surface. All painted surfaces, even white, have approximately the same emissivity, regardless of colour. Glossy paint has a slightly lower emissivity than a matt painted surface. Emissivity is lowest for polish surfaces, but will substantially increase as the surface oxidizes. In cases where the heat sink carries a protective coating, emissivity will be determined by the coating and not by the metal.

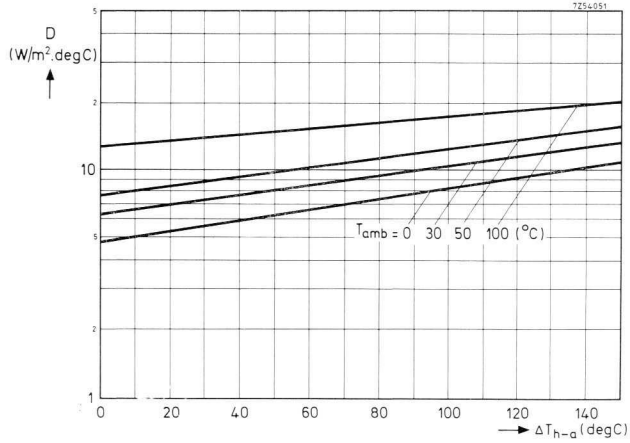


Fig. 5-6 Factor D vs. temperature difference from heat sink to ambient, ΔT_{h-a}.

5.2.5 Heat Sink Efficiency

Calculations of heat transfer such as those above, which are based on the assumption that the entire surface of the heat sink has the same temperatures as the hottest spot, are optimistic and should be corrected for the lower rate of heat transfer occurring at the cooler extremities of the sink. Since the sink material has a finite thermal conductivity, the surface tem-

perature of the sink will decrease as the distance to the heat source (i.e. the power device) increases, owing to surface cooling effects. Consequently, a practical heat sink will have an efficiency η_h, defined as the ratio of the heat actually transferred by the sink to the heat that would be transferred if its entire surface were at the temperature of the hottest spot.

A hypothetical circular heat sink, exhibiting no temperature difference over the surface, would have by definition 100% efficiency. The radius in m of such a hypothetical circular heat sink is given by:

$$r_h = (\gamma_s t/2h_t)^{\frac{1}{2}}, \tag{5-5}$$

where γ_s = thermal conductivity of the heat sink (W/m^{3}degC),
t = thickness of the heat sink (m),
h_t = total heat transfer coefficient (W/m^{2}degC).

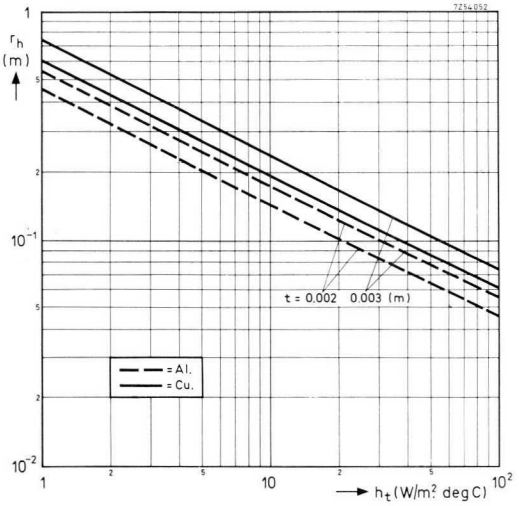


Fig. 5-7 Radius of hypothetical heat sink r_h vs. total heat transfer coefficient h_t.

Fig. 5-7 is a plot of r_h versus h_t for aluminium and copper heat sinks of 0.002 m and 0.003 m thickness. The thermal conductivity γ of various materials is given in Table 5-4.

Table 5-4. Thermal conductivity γ of several metals.

material	copper	aluminium	brass	iron	unit
γ	380	210	110	44	W/mdegC

To find the efficiency of a practical heat sink, dimensions r_i and r_s are introduced in Fig. 5-8, from which we find the heat input radius to be:

$$r_i = (d_1 + d_2)/4. \tag{5-6}$$

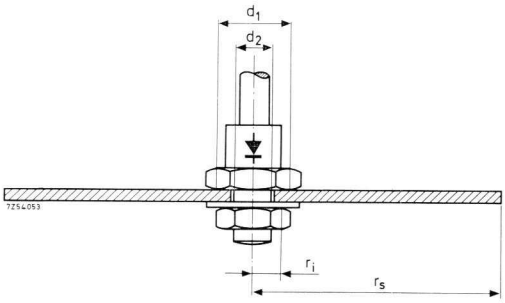


Fig. 5-8 Practical heat sink dimensions.

The heat sink surface is defined by r_s, which equals the external radius for a circular sink. For a rectangular heat sink of length l and width w (provided $l/w \simeq 1$):

$$r_s = (lw/\pi)^{\frac{1}{2}}. \tag{5-7}$$

Knowing the ratios $p = r_h/r_i$ and $q = r_s/r_i$ one can find η_h, the efficiency of a practical heat sink, by reference to Fig. 5-9. Optimum design should

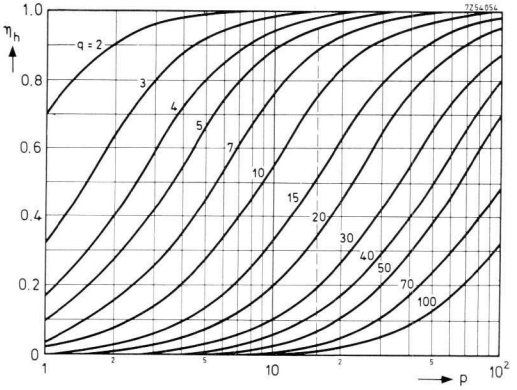


Fig. 5-9 Heat sink efficiency η_h vs. ratios p and q.

yield a figure of about 0.5. An efficiency appreciably lower than 0.5 indicates that the material used is too thin. One as high as 0.9 suggests that the material is too thick, so that the sink will be unnecessarily expensive.

5.2.6 Thermal Resistance of the Heat Sink

Eq. (5-1) can be rewritten:

$$R_{th\ h-a} = \Delta T/P = 1/\eta_h h_t a_t, \tag{5-8}$$

where $R_{th\ h-a}$ is the thermal resistance that exists between ambient and the hottest spot of the heat sink.

For free convection:

$$R_{th\ h-a} = 1/\eta_h(h_c + h_r)a_t, \tag{5-9}$$

and for forced convection:

$$R_{th\ h-a} = 1/\eta_h(h_f + h_r)a_t. \tag{5-10}$$

Since there is some loss of heat direct to ambient from the envelope and connecting leads of the device, only part of the power dissipation will be removed by the heat sink. This implies that $R_{th\ h-a}$ can safely be increased to some extent, i.e. that a smaller heat sink will provide adequate cooling (cf. Section 5.3).

5.3 The Effect of Heat Removal from the Device Envelope

In heat sink design, then, an economy can be made by taking into account the heat lost by the device via its leads and envelope. This more direct path to ambient lies in parallel with that through the heat sink, and its effect is thus to help the crystal get rid of its generated heat. Accordingly, in Fig. 5-10, the simple heat flow diagram *a* has been developed into a more accurate version *b* by shunting an additional thermal resistance $R_{th\ d-a}$, representing the more direct path from device to ambient, across the thermal resistance $R_{th\ h-a}$ from heat sink to ambient and the thermal resistance $R_{th\ mb-h}$ from mounting base to heat sink.

Actual values of $R_{th\ d-a}$ can be found on reference to Fig. 5-11, both for free and forced cooling. A numerical example will give some idea of the advantage obtainable by taking account of the shunt path from the device to ambient.

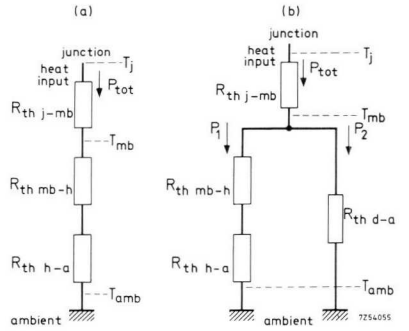


Fig. 5-10 Diagrammatic representation of heat flow. (a) Neglecting heat removal by device envelope; (b) heat removal by device envelope accounted for.

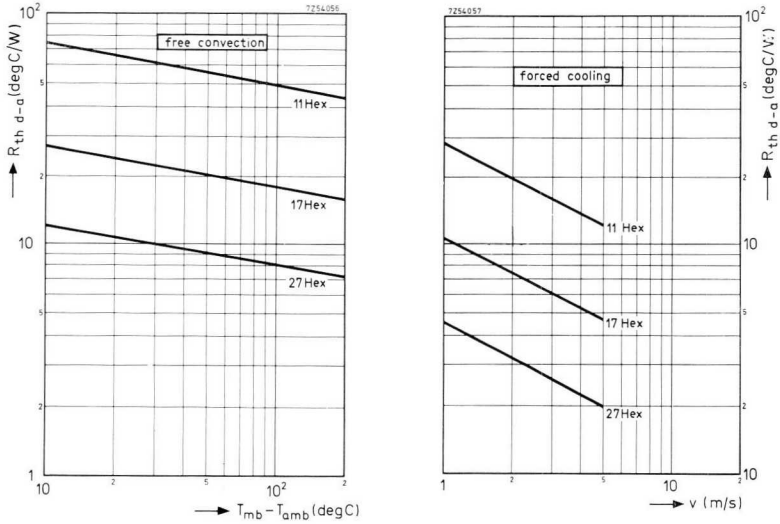


Fig. 5-11 Actual values of direct-to-ambient thermal resistance.

Example

Diode BYX25 is operated at a power dissipation P of 30 W. Ambient temperature $T_{amb} = 50\ ^\circ C$. Free convection is assumed.

The data sheet shows that $T_{j\,max} = 175\ ^\circ C$ and $R_{th\ j-mb} \leqslant 1.3$ degC/W. Assume $R_{th\ mb-h} = 0.5$ degC/W.

The maximum permissible mounting base temperature is:

$$T_{mb\,\max} = T_{j\,\max} - PR_{th\,j-mb} = 175 - 30 \times 1.3 = 136\ ^{\circ}\text{C}.$$

The permissible thermal resistance from mounting base to ambient is:

$$R_{th\,mb-a} = (T_{mb\,\max} - T_{amb})/P = (136 - 50)/30 = 2.86\ \text{degC/W}.$$

This thermal resistance can be considered as the sum of $R_{th\,mb-h}$ and $R_{th\,h-a}$. Neglecting the heat removal by the envelope gives:

$$R_{th\,h-a} = R_{th\,mb-a} - R_{th\,mb-h} = 2.86 - 0.5 = 2.36\ \text{degC/W}.$$

Taking account of the heat removal by the envelope, one thermal path is formed by the series connection of $R_{th\,mb-h}$ and $R_{th\,h-a}$, the other path consisting of $R_{th\,d-a}$. The BYX25 having an 11 Hex envelope, we find, from Fig. 5-11, $R_{th\,d-a} = 50$ degC/W. The two thermal paths may be considered as resistors in parallel. The total thermal resistance from mounting base to ambient is therefore:

$$\frac{(R_{th\,mb-h} + R_{th\,h-a})R_{th\,d-a}}{R_{th\,mb-h} + R_{th\,h-a} + R_{th\,d-a}} = \frac{2.86 \times 50}{2.86 + 50} = 2.72\ \text{degC/W}.$$

Subtracting from this value $R_{th\,mb-h}$, we obtain $2.72 - 0.5 = 2.22$ degC/W, which may be considered as a fictitious value of the resistance from heat sink to ambient. Thus, the thermal resistance is allowed to be $(2.36 - 2.22)/2.22 = 6\%$ higher.

The values quoted by the manufacturer for the thermal resistance from heat sink to ambient always take into account the heat removal from the envelope direct to ambient.

5.4 Heat Sink Nomograms

In the past it has been attempted to give a nomogram to simplify heat sink design. However, it was found that the physical construction of a diode significantly affected the heat transfer and it was not possible to guarantee that the optimum heat sink had been designed when using the nomogram. For the sake of completeness we include the following of how the nomogram was used. In heat sink nomograms $R_{th\,h-a}$ values are plotted along the ordinate which account for the loss of heat from the envelope and leads direct to ambient, so enabling the designer to dimension heat sinks with the utmost economy. Individually, the nomograms relate to particular types of heat sinks, distinction being made between free and forced convection. In the case of free convection, the air flow along the heat sink is caused by the temperature difference between heat sink and ambient. The higher the power dissipation, the higher will be the temperature difference and hence the heat transfer coefficient. When,

on the other hand, the air movement is forced by blowers or the like, the power dissipation rate does not greatly affect the heat transfer coefficient, and a fixed point on the power scale may be used as a reference.

5.4.1 Flat Heat Sinks

The use of the nomogram for flat heat sinks shown in Fig. 5-12 may be explained as follows, distinction being made between free convection and forced cooling.

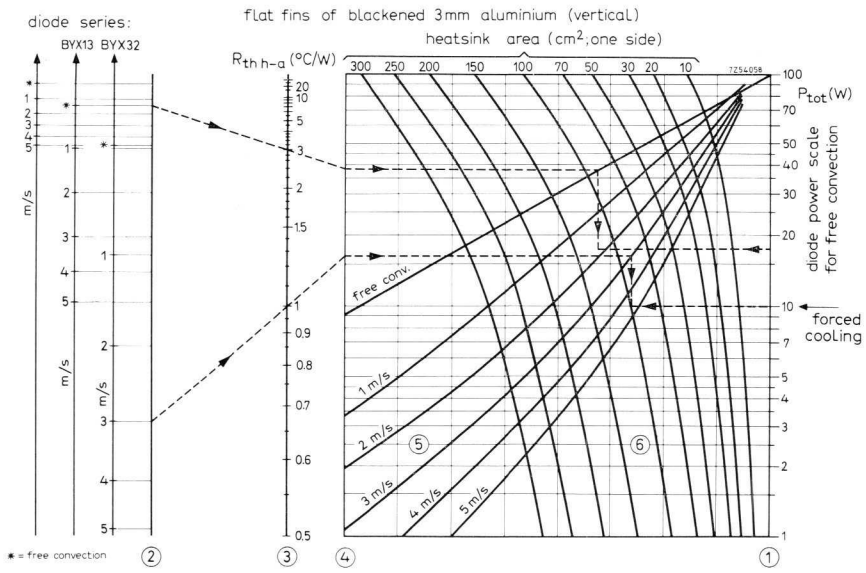


Fig. 5-12 Nomogram for finding data on flat heat sinks of blackened 3 mm thick aluminium (vertical).

Free Convection

Assume that the type of diode and its envelope, the power dissipation and the calculated maximum value of the thermal resistance from heat sink to ambient are known. Draw a straight line from the point on line 2 that corresponds to the free convection point of the diode used, through the thermal resistance value on scale 3, to the vertical line 4. Then move horizontally to the free convection line. The intersection of the vertical

through this point with the horizontal through the power disipation value on scale 1 gives the required heat sink area (interpolate between the values of the lines 6).

Example
An example has been plotted in Fig. 5-12 for a BYX13 diode, dissipating 17.5 W at $T_{amb} = 73$ °C. According to the data sheets a thermal resistance from heat sink to ambient of 3 degC/W is required. The nomogram shows that the heat sink area should be 125 cm^2.

Forced Cooling

Assume that the type of diode and its envelope, the calculated maximum value of the thermal resistance from heat sink to ambient and the velocity of the cooling air stream are known. Draw a straight line from the point on line 2 that corresponds to both the air velocity and the type of diode, through the thermal resistance value on scale 3, to the vertical line 4. Then move horizontally through the appropriate line for the air velocity (lines 5) and from there vertically to the intersection with the horizontal line through the arrow "forced cooling" at scale 1. This intersection gives the required heat sink area (interpolate between the values of the lines 6).

Example
In the nomogram an example has been plotted for a BYX32 (27 Hex envelope) diode, for which a required thermal resistance from mounting base to ambient of 1.1 degC/W has been calculated and which will be cooled with a forced velocity of 3 m/s. Since the thermal resistance from mounting base to heat sink is 0.1 degC/W, the thermal resistance from heat sink to ambient should be 1 degC/W. The nomogram shows that in this case the required heat sink area is 100 cm^2.

It should be remembered that unless the heat sink is mounted vertically, the position corrector factor f_p, given in Table 5-2, should be taken into account.

Influence of ambient temperature

It should be kept in mind that the nomograms are for an ambient temperature of 30 °C, but for other ambient temperatures no correction need be made except where the removal of heat takes place mainly by radiation. This is the case with, for example, painted heat sinks (high emissivity) at free convection. For these heat sinks, therefore, at an ambient temperature of, say, 10 °C the values found in the nomogram are too high; the

correct $R_{th\ h-a}$ value is 5% lower. Similarly, at an ambient temperature of for example 60 °C the nomogram values are too low and should be increased by 10%. (Interpolate for intermediate temperatures.)

Conversely, when the nomograms are used to ascertain the surface area of the heat sink for a given required value of $R_{th\ h-a}$, the latter should be decreased accordingly for ambient temperatures in excess of 30 °C or increased for ambient temperatures below this value if removal of heat takes place mainly by radiation.

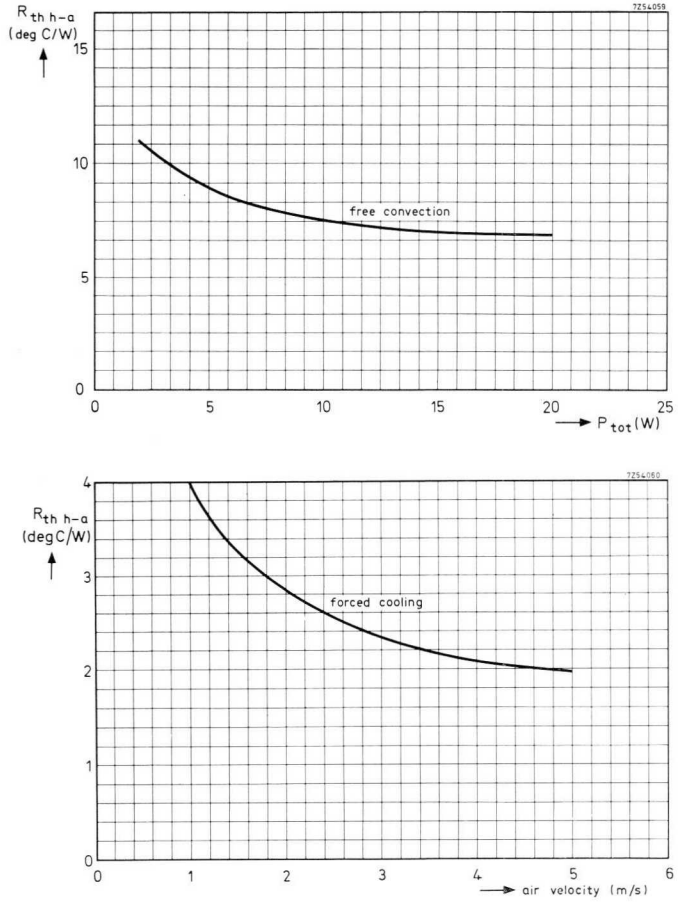


Fig. 5-13 Graph of $R_{th\ h-a}$ — die cast heat sink type 56256. (top) Free convection; (bottom) forced cooling.

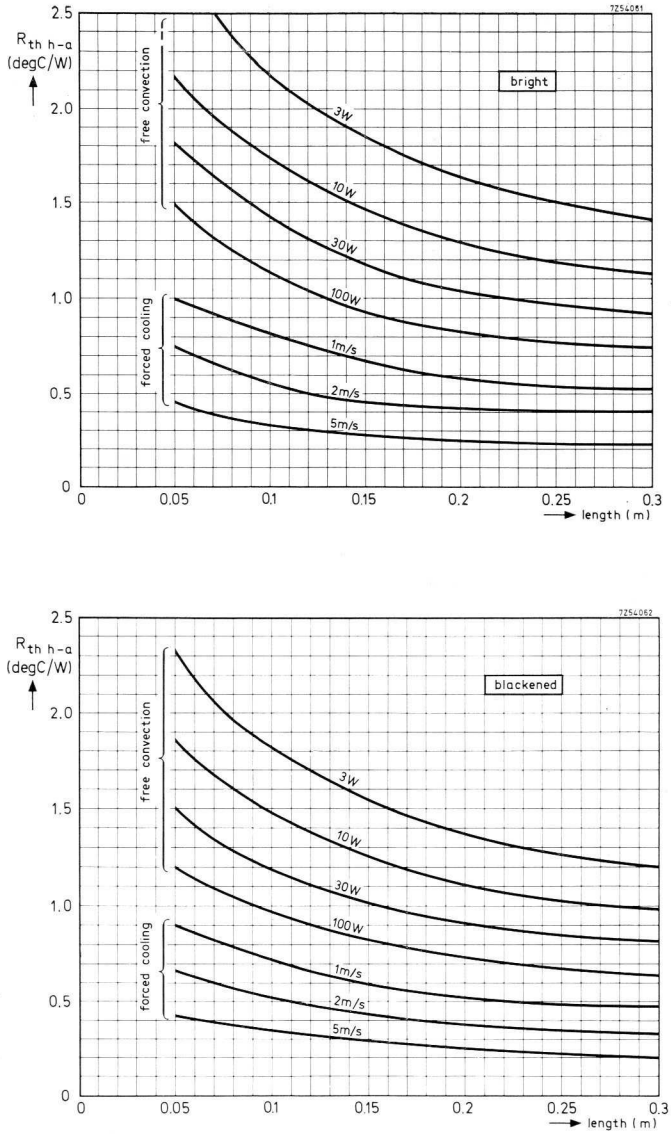


Fig. 5-14 Graph of $R_{th\ h-a}$ — extruded aluminium heat sink type 56230 (top) Bright; (bottom) blackened aluminium.

5.4.2 Die-Cast and Extruded Heat Sinks

When, instead of flat heat sinks, die-cast or extruded types are to be used, the designer is referred to other graphs, as for example those given in Fig. 5-13 for die-cast heat sinks and those given in Fig. 5-14 for an extruded one. These curves are not to be considered as nomograms since they depend on the type of diode used.

5.5 Use of Heat Sink Compounds

Heat sink compound or vacuum grease is often inserted between the mounting base of the power device and its heat sink, to reduce the thermal resistance from mounting base to heat sink. Measurements show that this thermal resistance decreases by a factor of about 3 when, for example, heat sink compound Dow Corning 340 is used and by a factor of about 1.5 when Dow Corning 280-300 vacuum grease is applied. However, the temperature difference between the mounting base and heat sink will not decrease by the same factor owing to the parallel path to ambient via the device envelope. When the thermal resistance drops, the mounting base temperature will also drop. As a result, the thermal resistance of the envelope increases, causing an increased power flow via the heat sink. The heat sink temperature will therefore be higher and the temperature drop from mounting base to heat sink will be larger than would be the case in the absence of a thermal resistance directly from the envelope to ambient.

Fig. 5-15 illustrates the effect of compound or grease on the temperature levels of mounting base and heat sink, at a given ambient temperature. Actual measurements indicate that in practice the fall-off in the mounting-base temperature is likely to be very small indeed. The use of compound or grease has no appreciable effect on heat removal, though they have their value in preventing corrosion of the surfaces in contact.

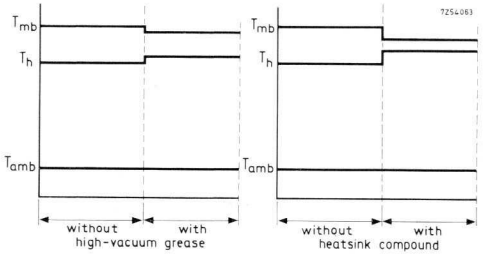


Fig. 5-15 Effect of high-vacuum grease or heat sink compound on mounting base and heat sink temperatures.

5.6 Practical Heat Sink Choice using the Data Sheets

This section gives several examples illustrating the use of the heat sink theories given above.

Example 1
Diode BYX25, mounted on a blackened vertical 3 mm aluminium heat sink, carries 15 A (single-phase circuit). Cooling is by free convection, and operation is at sea level. $T_{amb} = 40\ ^\circ C$ and $R_{th\ mb-h} = 0.5$ degC/W. Design a square heat sink to maintain the junction temperature within the rated value.

According to the data sheet $T_{j\ max} = 175\ ^\circ C$ and $R_{th\ j-mb} = 1.3$ degC/W. At 15 A average forward current, $P_{tot} = 28$ W. The simplified heat flow diagram is shown in Fig. 5-16.

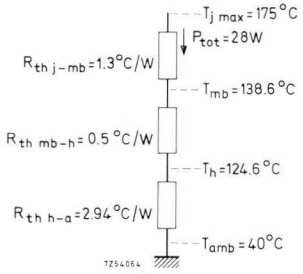


Fig. 5-16 Simplified heat flow diagram.

The mounting base temperature is:

$$T_{mb} = T_{j\ max} - P_{tot} R_{th\ j-mb} = 175 - 28 \times 1.3 = 138.6\ ^\circ C,$$

in accordance with the value derived from the corresponding graph in the data sheet. The heat sink temperature is therefore:

$$T_h = T_{mb} - P_{tot} R_{th\ mb-h} = 138.6 - 28. \times 05 = 124.6\ ^\circ C,$$

which gives for the permissible thermal resistance from heat sink to ambient:

$$R_{th\ h-a} = (T_h - T_{amb})/P_{tot} = (124.6 - 40)/28 = 3.03\ \text{degC/W}.$$

Since most of the heat is removed by radiation (blackened heat sink) and ambient temperature is 40 °C, 3% should be subtracted:

$$R_{th\ h-a} = 0.97 \times 3.03 = 2.94\ \text{degC/W},$$

whence

$$R_{th\ mb-a} = R_{th\ mb-h} + R_{th\ h-a} = 0.5 + 2.94 = 3.44\ \text{degC/W}.$$

To find the sink area by the method described in Section 5.4, we shall now refer to Fig. 5-12. For free convection and $P_{tot} = 28$ W we find an area of 110 cm^2, so a square sink with a side of 10 cm should be used.

In the following example $R_{th\ h-a}$ will be calculated once again for the

conditions given in Example 1, however by considering the direct heat flow from envelope to ambient separately.

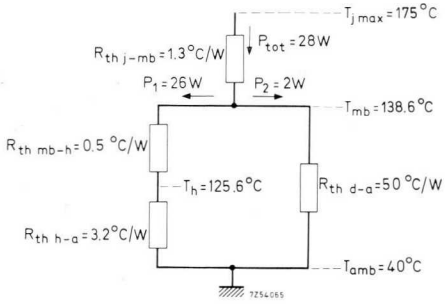


Fig. 5-17
Complete heat flow diagram.

Example 2
Fig. 5-17 shows the complete heat flow diagram; the values noted thereon are arrived at in the following way:

$$\Delta T_{mb-a} = 138.6 - 40 = 98.6 \text{ degC.}$$

Fig. 5-11 gives for an 11 Hex envelope $R_{th\ d-a} = 50$ degC/W. The heat flow direct to ambient, is therefore:

$$P_2 = \Delta T_{mb-a}/R_{th\ d-a} = 98.6/50 = 1.99 \text{ W} \simeq 2 \text{ W},$$

whence:

$$P_1 = P_{tot} - P_2 = 28 - 2 = 26 \text{ W},$$

being the heat flow from which the permissible thermal resistance $R_{th\ h-a}$ is to be derived. This gives:

$$T_h = T_{mb} - P_1 R_{th\ mb-h} = 138.6 - 26 \times 0.5 = 125.6 \text{ °C}.$$

Hence:

$$R_{th\ h-a} = \Delta T_{h-a}/P_1 = 0.97(125.6 - 40)/26 = 3.2 \text{ degC/W}.$$

(viz. 97% efficiency as before).

As a third example, the thermal resistance will be calculated for the heat sink design in Example 1, but applying the heat transfer theory given in Section 5.2.

Example 3
For a vertical heat sink of 10.5 cm × 10.5 cm and operation at sea level it follows from Tables 5-1 and 5-2 and Fig. 5-1 respectively that $l_c = 0.105$ m, $f_p = 1$ and $f_a = 1$. From Fig. 5-2 it is seen that, for $\Delta T_{h-a} = 117 - 40 = 77$ degC, $A = 7.3$ W/m^{2}degC.

This gives, from eq. (5-2):

$$h_c = f_p f_a A = 7.3 \text{ W/m}^2\text{degC}.$$

Table 5-3 shows that $\varepsilon = 0.8$, and according to Fig. 5-5, for a cooling fin in free space, $f_r = 1$. Fig. 5-6 shows that for $T_{amb} = 40\,^{\circ}\text{C}$ and $\Delta T_{h-a} = 77$ degC, $D = 9.9$ W/m^{2}degC. Hence, from eq. (5-4):

$$h_r = \varepsilon f_r D = 7.9 \text{ W/m}^2\text{degC},$$

whence

$$h_t = h_c + h_r = 15.2 \text{ W/m}^2\text{degC}.$$

The data sheet shows that the mounting hole diameter $d_2 = 0.013$ m and the mounting base diameter $d_1 = 0.027$ m, which gives, from eq. (5-6), for the heat input radius:

$$r_i = (d_1 + d_2)/4 = 0.01 \text{ m}.$$

Table 5-4 shows that the thermal conductivity of aluminium is $\gamma = 210$ W/mdegC, so that for a sink with a thickness t of 0.003 m, according to eq. (5-5):

$$r_h = \sqrt{(\gamma_s t/2h_t)} = 0.144 \text{ m},$$

as may also be derived from Fig. 5-7.

From eq. (5-7):

$$r_s = \sqrt{(lw/\pi)} = 0.059 \text{ m},$$

whence, according to Section 5.2.5:

$$p = r_h/r_i = 14.4 \qquad \text{and} \qquad q = r_s/r_i = 5.9.$$

This gives, according to Fig. 5-9, $\eta_h = 0.92$. The total heat dissipating area a_t being $2 \times 0.011 = 0.022$ m^2, it follows from eq. (5-8):

$$R_{th\ h-a} = 1/\eta_h h_t a_t = 3.25 \text{ degC/W}.$$

Hence (see Fig. 5-17):

$$R_{th\ h-a} + R_{th\ mb-h} = 3.4 \text{ degC/W}.$$

Since the two heat paths act as resistors in parallel, the total thermal resistance from mounting base to ambient is therefore:

$$R_{th\ mb-a} = 3.4 \times 8.6/(3.4 + 8.6) = 2.44 \text{ degC/W}.$$

Summarizing, the methods of calculation given in Examples 1, and 3 yield for $R_{th\ mb-a}$ values of 2.62 degC/W and 2.44 degC/W respectively. The shorter method used in Example 1 is seen to be on the safe side by a $(2.62 - 2.44)100/2.62 = 7\%$ margin.

Finally an example dealing with the use of die-cast and extruded heat sinks will be given.

Example 4

Dode BYX25 operates at full load (20 A single phase). Assume $T_{amb} = 50\,^{\circ}\text{C}$ and $R_{th\ mb-h} = 0.5$ degC/W. Find the correct heat sink or extrusion length capable of maintaining the junction temperature within the rating.

According to the data sheet, $T_{j\,max} = 175\,^{\circ}\text{C}$, $R_{th\ j-mb} = 1.3$ degC/W and P_{tot} (at 20 A) = 38 W.

The heat sink temperature

$$T_h = T_{j\,\max} - P_{\text{tot}}(R_{th\,j-mb} + R_{th\,mb-h})$$
$$= 175 - 38(1.3 + 0.5) = 106.6\ ^\circ\text{C}.$$

Hence

$$R_{th\,h-a} = (T_h - T_{amb})/P_{\text{tot}} = (106.6 - 50)/38 = 1.49\ \text{degC/W},$$

which in the case of free convection and a painted heat sink should be corrected by 7% for $T_{amb} = 50\ ^\circ\text{C}$, whence:

$$R_{th\,h-a} = 0.93 \times 1.49 = 1.39\ \text{degC/W}.$$

If the diode BYX25 is mounted on a die-cast heat sink assembly Type 56256 the heat sink graph of Fig. 5-13*(bottom)* should be consulted. It will be seen that the horizontal line through $R_{th\,h-a} = 1.39$ does not intersect the free convection curve, so recourse must be had to forced cooling. Using the (uncorrected) $R_{th\,h-a}$ value of 1.39 degC/W yields an impractically high air velocity, which shows that a Type 56256 heat sink assembly is unsuitable for the BYX25 operating at full load.

To investigate the possibility of a Type 56230 (bright) extruded section, the graph of Fig. 5-14*(top)* will be consulted. The graph shows that to obtain a $R_{th\,h-a}$ value of 1.39 degC/W with free convection an extruded section with a length of 10 cm is required.

If type 56230 (blackened) is to be used, reference to Fig. 5.14*(bottom)* shows that a length of 5 cm is sufficient.

6 Protection against Voltage Transients

6.1 Voltage Transients and Diode Ratings

Semiconductor diodes generally have lower reverse voltage handling capabilities than thermionic rectifying elements. In semiconductor diodes there is a more or less abrupt change of dynamic reverse resistance from a very high value (low leakage current) to a very low value (avalanche breakdown region). This means that there is only a small safety margin between the maximum working reverse voltage of the diode and the voltage at which the diode may break down. For our semiconductor diodes a half cycle non-repetitive transient reverse voltage is specified in the data sheets, which is generally twice the continuous duty or crest working level; this additional reverse voltage handling capability is a valuable asset in achieving reliable operation.

In cases where transients are expected to exceed the maximum ratings, voltage suppressing elements must be incorporated in the circuit to restrict any overvoltage to within the maximum permissible value. Controlled avalanche diodes have a "built-in" transient suppressing mechanism, and so may operate at a continuous voltage level much closer to the breakdown value. This feature allows better utilization of the unit. In practice, however, care must be taken not to exceed the rated transient energy dissipation. This may require additional surge arresting elements in spite of the high transient absorbing capabilities of controlled avalanche diodes.

Overvoltage suppressing elements may operate in two ways: the transient energy may be dissipated in a resistance, or it may be temporarily stored in a capacitor. Both methods result in a reduced transient voltage amplitude.

In the subsequent section transient energy dissipating means are discussed, but switch-arcing, distributed capacities and the like are not considered. Where applicable, no-load conditions are assumed (worst-case considerations).

6.2 Voltage Transient Sources

Various sources which generate voltage transients are enumerated below.

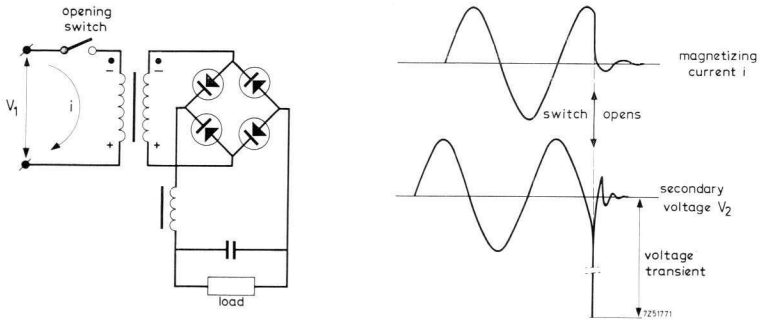


Fig. 6-1 Voltage transient due to opening of transformer primary (number of turns n, inductance L). No transient results if switch is opened at zero transition of the magnetizing current.

(*a*) *Transient due to interruption of magnetizing current (Figs 6-1, 6-2)*

This is the most serious effect encountered in practical circuit applications, especially under no-load conditions and in the case of choke input smoothing filters. The choke input prevents a transient from being dumped into the load or buffer capacitor, and the full transient must then be absorbed by the reverse biased power diodes. When the transformer primary is interrupted, the voltage and the magnetizing current will decay resonantly due to the inductance and the winding stray capacity in conjunction with circuit losses (ringing effect). The magnetic energy available $-\int i n \, d\phi$ is represented by the shaded area in Fig. 6-2. Depending on the instantaneous magnitude

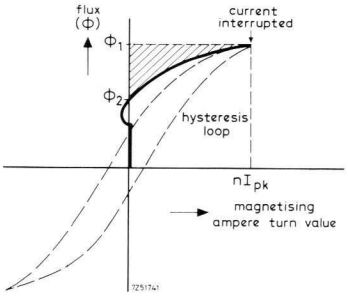


Fig. 6-2 Decay of magnetic flux at interruption of transformer magnetizing current. Shaded area represents the stored magnetic energy,

of the magnetizing current immediately prior to current interruption, a peak voltage transient may develop of 8 to 10 times the crest value

of the sinusoidal voltage. Such high levels are due to relatively low transformer stray capacities, so that an obvious means of suppressing voltage transients is to add parallel capacitive elements across the power diodes or the transformer windings. The voltage transient amplitude will also depend on the type of switch used. A switch or fuse that does not interrupt too abruptly will dissipate the stored magnetic energy in its arc, and limit the transient in this way. Contact chatter also absorbs some transient power in the arcs formed between bounces.

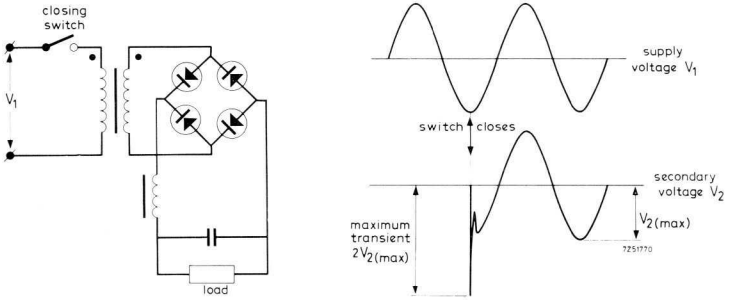


Fig. 6-3 Voltage transient at energization of transformer primary. No transient results if switch is closed when V_1 passes zero.

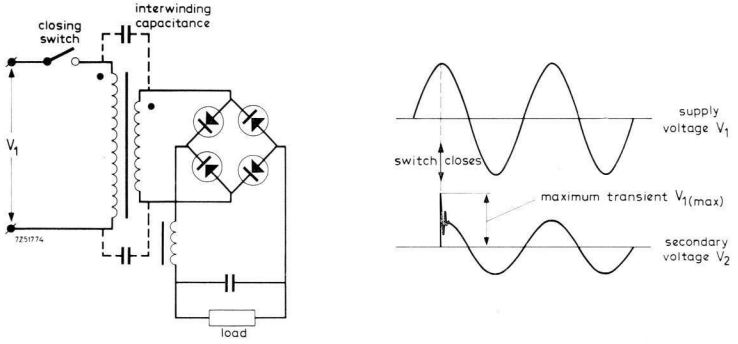


Fig. 6-4 Voltage transient at energization of a step-down transformer. No transient results if switch is closed when V_1 passes zero.

(*b*) *Transient due to energizing the transformer primary (Fig. 6-3)*
The maximum value of the voltage transient occasioned by energizing the transformer primary is twice the peak value of the secondary voltage.

(*c*) *Transient due to energizing a step-down transformer (Fig. 6-4)*
When energizing a step-down transformer, the maximum value of the voltage transient is equal to the primary crest voltage. The simplest method of obviating this type of transient is to interpose a grounded electrostatic shield in the winding to divert the primary voltage surge.

(*d*) *Transient due to an inductance across the input (Fig. 6-5)*
When a rectifier with an inductance across its input is switched the transient effect is similar to case (*a*). It must be borne in mind that the maximum available magnetic energy $LI_{pk}^2/2$ (where I_{pk} denotes the peak value of the magnetizing current) will increase at lower values of the parallel inductance.

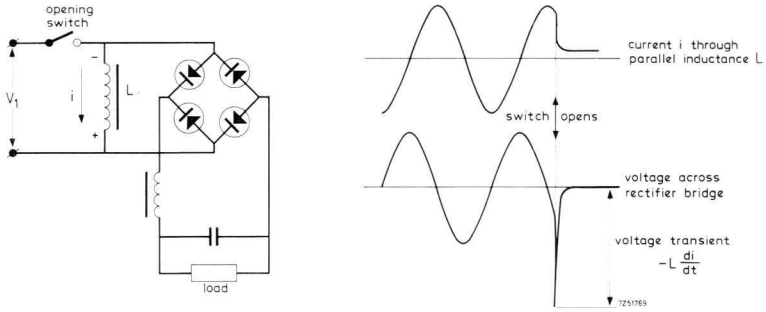


Fig. 6-5 Voltage transient due to opening of rectifier circuit with parallel inductance. No transient results if switch is opened when i passes zero.

(*e*) *Transient due to inductive load switching (Fig. 6-6)*
Both the inductive load and leakage inductance tend to maintain the flow of current despite switch opening. The load inductance sets up a voltage transient across the switch. Similarly, a voltage transient is

generated by the leakage inductance across the bridge rectifier. This transient will be less severe than in the case of interrupting the transformer primary, since the leakage inductance is relatively low.

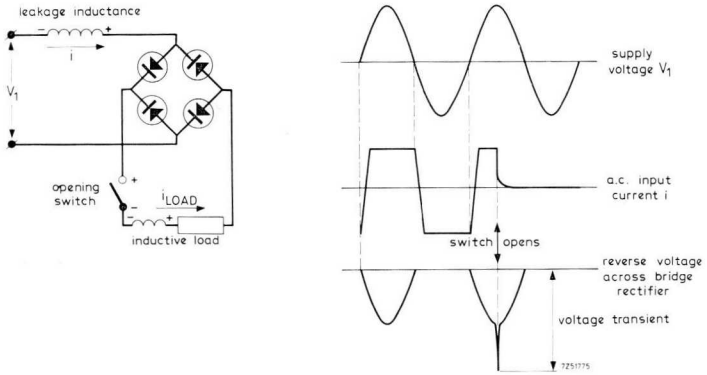


Fig. 6-6 Voltage transient due to opening of inductive load circuit. No transient results if switch is opened when a.c. input current passes zero.

(*f*) *Cyclic transients due to reverse recovery phenomena (Fig. 6-7)*
The occurrence of this phenomenon is clearly illustrated in Fig. 6-7. The accompanying voltage transient is governed by the frequency of the supply voltage, the load and the leakage inductance of the supply transformer as well as by the diode reverse recovery characteristic. Its amplitude may be substantial because the diode has just built up its potential barrier, and thus will exhibit a high reverse resistance.

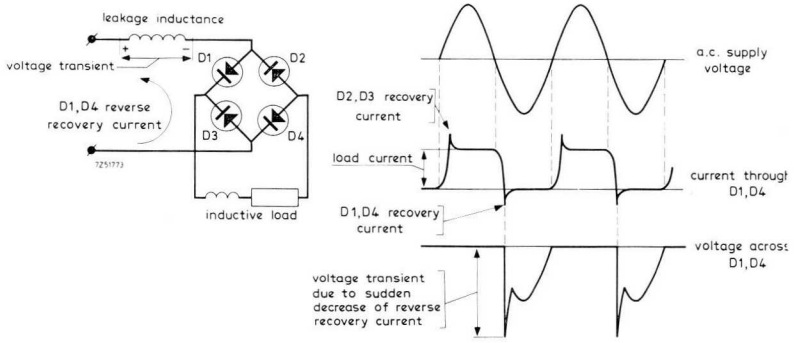


Fig. 6-7 Voltage transient due to reverse recovery phenomena. This is of a periodic nature.

(*g*) *Transients originating from parallel circuitry*
Voltage transients can be occasioned by motor switching, contactor operation and fuse blowing in adjacent circuitry.

(*h*) *Overvoltage due to a regenerative load (Fig. 6-8)*
This is actually not a transient effect, but a phenomenon of a more or less continuous nature, occurring for example when a hoist motor is driven by its load. A relay may be used to connect a dynamic braking resistor when a predetermined overvoltage level is reached. An electronic circuit to restrict regenerative overvoltages is discussed in Section 11.6.3.

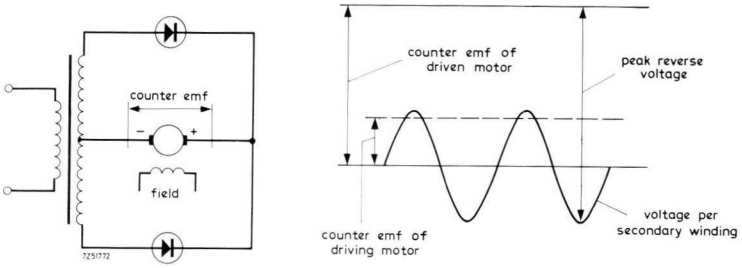


Fig. 6-8 Overvoltage due to a regenerative load.

(*i*) *Random power line disturbance*
An additional source of transients is random power line disturbance such as caused by lightning, which may give rise to considerable overvoltages merely by inductive effects. Such phenomena are most effectively suppressed by mounting surge arresters or similar devices directly acros the power line input.

Transient phenomena can have different effects on a semiconductor diode. They may cause breakdown and thus lead to failure because of excessive reverse dissipation. In the case of high-resistivity material (with a high breakdown voltage, cf. Section 2.2.3), flash-over across the interface between outer surface and junction rather than body breakdown is liable to occur, which may destroy the crystal locally. A reverse voltage transient during forward conduction may cause an excessive current flow, since an abundance of charge carriers is available to sustain such high current levels. All these phenomena call for different measures, as explained below, to ensure reliable operation even in the event of severe voltage transients.

6.3 Voltage Transient Suppression Methods

Transient suppression by series-connected capacitors and resistors is the method most commonly used. By shunting such networks across those parts of the circuit where the transient is apt to occur, the resistor will partially absorb the transient energy and reduce its voltage level. Capacitors do not dissipate energy, but temporarily act as energy storing elements during the transient, discharging the stored energy back into the circuit after the transient has passed. A diode protected by a capacitor then has more time to dissipate the same amount of transient energy, which increases its surge-energy absorbing capability.

Since inductance in the suppression circuit will reduce its effectiveness, carbon resistors and low-inductance capacitors should be used. It should be borne in mind that if electrolytic capacitors are used they may have too high an inductive reactance at high frequencies; they must then be bypassed by a type of capacitor (0.1 μF to 1.0 μF) capable of handling these components in the transient. A capacitor exceeding approximately 0.01 μF may need a series resistance to obviate ringing effects with inductances at the occurrence of transients. Capacitors may have to be bypassed by a bleeder resistance for safety reasons in order to drain off their charge on shut-down of the equipment.

Use of a VDR (voltage dependent resistor rather than an ordinary resistor will result in lower energy consumption. Normally, the VDR has a high resistance, but when a transient with a high voltage appears, the resistance drops to a much lower value.

In high-voltage systems spark gaps may be utilized as transient suppressors. A non-inductive series resistance of at least 1 Ω/V should then be mounted in series at the grounded side to limit the current when the gap breaks down.

Voltage transients can be limited by switching techniques, for example by slowing down the speed of switching. A switch or fuse that does not interrupt the current too abruptly will in itself limit transients to lower levels, since part of the transient energy is dissipated in the arc. Sequential switching is another useful aid. When the rectifier circuit is disconnected before the primary is opened (interlocked operation), voltage transients are diverted from the diodes.

6.3.1 The Use of Simple RC-Networks with Conventional Diodes

The following formulae constitute a conservative approach to the design

of *RC*-networks for protecting diodes against voltage transients, being based on the interruption of the transformer magnetizing current. As this is the most severe case for all circuit-imposed transients, the protecting components, which have been calculated, will be adequate for coping with all other types of voltage transient.

Voltage suppressing *RC*-series elements, to be shunted across each transformer leg (or diode) are dimensioned as follows. The capacity (in μF) and the resistance (in Ω) across the transformer primary should be:

$$C_1 = A_1 I_{magn}/V_1, \qquad R_1 = B_1/C_1, \tag{6-1a}$$

and across the transformer secondary (or diode):

$$C_2 = A_2(I_{magn}/V_2)k_t^2, \qquad R_2 = B_2/C_2, \tag{6-1b}$$

where V_1 = transformer primary r.m.s. voltage,
V_2 = transformer secondary r.m.s. voltage,
k_t = primary-to-secondary turns ratio ($= V_1/V_2$),
I_{magn} = primary magnetizing r.m.s. current.

The factors A_1, A_2, B_1 and B_2 are governed by the ratio of $V_{RSM\max}$, the maximum non-repetitive peak reverse voltage, to V_{RWM}, the circuit-imposed crest working reverse voltage (excluding transients) and can be derived from Table 6-1.

Table 6-1.

$V_{RSM\max}/V_{RWM}$	1.0	1.25	1.5	2.0
A_1	800	550	400	200
A_2	900	620	450	225
B_1	300	260	225	150
B_2	350	310	275	200

Example

A three-phase, full-wave bridge circuit, rated to deliver 15 A average current per diode, is supplied from the 380 V three-phase mains (secondary in star connection). The primary-to-secondary turns ratio is 1 : 1; the primary magnetizing current is 5 A; the power line fluctuations are $\pm$ 10%. Calculate the transient suppressing *RC*-series elements to be shunted across the transformer secondary.

Table 9.3 shows that the circuit-imposed crest working reverse voltage is:

$$V_{RWM} = 2.45 V_L = 2.45 \times 1.10 \times 380 = 1025 \text{ V}.$$

Thus, two diodes BYX13-1200R in series may be taken per bridge leg. $V_{RSM\max}$ per diode is 1200 V, and V_{RWM} per diode is 1025/2 = 513 V, whence

$$V_{RSM\max}/V_{RWM} = 1200/513 > 2.0,$$

which gives, from Table 6-1, $A_2 = 225$ and $B_2 = 200$. Hence, from eq. (6-1*b*):

$$C = 225(5/380)1^2 = 2.95\ \mu\text{F},$$
$$R = 200/2.95 = 68\ \Omega.$$

6.3.2 The Use of Simple RC-Networks with Controlled Avalanche Diodes

Controlled avalanche diodes are able to absorb a definite amount of transient energy in the reverse direction, as specified in their data sheets. If, however, the non-repetitive reverse power ratings are liable to be exceeded, transient suppressing elements must be provided to prevent damage. When controlled avalanche diodes are connected in series, the transient will be distributed across them, because they then all operate in their avalanche breakdown region. On the other hand, in the case of paralleled diodes, the full power surge will be absorbed almost entirely by a single diode, being the one having the lowest breakdown voltage.

The calculation of the requisite *RC*-series network to be shunted across the transformer secondary (or across the diodes) will be explained with reference to the following analysis and accompanying design examples. The calculations are based on worst-case conditions, i.e. at disconnection of the primary of an unloaded transformer. (In an actual rectifier system the transient energy will be dumped only into the leg that is reverse biased

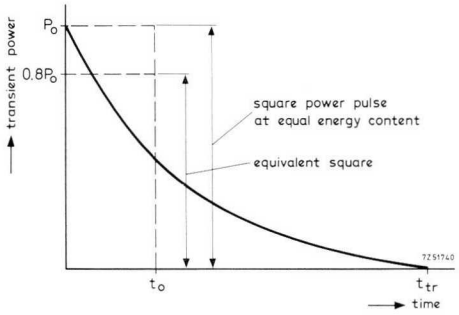


Fig. 6-9 Time function of transient power occurring at disconnection of transformer primary, and equivalent power pulses.

at the instant the transformer primary is switched off.) The magnetic energy stored in the transformer core is released when the magnetizing current is interrupted, and the transient power will decay (approximately) exponentially, as shown in Fig. 6-9. The duration of the surge, t_{tr}, expressed in s, may be approximated by the following formula:

$$t_{tr} = V_{RWM}/(V_{(BR)R} + \Delta V) \times 10^{-3},$$

where $V_{(BR)R}$ = reverse breakdown voltage at the maximum permissible junction temperature,

ΔV = additional voltage drop due to the dynamic resistance in the avalanching region (this voltage drop is assumed to be constant during the avalanching period).

This exponential power transient can be considered as a square pulse (of the same energy content), having the same maximum amplitude P_0 and pulse duration t_0, i.e. the time constant of the exponential function expressed by:

$$t_0 = t_{tr}/4. \tag{6-3}$$

The transient energy supplied by the transformer thus equals:

$$W = P_0 t_0. \tag{6-4}$$

Basing the peak junction temperature calculations on a square pulse of amplitude P_0 and duration t_0 would be too conservative because actual transient extends over a period $4t_0$, allowing the junction area to cool down to some extent. To obtain approximately the same peak junction temperature, an equivalent square pulse of amplitude $0.8P_0$ may be substituted for the actual power transient, though the energy absorbed by the diode is in fact $P_0 t_0$.

If the whole of the transformer energy can be absorbed by the diode(s), no transient suppressing elements need be incorporated, but where the energy content of the transient exceeds the non-repetitive reverse power ratings of the diode, protection means must be provided. This can be achieved by shunting the transformer secondaries by *RC*-series networks; the maximum capacity C required (expressed in μF) can be derived from the following empirical formula:

$$C = 10^6(W - nP_{RSM\max}\, t_0)/(nV_{(BR)R\min})^2, \tag{6-5}$$

where $P_{RSM\max}$ = reverse power rating for square power pulses of duration t_0, (W)

t_0 = $(V_{RWM}/4V_{(BR)R\min}) \times 10^{-3}$ (s)

$V_{(BR)R\min}$ = minimum reverse breakdown voltage at the maximum permissible junction temperature, (V)

n = number of diodes connected in series.

The required series resistance can subsequently be derived from:

$$R = B/C, \tag{6-6}$$

in which C is expressed in μF; the factor B_2, which here equals $V_{(BR)R\min}/V_{RWM}$, may be taken to be equal to that given by Table 6-1 for the ratio $V_{RSM\max}/V_{RWM}$.

The calculation procedure is now as follows. First, check whether the transient energy delivered by the transformer can be safely absorbed by the controlled avalanche diode in the time determined by eqs (6-2) and (6-3). In these equations the maximum reverse breakdown voltage $V_{(BR)R\max}$ should be used because this will give a minimum time in which the diode can absorb the given amount of energy, this being the most unfavourable condition. Then, if the non-repetitive peak reverse power ratings are endangered, the required transient suppressing capacity must be calculated from eq. (6-5). based on the minimum reverse breakdown voltage; this gives the maximum capacity required.

We shall first discuss a case where the controlled avalanche diodes are capable of handling the transient energy stored by the transformer.

Example

A three-phase bridge rectifier system having three controlled avalanche diodes BYX27-600 in series per leg is supplied by a 1 MVA transformer operating at 50 Hz, capable of delivering up to 9 Ws when its primary is disconnected. The secondary phase voltage is 640 V.

The circuit imposed crest reverse working voltage per diode is:

$$V_{RWM} = 640\sqrt{2}\sqrt{3}/3 = 523 \text{ V}.$$

The maximum reverse breakdown voltage for the BYX27-600 at $T_j = 25\,^{\circ}\text{C}$ is 1050 V. From eq. (3-3), or the data sheets, 170 V should be added because $T_{j\,\max} = 190\,^{\circ}\text{C}$. In addition, the dynamic resistance voltage drop in avalanche region = 170 V. Thus:

$$V_{(BR)R\max} + \Delta V = 1050 + 170 + 170 = 1390 \text{ V}.$$

From eq. (6-2):

$$t_{tr} = (523/1390) \times 10^{-3} \approx 0.4 \text{ ms}.$$

whence, from eq. (6-3):

$$t_0 = t_{tr}/4 = 0.1 \text{ ms}.$$

Part of the transient energy generated by the supply transformer is dissipated in the primary circuit breaker and stored by the secondary winding capacity. Assuming 50% of the transient energy to be delivered to a single leg, any one of the three diodes connected in series may have to absorb:

$$W = 9/(2 \times 3) = 1.5 \text{ Ws}.$$

From eq. (6-4) the maximum transient power per diode is:

$$P_0 = W/t_0 = 1.5/10^{-4} = 15 \text{ kW}.$$

The equivalent power pulse P_{eq} at $t_0 = 0.1$ ms is 0.8 times this value, i.e. 12 kW. The data sheets specify that for 0.1 ms pulse duration, $P_{RSM\max} = 17$ kW (at $T_j = 190\ ^\circ\text{C}$). This exceeds the effective transient power, so that no transient suppressing elements need be provided.

In the following example transient suppressing elements cannot be dispensed with; the requisite values will be calculated.

Example

A three-phase bridge rectifier is supplied by a 500 kVA transformer operating at 50 Hz and capable of delivering up to 7.5 Ws of transient energy when the transformer primary is disconnected. The secondary phase voltage is 220 V. Three controlled avalanche diodes BYX23-600 are connected in parallel per leg.

The circuit-imposed crest working reverse voltage per diode is:

$$V_{RWM} = 220\sqrt{6} = 540 \text{ V}.$$

The maximum reverse breakdown voltage for the BYX23-600 at $T_j = 25\ ^\circ\text{C}$ is 1050 V. Adding 170 V because $T_{j\max} = 190\ ^\circ\text{C}$ and putting $\Delta V = 190$ V gives:

$$V_{(BR)R\max} + \Delta V = 1050 + 170 + 190 = 1410 \text{ V}.$$

From eqs (6-2) and (6-3):

$$t_0 = (540/1410)/4 = 0.1 \text{ ms}.$$

Again assuming 50% of the transformer transient energy to be delivered to a single leg, and keeping in mind that now one diode will absorb almost all of the energy content of the transient, any one diode may have to absorb:

$$W = 7.5/2 = 3.75 \text{ Ws}.$$

From eq. (6-4) the maximum transient power per diode is:

$$P_0 = W/t_0 = 3.75/10^{-4} = 37.5 \text{ kW}.$$

At $t_0 = 1$ ms this corresponds to an equivalent power pulse P_{eq} of 0.8 times this value, i.e. 30 kW, which is far in excess of the value of $P_{RSM\max} = 6.4$ kW derived from the data sheets for a square pulse of duration 0.1 ms at $T_j = 190\ ^\circ\text{C}$. Therefore, it will be necessary to shunt the transformer secondaries by *RC*-series networks. The calculation of the maximum capacity required should be based on the minimum reverse breakdown voltage of 750 V at $T_j = 25\ ^\circ\text{C}$. Adding again 125 V because $T_j = 190\ ^\circ\text{C}$ gives:

$$V_{(BR)R\min} = 750 + 125 = 875 \text{ V},$$

whence, from eqs (6-2) and (6-3):

$$t_0 = V_{RWM}/4V_{(BR)R\min} = 540/4 \times 875 = 0.15 \text{ ms}.$$

According to the data sheet $P_{RSM\max} = 5.5$ kW for a square pulse of 0.15 ms duration at $T_j = 190$ °C, which means that the diode can absorb:

$$P_{RSM\max}\, t_0 = 5.5 \times 0.15 = 0.83 \text{ Ws}.$$

Hence, from eq. (6-5), for $n = 1$:

$$C = 10^6(3.75 - 0.83)/875^2 = 3.8 \ \mu\text{F}.$$

According to Table 6-1, for

$$V_{(BR)R\min}/V_{RWM} = 750/540 = 1.4.$$

we find $B_2 = 290$, which gives from eq. (6-6):

$$R = 290/3.8 = 76 \ \Omega.$$

To safeguard the diodes a capacitor of 3.9 μF in series with a 68 Ω resistor may thus be shunted across each transformer secondary (phase to neutral).

6.3.3 Suppression of Cyclic Transients

In the case of cyclic commutation from one diode to another, reverse recovery phenomena will occur in the switched-off diode, giving rise to a reverse current. This reverse current will induce a magnetic field in the leakage inductance of the transformer. At the instant the switched-off diode ceases to conduct and the diode current drops to zero, this field produces a transient which is only partly absorbed by the small internal capacity of the diode. As a consequence, there is a risk of the reverse voltage ratings of the diode being exceeded.

The transient absorbing capability can be raised to the required level by shunting a capacitor across the diode. The requisite additional capacity C is dictated by the condition that the energy $\frac{1}{2}CV^2$ at a voltage smaller than the $V_{R\max}$ value of the diode shall exceed the energy $\frac{1}{2}Li^2$ of the commutation transient. As a rule the commutation energy is comparatively small so that no additional measures need be taken if suppression networks are incorporated at the secondary to cope with transients due to the magnetizing current. If not, a capacity ranging from 0.5 μF to 2 μF will usually be ample.

6.3.4 The Use of Complex Networks for Suppressing Voltage Transients

To suppress power line transients the most economical solution usually is to connect a common electrolytic capacitor and bleeder resistor (time constant about 2 s) via a diode bridge circuit across the mains supply,

as shown in Figs 6-10*a* and 6-10*b*. The low value of the line impedance imposes the use of large capacities; bypassing each line by paper or similar capacitors is therefore scarcely worth considering.

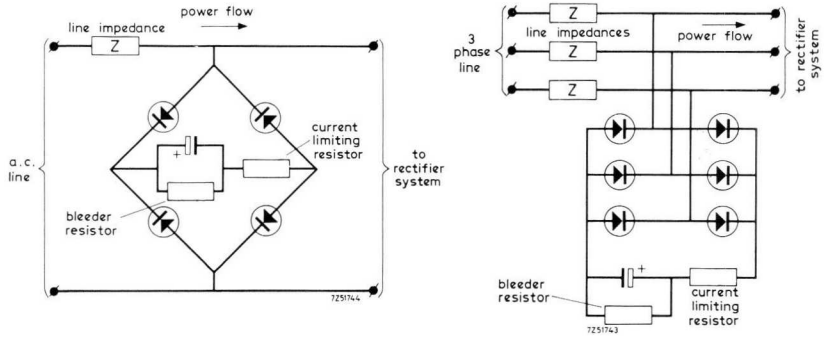


Fig. 6-10 Suppression of power line transients: (a) single phase; (b) three-phase.

Fig. 6-11 shows a more elaborate "crow bar" transient protection circuit to be connected across the power lines. This two-way system is inoperative under normal working conditions. However, if a transient occurs the controlled avalanche diode D_5 will break down either via D_4 and D_2 or via D_5 and D_1, depending on the polarity of the transient. One of the thyristors Th_1 ir Th_2 is then triggered and will conduct for the remainder of the half cycle, causing a line voltage drop across the line impedance. The speed of operation is very high since the turn-on time of the thyristor is extremely short (1 μs to 3 μs). Diodes D_1 and D_4 protect the thyristor gates against excessive reverse voltages.

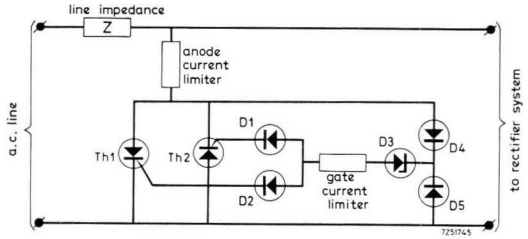


Fig. 6-11 Two-way "crow bar" power line transient protection.

The circuit of Fig. 6-12, to be connected across the rectifier output, is particularly useful in cases where the load cannot absorb transient energy

because it is inductive, or where it may be disconnected. Diode D_1 must be able to pass the capacitor charging current without damage, and withstand the anticipated peak rectifier output voltage. The value of capacitor C_1 depends on the actual application and should be determined by experiment. Resistor R_1 is usually selected so that the time constant R_1C_1 is approximately 2 s.

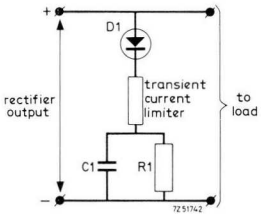


Fig. 6-12 Transient suppression network at rectifier output.

A similar network intended for individual diode protection is shown in Fig. 6-13. Its use will be attractive where a large capacity is required since the use of an electrolytic capacitor is permissible. Capacitor C_1

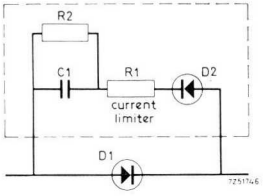


Fig. 6-13 Individual diode protection network.

charges up to the circuit-impressed crest working reverse voltage, developed across diode D_1, which is to be protected. Reverse voltage transients cause diode D_2 to conduct, and the transient energy will be stored in C_1, and absorbed by both R_1 and R_2.

7 Overcurrent Protection

7.1 Introduction

For a semiconductor diode circuit to operate satisfactorily, adequate provisions must be made to enable the system to survive abnormal overcurrent conditions. These conditions include situations varying between moderate overloads and heavy shorts. Depending on the duration of an overload, the mass of both the diode (thermal time constant approximately 1 s, heat storage capacity a few Ws/degC) and the heat sink (thermal time constant several minutes, heat storage capacity several tens of Ws/degC) can aid in removing excessive heat developed in the diode. During a short circuit considerable heat will develop in the junction area with negligible initial heat dissipation. Since the thermal time constant of the junction is so small (about 1 ms), the junction area will become thermally overloaded within a few ms. In a low-impedance system the current will have a high rate of rise and attain a considerable amplitude, and additional phases and circuit legs will help very little in increasing fault-carrying capacity, since permanent damage of the diodes may occur before commutation to another leg has taken place.

One proposition (but not usually an economic one) is to design a system to withstand the worst possible fault current on a continuous basis. This will require an installation rated for many times the normal load current, but such a system is seldom acceptable because of economic reasons or available space. The alternative is to incorporate fast-acting protection equipment to prevent full short-circuit current from reaching the diodes.

The protective devices now widely used stem partially from earlier developments when semiconductor rectifiers were unknown. The fast-acting, high-power shorting switch, originally evolved to safeguard mechanical contact rectifiers, still proves an effective means for the protection of semiconductor diodes.[9] The current-limiting safeguarding device, such as the explosive type surge-current limiter with extremely short current-interrupt time, is another valuable development in this area; it has the added advantage in that it will relieve rectifier transformers, busbars, and associated electrical gear from excessive magnetic stresses, these being proportional to the square of the peak fault current. Develop-

ment of protection devices for modern rectifier installations is still progressing.

Short circuits may be categorized as follows:

— *Diode failures* rarely occur in practice, but if a diode fails it is unfortunately apt to form a short circuit rather than an open circuit. Such a failure will always give a direct line-to-line short circuit, due to the low forward resistance of good diodes in adjacent circuit legs (see Figs 7-1 and 7-2), except when used in single-phase, half-wave circuits.

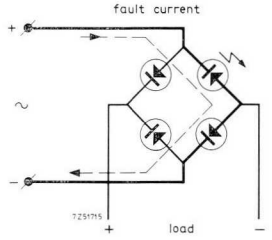


Fig. 7-1 Faulty diode in single-phase full-wave rectifier circuit.

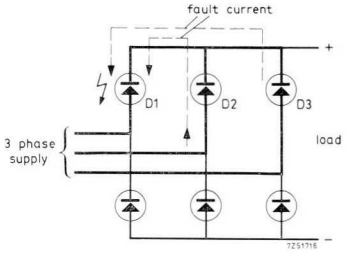


Fig. 7-2 Faulty diode in three-phase full-wave rectifier curcuit.

— *External shorts in the supply or load* are highly improbable in a well designed system. Depending on the type of load, shorts from the load side might occur due to operational errors, for example.

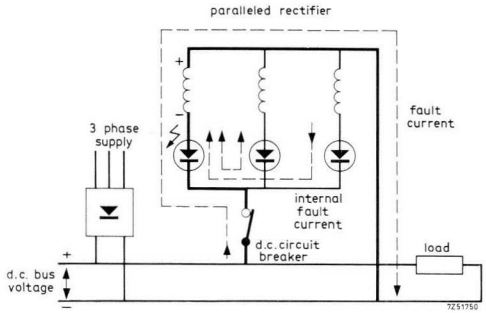


Fig. 7-3 Faulty diode in parallel rectifier half-wave.

— *External shorts in a paralleled rectifier* with star configuration may result in a heavy short circuit, since the d.c. voltage is sustained by the phase voltage feeding the shorted unit (Fig. 7-3). Bridge type rectifiers present an external short only when diodes in opposite legs fail (see Figs 7-4*a* and *b*).

To protect a semiconductor power diode against short-circuit conditions, consideration must be given to its permissible I^2t-value, which must exceed the I^2t-value required for the protective device to open the circuit. Other properties of the protective device such as cut-off currents and voltage transients during interruption must never exceed the surge current ratings and the non-repetitive voltage ratings of the diodes under protection.

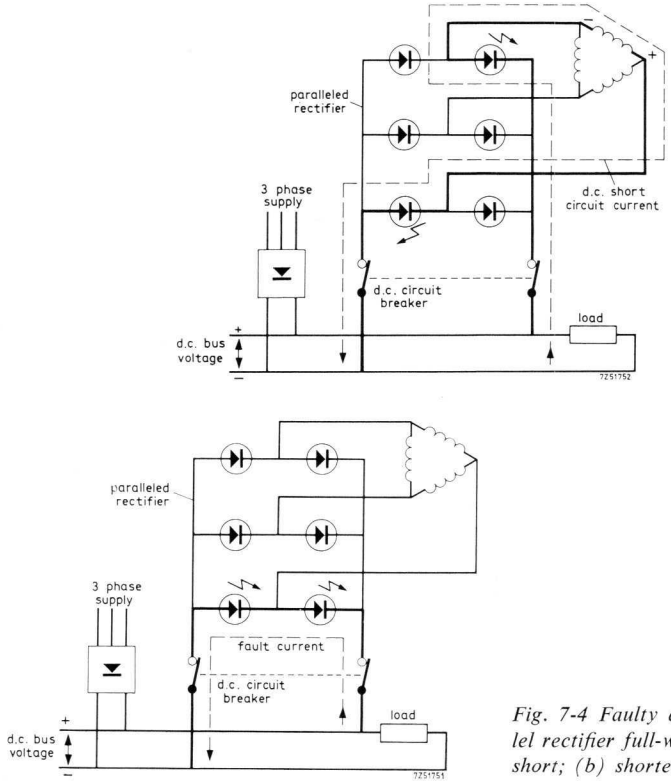


Fig. 7-4 Faulty diodes in parallel rectifier full-wave (a) direct short; (b) shorted via supply.

7.2 The Short-Circuit Phenomenon

In the case of a sustained d.c. short circuit, the steady-state current flowing through the diode will be sinusoidal and of half cycle duration. Its peak value is equal to the crest value of the potential symmetrical short-circuit current, i.e. the current flowing after decay of asymmetric phenomena at initiation of the short.[10],[11] (See Fig. 7-5.)

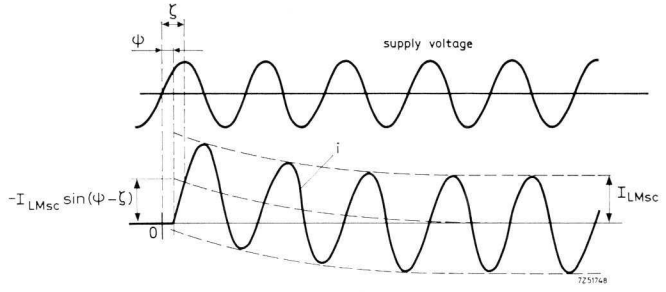


Fig. 7-5 Decay of diode current immediately after short circuit load applied

The instantaneous value of the short-circuit current may be expressed as:

$$i = I_{LMsc}\{\sin(\omega_S t + \psi - \zeta) - \sin(\psi - \zeta)\exp(-R_{sc}t/L_{sc})\}, \quad (7\text{-}1)$$

where I_{LMsc} = available peak steady-state line fault current,
ω_S = angular frequency of the supply voltage,
t = time duration following initiation of the short,
ψ = phase angle at which the short is initiated, referred to the preceding positive-going zero transition of the a.c. supply voltage,
$\tan\zeta$ = short-circuit reactance ($X_{sc} = \omega L_{sc}$) over the ohmic resistance (R_{sc}).

It may be seen that the fault current consists of a sinusoidal time function with an exponential component superimposed. The latter component gives rise to an asymmetric phenomenon and will decay to almost zero within 5 to 6 power cycles during a sustained short, leaving only the steady-state sinusoidal current. This indicates that in any practical system the series impedances of transformers and similar elements are mainly inductive.

The exponential time function will be zero for both $L = 0$ and $\psi = \zeta$, i.e. no current asymmetry will occur in a purely ohmic circuit, or in cases where a short occurs at a phase delay equal to the power factor angle of the short circuit. Likewise, in the imaginary case of a purely inductive circuit with zero ohmic losses, a constant asymmetry may result since under these conditions the exponential time function will become a d.c. component, namely $I_{LMsc} \sin(\zeta - \psi)$.

For all practical purposes, the first fault current pulse will be decisive because a protective device will have opened the circuit long before the second (negative) current pulse can occur. The amplitude of this first pulse can be shown to become maximum when a short occurs at the moment the supply voltage passes zero ($\psi = 0$). The relevant equation expressing the instantaneous value of the short-circuit current is found from eq. (7-1) by substituting $\psi = 0$:

$$i = I_{LMsc}\{\sin(\omega_s t - \zeta) + \sin \zeta \cdot \exp(-R_{sc} t \omega_s / X_{sc})\}. \qquad (7\text{-}2)$$

The degree of current asymmetry is determined by the offset factor, i.e. the ratio of the first pulse peak asymmetric fault current I_{LMsc0} to the steady-state peak fault current I_{LMsc}. The offset factor is a function of the short-circuit parameter R_{sc}/X_{sc} and will range from 1 for $R_{sc}/X_{sc} = \infty$ (purely ohmic circuit) to 2 for $R_{sc}/X_{sc} = 0$ (purely inductive circuit). A practical offset factor value is 1.5 ($R_{sc}/X_{sc} \approx 0.25$).

The above theory is illustrated by the graphical representations shown in Figs 7-6, 7-7, 7-8 and 7-9.

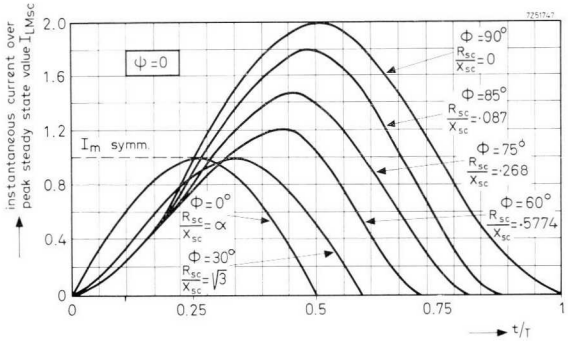


Fig. 7-6 Plot of i/I_{LMsc} against t/T for various ratios R_{sc}/X_{sc}.

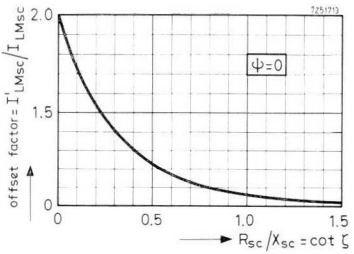


Fig. 7-7 Plot of I_{LMsc}'/I_{LMsc} against R_{sc}/X_{sc}.

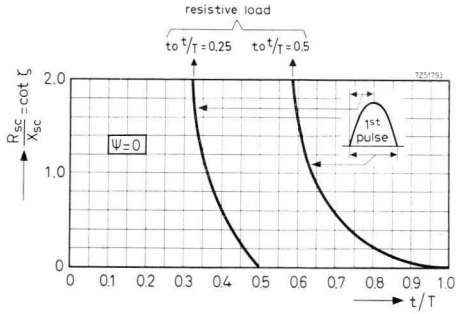


Fig. 7-8 Plot of R_{sc}/X_{sc} against t/T.

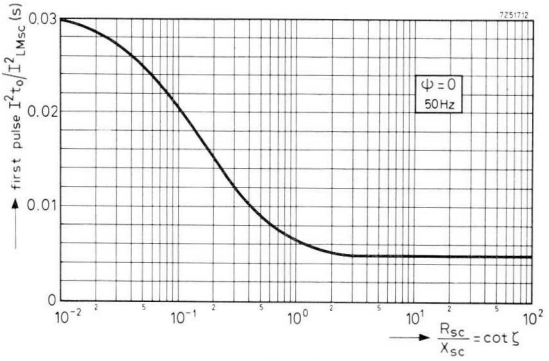


Fig. 7-9 Plot of first pulse I^2 to/$I_{LMsc}{}^2$ against R_{sc}/X_{sc}.

The maximum possible first pulse I^2t-value (worst case) for any circuit parameter $\tan \zeta = X_{sc}/R_{sc}$ is found by squaring and integrating eq. (7-2) over the period of the first pulse (Fig. 7-6). The graph can be used to

find the first pulse I^2t (worst case) value, for a circuit of a given R_{sc} and X_{sc}, by multiplying the value given by the curve by $I_{LMsc}{}^2$.

The initial rate of rise of the fault current depends on the ratio R_{sc}/X_{sc} and on the phase angle ψ. The maximum rate of rise takes place when a short occurs at the maximum supply voltage ($\psi = \pi/2$ or $3\pi/2$), independent of R_{sc}/X_{sc}. The minimum rate of rise occurs where the largest amplitude of the first current pulse may be expected, i.e. at $\psi = 0$ or π (see Fig. 7-10). This is of importance when overcurrent protective devices are used, which rely on the sensing of the initial dI_{sc}/dt to detect a short circuit.

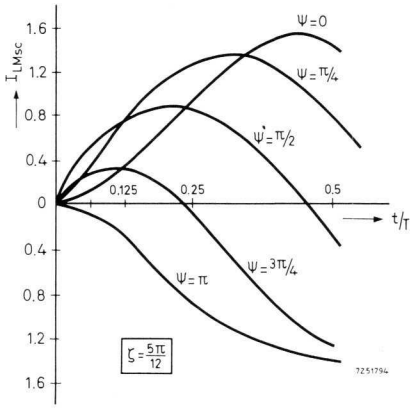


Fig. 7-10 Plot of I_{LMsc} against t/T for various values of ψ.

7.3 Short-Circuit Calculations

7.3.1 General Remarks

— All system reactances (reactance of source, reactances of preceding transformers, etc.) should be taken into consideration in order to arrive at the most realistic short-circuit current.

— In polyphase systems, the total volt-amperes (VA) equal the sum of the phase volt-amperes ($VA_{(ph)}$). In rectifier systems, the primary and secondary volt-amperes may differ owing to the difference between the primary and secondary current from factors. The following calculations are based on transformer *secondary* ratings.

— Series impedances of transformers and circuit elements present in the shorted circuit are predominantly inductive and may thus simply be added without large error.

7.3.2 Short-Circuit Volt-Ampere Value

In order to simplify the addition of series element effects in a system, one of the elements should first be selected as the base, volt-ampere value (usually the output transformer) and the per cent or per unit impedance (x) of each element then converted to an equivalent per cent or per unit impedance (x_{eq}), referred to the base volt-amperes. This is done by multiplying the per cent or per unit element impedance by the ratio of the base volt-amperes to the element volt-amperes. All the resulting equivalent values, derived for each element in turn, may then be added to obtain the equivalent per cent or per unit impedance for the total system; dividing the base volt-amperes by this total equivalent value gives the available net short-circuit volt-amperes.

For *single-phase supply*, this works out as follows, in per unit values (see Fig. 7-11). Per definition

$$x = X_L/X_{LOAD},$$

and

$$VA_{\text{nom}(ph)} /= V_L I_L = V_L{}^2/X_{LOAD},$$

the short-circuit volt-amperes being:

$$VA_{sc(ph)} = V_L{}^2/X_L,$$

whence

$$VA_{sc(ph)} = VA_{\text{nom}(ph)}/x. \tag{7-3}$$

Approximately, x equals the fraction of the nominal primary voltage required to produce the rated secondary load current per line, I_L, with the secondary winding shorted.

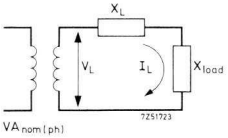


Fig. 7-11

For *three-phase supply*, we find for the total volt-amperes:

$$\left.\begin{aligned} VA_{\text{nom}} &= m_2 VA_{\text{nom}(sec)ph}, \\ \text{and} \qquad VA_{sc} &= m_2 VA_{sc(ph)}, \end{aligned}\right\} \tag{7-4}$$

where m_2 denotes the number of secondary phases. Hence, according to eq. (7-3):

$$VA_{sc} = VA_{\text{nom}}/X. \tag{7-5}$$

Example
Calculate the available short-circuit volt-amperes for a rectifier supplied by the system shown in Fig. 7-12.

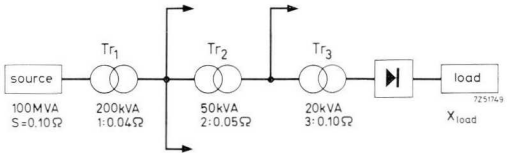


Fig. 7-12 Block diagram of rectifier system.

Taking as base transformer Tr_3 ($VA_{\text{nom}} = 20$ kVA), we have:

$x_{S\text{eq}} = (20/10^5)x_S$	$= (20/10^5)0.10$	$= 0.000\,02$	per unit
$x_{1\text{eq}} = (20/200)x_1$	$= (20/200)0.04$	$= 0.004$	per unit
$x_{2\text{eq}} = (20/50)x_2$	$= (20/50)0.05$	$= 0.02$	per unit
$x_{3\text{eq}} = x_3$		$= 0.10$	per unit
total x_{eq}		$\simeq 0.124$	per unit

Thus, from eq. (7-5):

$$VA_{sc} = VA_{\text{nom}}/x_{\text{eq}} = 20/0.124 = 161 \text{ kVA}.$$

7.3.3 Short-Circuit Current

Fault currents which may occur during short circuits can be derived in the following way.

For *single-phase supply* we know that:

$$VA_{\text{nom}(ph)} = I_L V_L \qquad \text{and} \qquad VA_{sc(ph)} = I_{Lsc} V_L,$$

where I_{Lsc} denotes the r.m.s. steady-state (symmetric) fault current. From eq. (7-3):

$$I_{Lsc} = VA_{sc(ph)}/V_L = VA_{\text{nom}(ph)}/V_L x. \tag{7-6}$$

The peak steady-state fault current is therefore:

$$I_{LMsc} = VA_{sc(ph)}\sqrt{2}/V_L = VA_{\text{nom}(ph)}\sqrt{2}/V_L x. \tag{7-7}$$

Due to asymmetric phenomena at the start of a short circuit, the maximum potential peak fault current for an offset factor of 1.5 is:

$$I_{LMsc0} = 1.5 I_{LMsc} = 3VA_{\text{nom}(ph)}/V_L x\sqrt{2}. \tag{7-8}$$

For *three-phase supply* we get:

$$VA_{\text{nom}} = 3VA_{\text{nom}(ph)} = V_{LL}I_L\sqrt{3},$$

and

$$VA_{sc} = V_{LL}I_{Lsc}\sqrt{3},$$

where V_{LL} denotes the line-to-line voltage. Thus, from eq. (7-5), the r.m.s. steady-state (symmetric) fault current per line becomes:

$$I_{Lsc} = VA_{sc}/V_{LL}\sqrt{3} = VA_{\text{nom}}/V_{LL}x\sqrt{3}, \tag{7-9}$$

and the peak steady-state fault current per line:

$$I_{LMsc} = VA_{sc}/V_{LL}\sqrt{(3/2)} = VA_{\text{nom}}/V_{LL}x\sqrt{(3/2)}. \tag{7-10}$$

The peak steady-state fault current may be expressed conveniently in terms of the rated d.c. load current I_o. For a three-phase bridge circuit, using Tables 9-5 and 9-6:

$$VA_{\text{nom}} = 1.05V_oI_o \qquad \text{and} \qquad V_{LL} = 0.428V_o\sqrt{3} = 0.74V_o.$$

Substituting these values in eq. (7-10), we find for an inductive or resistive load:

$$I_{LMsc} = 2I_o/x\sqrt{3}. \tag{7-11}$$

The above expression is equally valid for three-phase double star circuits with interphase transformer.[10]

A similar derivation yields for the six-phase half-wave circuit with inductive or resistive load:

$$I_{LMsc} = I_o/x\sqrt{3}, \tag{7-12}$$

and for the three-phase half-wave circuit with inductive load:

$$I_{LMsc} = I_o/x\sqrt{(3/2)} \tag{7-13}$$

the maximum peak potential fault current for an offset factor of 1.5 being:

$$I_{LMsc0} = 1.5I_{LMsc}. \tag{7-14}$$

7.3.4 Reactance per Line

For *single-phase supply* we obtain the reactance per line from eq. (7-3):

$$X_L = xV_L^2/VA_{\text{nom}(ph)}. \tag{7-15}$$

For *three-phase supply*, substitution of

$$VA_{\text{nom}} = 3VA_{\text{nom}(ph)} \qquad \text{and} \qquad V_{LL} = V_L / 3$$

in eq. (7-13) gives:

$$X_L = xV_{LL}^2 / VA_{\text{nom}}. \tag{7-16}$$

7.3.5 Additional Line Impedances

Impedances may be added in the lines to restrict the maximum potential peak fault current I_{LMsc0} to the safe maximum permissible peak fault current $I_{LMsc\ \max}$.

For *single-phase supply* the required per unit reactance is, according to eq. (7-8):

$$x_{\text{req}} = 3VA_{\text{nom}(ph)} / V_L I_{LMsc\ \max} / 2. \tag{7-17}$$

The per unit reactance to be added equals the required per unit reactance, minus the total per unit reactance:

$$x_{\text{add}} = x_{\text{req}} - x. \tag{7-18}$$

The line reactance to be added, $X_{L\ \text{add}}$ is related to x_{add} by the expression (cf. eq. (7-15)):

$$X_{L\ \text{add}} = x_{\text{add}} V_L^2 / VA_{\text{nom}(ph)}. \tag{7-19}$$

The required reactor may be incorporated in either the primary or the secondary circuit. The requisite inductance of the reactor to be connected in series with the secondary is:

$$L_{\text{add}\ 2} = X_{L\ \text{add}} / \omega_S. \tag{7-20}$$

When the reactor is connected in series with the primary, we need:

$$L_{\text{add}\ 1} = k_t^2 L_{\text{add}\ 2}. \tag{7-21}$$

For *three-phase supply*, we substitute in eq. (7-17):

$$VA_{\text{nom}} = 3VA_{\text{nom}(ph)} \qquad \text{and} \qquad V_{LL} = V_L / 3,$$

which gives

$$x_{\text{req}} = VA_{\text{nom}} / (3/2) / V_{LL} I_{LMsc\ \max}. \tag{7-22}$$

Once again, the per unit reactance to be added equals the required per unit reactance minus the per unit circuit reactance:

$$x_{\text{add}} = x_{\text{req}} - x. \tag{7-23}$$

As above, the line reactance is, from eq. (7-19):

$$X_{L\,\mathrm{add}} = x_{\mathrm{add}} V_{LL}^2 / VA_{\mathrm{nom}}. \tag{7-24}$$

The required line inductance can be found from eq. (7-20) and when the reactor is taken up in the primary, from eq. (7-21).

7.3.6 Filter Chokes

Where filters with a choke are used, the latter will give a substantial fault current limiting action. During a short-circuit, the effective choke reactance $X_{L\,ch\,sc}$ will decrease due to saturation. For a well-designed choke, the effective reactance should be at least one quarter of the normal reactance. Hence:

$$X_{L\,ch\,sc} = \omega_S L_{ch}/4. \tag{7-25}$$

For *single-phase supply th*e per unit reactance contributed by the choke is, by analogy to eq. (7-15):

$$x_{ch\,sc} = X_{L\,ch\,sc} VA_{\mathrm{nom}(ph)} / V_L^2, \tag{7-26}$$

and for *three-phase supply*, by analogy to eq. (7-26):

$$x_{ch\,sc} = X_{L\,ch\,sc} VA_{\mathrm{nom}} / V_{LL}^2. \tag{7-27}$$

Example

A three-phase bridge circuit, rated at 250 V, 500 A, has two diodes BYX14-600 in parallel in each leg. The total value of x is 0.15 and R_{sc}/X_{sc} is taken to be 0.25. The supply frequency is 50 Hz. The line fuses are assumed to blow after the first fault current pulse. Calculate the inductance to be inserted per secondary phase.

According to Table 9-3:

$$VA_{\mathrm{nom}} = 250 \times 500 \times 1.05 = 131.2 \text{ kVA}.$$

The line-to-line voltage is

$$V_{LL} = V_0 \sqrt{3}/2.34 = 0.74 \times 250 = 185 \text{ V}.$$

From eq. (7-10):

$$I_{LMsc} = 131.2 \times 10^3 / [185 \times 0.15 \sqrt{(3/2)}] = 3860 \text{ A}$$

or, from eq. (7-11)

$$I_{LMsc} = 2 \times 500 / 0.15 \sqrt{3} = 3860 \text{ A}.$$

From Fig. 7-7 the offset factor for $R_{sc}/X_{sc} = 0.25$ is seen to be about 1.5. Thus, the maximum potential peak fault current is:

$$I_{LMsc0} = 1.5 I_{LMsc} = 5790 \text{ A}.$$

Fig. 7-8 shows that the duration t of the first current pulse is about $0.8 \times 20 = 16$ ms.

From Fig. 7-9 it follows that the division of the first pulse (I^2t)-value by $I_{LMsc}{}^2$ is 0.0136 s, which gives:

$$I^2t = 0.0136 I_{LMsc}{}^2 = 0.0136 \times 3860^2 = 203\,000 \text{ A}^2 \text{ s}.$$

Assume, for a conservative design, that the I^2t-value of the diode, I^2t_d at 16 ms is equal to that at 10 ms, and that the current derating for parallel diodes under surge conditions is as for continuous duty. As will be shown in Section 8.3.3, a current derating factor f_d of 0.9 should be introduced for two paralleled diodes, which gives for the total I^2t value (I^2t_{tot}) for the two diodes:

$$I^2{}_{\text{tot}} = n^2 f_d{}^2 I^2 t_d,$$

where $n = 2$ denotes the number of diodes in parallel. The data sheet specifies that for 10 ms pulse duration, $I^2t_d = 32\,000$ A^2 s, whence:

$$I^2t_{\text{tot}} = 2^2 \times 0.9^2 \times 32\,000 = 103\,700 \text{ A}^2 \text{ s}$$

Because the I^2t_{tot}-value of the two diodes in parallel is lower than I^2t_0, the potential peak asymmetric fault current $I_{LMsc\,0}$ must be reduced to the safe value $I_{LMsc\,\max}$ according to:

$$I_{LMsc\,\max} = (I^2t_{\text{tot}}/I^2t_0)^{\frac{1}{2}} I_{LMsc\,0} = (103\,700/203\,000)^{\frac{1}{2}} 5790 = 4130 \text{ A}.$$

This reduction can be achieved by inserting reactors satisfying the condition:

$$x_{\text{req}} = (I_{LMsc0}/I_{LMsc\,\max})x = (5790/4130)0.15 = 0.21 \text{ per unit}.$$

This value may be checked against eq. (7-22), which gives:

$$x_{\text{req}} = 131.2 \times 10^3 \sqrt{3}/2/185 \times 4130 = 0.21 \text{ per unit}.$$

The reactance to be added is, from eq. (7-23):

$$x_{\text{add}} = x_{\text{req}} - x = 0.21 - 0.15 = 0.06 \text{ per unit}$$

From eq. (7-24):

$$X_{L\,\text{add}} = 0.06 \times 185^2/131.2 \times 10^3 = 0.01565\ \Omega = 15.65\ \text{m}\Omega.$$

According to eq. (7-20) the inductance to be added per phase, at 50 Hz operation, is therefore:

$$L_{\text{add}} = 15.65/100\pi = 50 \times 10^{-6} \text{ H} = 50\ \mu\text{H}.$$

Although, by increasing the reactance, the peak current surge can be reduced to a safe value, it should be recognized that load regulation is impaired thereby. Where this is undesirable, current-limiting protective elements must be used, or additional diodes must be connected in parallel to increase the value of I^2t_{tot}. The way in which the requisite number n of paralleled diodes may be calculated, follows from the following example.

Example

Calculate for the conditions given in the preceding example, the total number of parallel diodes required if it is intolerable to add reactors. In other words, the total I^2t-value of the parallel diodes (I^2t_{tot}) must be at least equal to the first crest I^2t-value (I^2t_0):

$$I^2t_{\text{tot}} = n^2 f_d{}^2 I^2 t_d \geqslant I^2t_0.$$

Solving this expression for n gives $n \geqslant 2.9$, which means that almost three diodes in parallel must be used. The I^2t_{tot}-value per leg is thus raised to:

$$I^2t_{tot} = n^2f_d^2I^2t_d = 216\,000 \text{ A}^2 \text{ s},$$

which indeed exceeds the I^2t_0-value of 203 000 A^2 s.

7.4 Protective Devices

7.4.1 Brief Survey

Elements intended for protection against short circuits may be subdivided into two major categories, namely:

— elements having the ability to restrict the rate of rise of the fault current or the magnitude of the steady-state fault current, such as
  transformer impedances,
  line reactors,
  inductances and resistances in the shorted d.c. load circuit;
— elements having the ability to interrupt current flow, such as
  a.c. circuit breakers in the primary or secondary line,
  rapid d.c. circuit breakers.
  shorting switches across the transformer secondary,
  fast-acting current limiting fuses,
  explosive-type surge current limiters.

The action of reactive elements in the a.c. circuit has been considered in Sections 7.3.4 to 7.3.6. Inductances on the d.c. side may limit the rate of rise of fault currents to such a value that a fast-acting protective device can interrupt the current before a disastrous level is reached.

It must be borne in mind that, when coordinating thermal protective devices with power diodes, these devices will react to the r.m.s. value of the current, whereas diodes respond essentially to heating alone. Since a diode is a non-linear circuit element, heating will be proportional to a current level somewhere between the r.m.s. and the average value. Such deviation must be taken into account.

The properties of several types of protective device are summarised in Table 7-1.

7.4.2 Circuit Breakers

Devices such as conventional circuit breakers have in common with fuses that they are intended to remove a short circuit before excessive heating can occur in the electrical gear, that is, to disconnect the entire circuit

Table 7-1. Properties of protective devices under short-circuit conditions.

type	pre-arcing time (ms)	arcing time (ms)	current limiting action	voltage transients across diodes	selective action	remote control facilities	power handling capabilities	auxiliary equipment	spare parts	maintenance
primary a.c. circuit breaker	20-120	5-10	no	yes	no	yes	high	few	few	once every year
secondary a.c. circuit breaker	20-120	5-10	no	no	no	yes	high	few	few	once every year
rapid d.c. circuit breaker	0.2-5	1-10	yes	yes	no	yes	restricted	few	few	once every year
shorting switch across secondary	< 0.1-3	—	only for diodes	no	no	yes *	high	rather extensive	few	once every year
fuse in primary a.c. line	0.1-0.5	1-10	yes **	yes	no	no	restricted	none	many	none
fuse in secondary a.c. line	0.1-0.5	1-10	yes	no	no	no	restricted	none	many	none
fuse in individual diode branches	0.1-0.5	1-10	yes	yes	yes	no	restricted	none	many	none
fuse in d.c. line	0.1-0.5	1-10	yes	yes	no	no	restricted	none	many	none
explosive type surge currrent limiter	0.1-0.3	1-10	yes	no	no	no	high	extensive	few	none

* not for ultra-rapid switch operated by an explosive cartridge ** on heavy shorts

from the supply in the event of an overload before permanent damage is caused to this gear. Being interposed between the supply mains and the installation, these devices must be slow-acting in order to handle the transformer inrush current. The relatively long current interrupt time renders this type of circuit breaker unsuitable for diode protection.

The rapid d.c. circuit breaker on the other hand may be used to advantage in situations where d.c. shorts are to be expected, or where rectifying units operate in parallel. It may obviate complete shutdown if a short develops in one of the units, as the fault current fed back into the shorted unit can be interrupted within 3 ms.

7.4.3 Shorting Switches

By a fast-acting shorting switch the secondary phases are short-circuited as soon as a predetermined fault current level is exceeded, the device being used in conjunction with a primary or secondary circuit breaker. Contact closing time may be less than 2.7 ms without arcing; peak asymmetric short-circuit current capabilities of up to 200 kA at several kV are possible.[9]

Contact opening can be motor-controlled, which makes the switch suitable for application in unmanned power stations for railway traction systems for example, where remote operation may be a requisite. Ultra-rapid shorting switches have an explosive-type contact drive, resulting in contact closing times below 1 ms.[12] Originally developed to protect mechanical contact rectifiers, the fast-acting shorting switch is an excellent means of diode overcurrent protection, since the diode current is immediately reduced to zero without voltage transients as soon as the contacts close. However, the preceding electrical gear must be capable of interrupting high power levels and withstanding excessive dynamic forces over the duration of the full short. A construction, proof against short circuit, means increased transformer impedance, and this may be intolerable for some applications.

7.4.4 Explosive-Type Surge Current Limiters

This type of protective device is tripped by electronic circuitry that senses fault current levels or detects a short by the excessive initial value of di/dt.[13],[14] The electronic circuitry discharges a capacitor across a three-electrode spark gap. The accompanying pulse energy (over 100 kW peak power) is applied to an explosive cartridge via a pulse transformer to interrupt the main current path.

Selective operation by means of such surge current limiters in a paralleled rectifier system, to obviate shutdown of the entire installation when one rectifier unit fails, may be achieved by the protective scheme shown in Fig. 7-13.

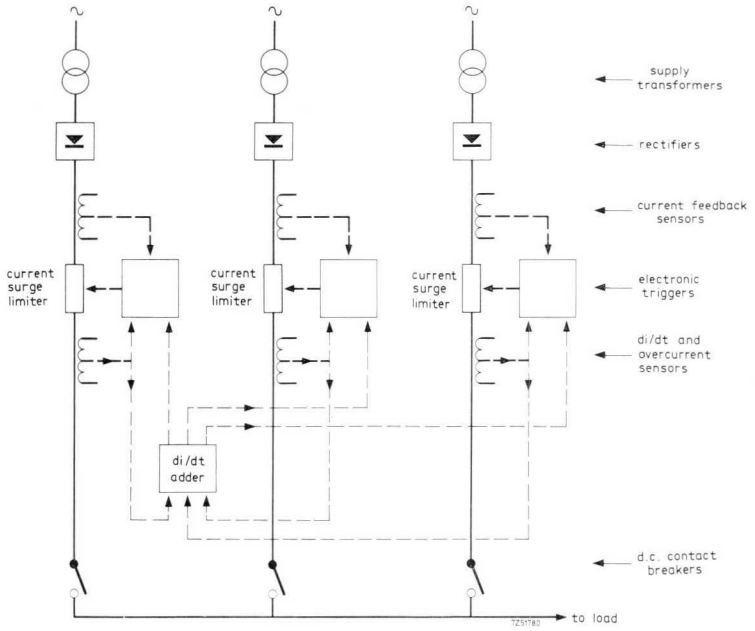


Fig. 7-13 Arrangement to prevent shutdown of an entire system when failure occurs in one rectifier branch.

7.5 Protective Measures for Specific Applications

Overcurrent protection system design is concerned with the type of installation, the reliability desired, and the continuity of operation required.

To maintain continuity of operation, diode redundancy will have to be used, and selective protection incorporated to isolate any faulty diode. Where redundancy of diodes is used, a suitable warning system should be incorporated to facilitate the finding of defective diodes and fuses during routine overhaul of the installation.

Further factors that will govern the selection of any particular protective system are:

— the possibility of a short-circuit in the d.c. load,
— the possibility of a d.c. busbar fault,
— the possibility of a short circuit between output transformer and rectifier,
— the likelihood of an internal short in a paralleled rectifier unit,
— the magnitude and rate of rise of the possible fault current.

Some specific applications are discussed below.

Electrochemical installations are characterized by continuous operation at a rated load. To achieve an optimum power factor and high efficiency together with an economic transformer design, 5% to 8% impedance will usually be selected, resulting in substantial fault current levels. There is little likelihood of d.c. busbar or load shorts in a well-designed system operating under the supervision of skilled personnel. Sometimes, however, when semiconductor rectifier units are operated in parallel with mercury arc rectifiers, shorts are unavoidable, such as those due to backfiring of the mercury arc rectifiers.[15] Saturable reactors, for adjustment of the d.c. output voltage, will limit the initial rate of rise of fault currents, and overcurrent protective circuitry can be incorporated to interrupt the reactor d.c. control current, thus limiting the rectifier output should a short circuit occur. In large installations, a shorting switch or surge current limiter should be used because of the high power-handling capability of these devices.

In *small electrochemical installations*, *supply systems for tramway* or *omnibus traction*, etc. the rapid d.c. circuit breaker is a suitable protective device. It can interrupt the circuit well within 5 ms, resulting in a substantial fault-current-limiting action. Traction supply systems are usually designed for continuous operation without failure, at loads exceeding the rated level by 50% to 60%.

Rectifiers in locomotives, fed by a.c. from overhead contact lines, are used to supply the traction motors with d.c. power. To achieve continuity of operation when part of the installation fails, and for economic transformer design, each motor will preferably have its own rectifier unit, with all rectifiers fed from a common secondary. A common, fast-acting shorting switch constitutes a suitable protection device for this type of installation, making possible resumption of operation after isolation of the rectifier unit at fault. Use of fuses to isolate faulty diodes may be considered unnecessary where they are connected in series, since under

these circumstances the risk of system breakdown due to shorted diodes is remote.

It must be borne in mind that the fluctuations in diode junction temperature are more pronounced where $16\frac{2}{3}$ Hz a.c. supply is involved; in addition, surges may be of a longer duration than in the case of conventional 50 Hz supply.

In *low-power installations* application of expensive, fast-acting circuit breakers is not generally an economic proposition. A better approach in this case is to use selective fusing in conjunction with a conventional type of circuit breaker on the primary side (see Section 7.6.4).

Selective protection is used to minimize replacement of fuses after any type of short circuit, or to isolate a defective diode where continuity of operation is a requisite. Branch fuses should only operate when a diode becomes defective, that is, they must not open due to an external short. When using series stacks, the necessity of branch fusing (which may give rise to excessive voltage transients when a branch is isolated due to a faulty diode) can be obviated by building extra voltage, tolerances into the system. This can be achieved by using either diodes of higher voltage rating, or more diodes in series than actually required by the application. This approach virtually eliminates the risk of shutdown of the entire equipment due to shorted diodes.

A suitable warning system should be incorporated to facilitate tracing of faulty diodes during maintenance. One of several possible methods is shown in Fig. 7-14. The warning device (relay or lamp) is placed as near as possible to the centre of the paralleled series stacks, to receive maximum voltage should any diode in the stack fail. Each warning device supervises a parallel pair of rectifier stacks.

An alternative scheme for isolating a defective branch is illustrated in Fig. 7-15. A trip coil of each isolating relay is connected across a bridge formed by a pair of diodes and their respective low-value series resistor R. When a diode becomes shorted, or open-circuited, the balance will be disturbed and the relay will come into operation.

Design of a protective system depends greatly on both the installation and the specific requirements. It is reasonable, therefore, that the system designer rather than the semiconductor manufacturer decide what level of protection is required for the particular application. It is not until the requirements have been determined, that the semiconductor manufacturer can recommend measures to attain these objectives. Table 7-2 gives a general idea of the protection suggested for different applications.

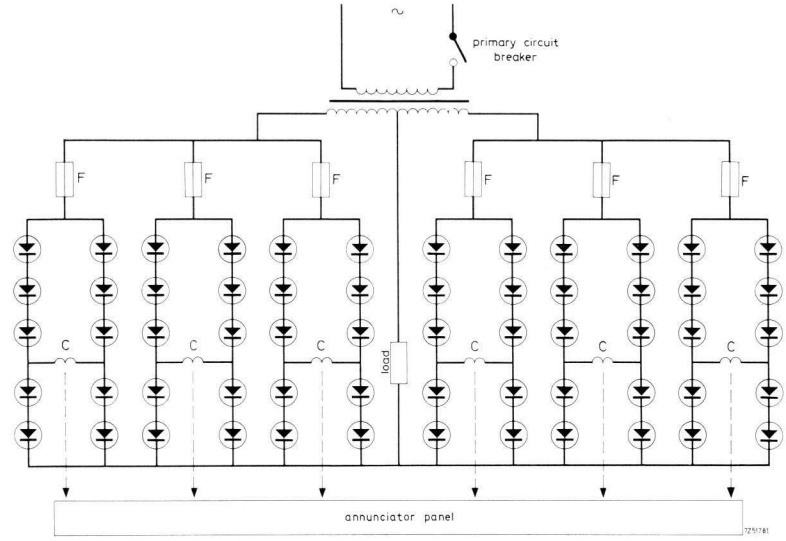


Fig. 7-14 Faulty diode warning system.

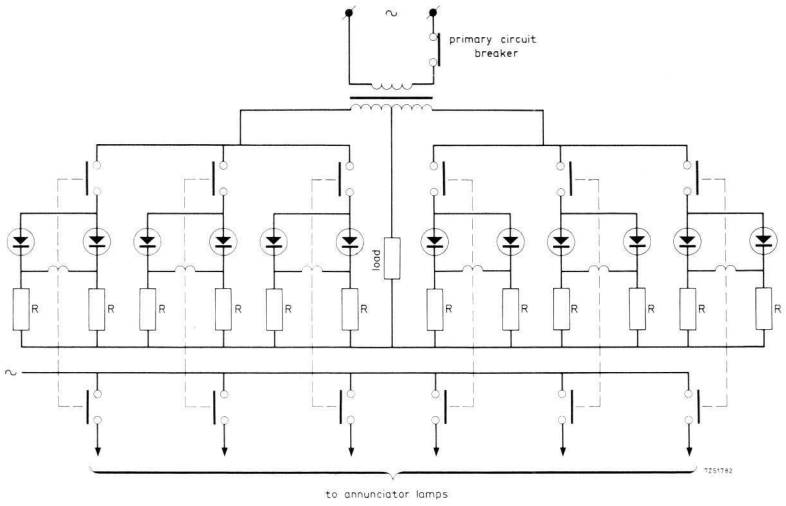


Fig. 7-15 Faulty diode warning system providing automatic isolation of defective branch.

Table 7-2. Application of protective devices in typical semiconductor rectifier installations.

protective device	electro-chemical plants		railway and tram way traction	welding equip-ment	rectifier systems		high-voltage rectifier installations		battery chargers	
	large sized	medium sized			medium sized	small sized	large sized	small sized	large sized	small sized
in primary line:										
circuit breaker	●	●	●	●	●	○	●	○	●	○
fuse						○		●		
current surge limiter					○					
in secondary line:										
fuse					○	○				
across secondary:										
fast-acting shorting switch	●	○	○				○			
at d.c. output:										
rapid circuit breaker		○	●		○				●	
fuse					○	○				●
current surge limiter	○									
in individual diode branches:										
fuse	●	●			○	○				

● recommended
○ to be added where required

7.6 Fusing of Power Diodes

When designing a diode rectifier with fuse protection, the I^2t-values of diodes and fuses must be compared, keeping in mind that the peak value of fuse cut-off current should not exceed the diode surge current rating, and that blowing of the fuse depends on the r.m.s. value of the current, whereas the diode is a non-linear device. In addition, the I^2t-value of the fuse is approximately constant during subcycle surges owing to fuse link geometry, whereas the I^2t-value of the diode will decrease as the surge duration decreases.

Fuse data (prospective current and virtual times) do not represent practical figures in the case of a subcycle blow; for critical circuit applications, fuse tolerances must be allowed for in the design. The following paragraphs are intended to give an insight into the operation of the fuse and its current-limiting action. When properly applied, the fast-acting fuse is an adequate means of protection for semiconductor diodes.

7.6.1 Current-Limiting Action

The current-limiting action under short-circuit conditions is shown in Fig. 7-16. The potential short-circuit current (first pulse of asymmetric current shown in broken line) is determined by the inductance inherent even in very low impedance supply systems. The fuse link will offer no substantial impedance during the melting period, and the actual short-circuit current will closely follow the potential fault current time function.

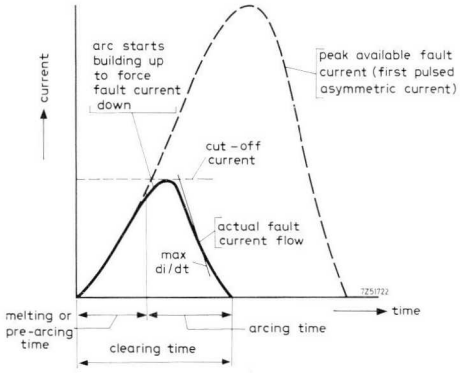


Fig. 7-16 Current limiting under short circuit conditions.

Upon melting of the fuse, an arc is struck and the net circuit voltage (difference between the arc and the supply voltage), in conjunction with the short-circuit impedance, reduces the current eventually to zero. The total time required to open the circuit after onset of the short, that is, the sum of the melting (pre-arching) time and the arcing time, is termed the clearing time t_{cl}.

A fuse is said to be "current-limiting" when its cut-off current (Fig. 7-16) is substantially lower than the potential peak fault current (ratios of 1 : 10 and greater). Current-limiting action will depend on the magnitude of the actual fault current. The energy which causes the fuse to melt, $(I^2t)_m$, increases with decreasing fault current, since heat in the fuse link is developed slowly, permitting heat dissipation to the filler material, fuse mountings and external circuit. A moderate fault current may flow during several cycles before the fuse will ultimately open (long-time blow), and no current-limiting action will occur. Where a heavy short is involved, the fuse link geometry will inherently control the melting time; heat is generated very rapidly in the fusing element, with virtually no heat flow to the surrounding media. Under these conditions the melting time of a fast-acting fuse will be less than a cycle, and current-limiting action will occur. The I^2t-value necesary to melt the fuse link will be essentially constant and independent of the available short-circuit current. At moderate overloads.

The energy dissipated by the arc, $(I^2t)_{arc}$, is governed by the fuse characteristics as well as circuit parameters. The rate of rise of the arc voltage determines the period of time required for the short-circuit current to attain the cut-off level after the fuse link has melted; the cut-off current is reached when the arc voltage equals the instantaneous a.c. supply voltage (see Fig. 7-17). Then, when the arc voltage exceeds the instantaneous supply voltage, the current is forced down at a decay rate di/dt equal to the quotient of the net circuit voltage (arc voltage minus supply voltage) and the overall short-circuit inductance. The arc voltage depends on the fuse voltage rating but, in the majority of cases, the magnitude of the d.c. supply voltage and its waveform during arcing are additional determining factors. When the arc voltage is high (assuming ample fuse voltage rating), the fault current will drop quite abruptly to zero, resulting in a relatively low value of $(I^2t)_{arc}$. Because high-voltage fuses open the circuit rapidly at minimum $(I^2t)_{arc}$-values, such fuse types may be used to advantage with semiconductor devices (the overall diode I^2t-rating must exceed the $(I^2t)_{cl}$-value of the fuse). It must be borne mind that

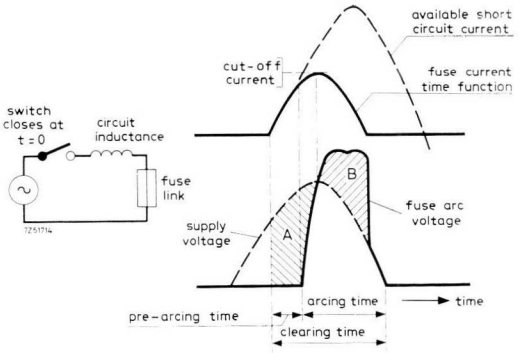


Fig. 7-17 Currents and voltages occurring during a short circuit.

diodes of a suitable voltage classification (capable of handling the arc voltage during interruption of the fault current) should be selected when using high-voltage fuses in paralleled diode branches.

An alternative to the use of fuses is to employ current derating, that is, using diodes of a higher current rating or paralleling a greater number of diodes than actually required by the application.

7.6.2 Fuse Arc Voltage

In a purely inductive circuit, the supply voltage

$$v = L \cdot \mathrm{d}i/\mathrm{d}t, \qquad \text{or} \qquad i = (1/L) \int v \cdot \mathrm{d}t.$$

If the circuit is closed, the current will start at zero level and show an initial rate of rise determined by the supply voltage, the inductance and the phase angle at which current starts to flow. The first current zero transition will occur when the integrated voltage-time function becomes zero (Fig. 7-18). This means that in an inductive circuit with zero losses, constant current asymmetry will result when current starts to flow at a time non-coincident with the voltage maximum (cf. Section 7.2).

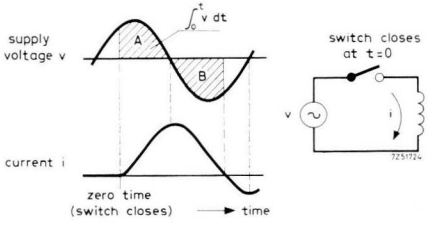


Fig. 7-18 First current zero transition after switch on.

When the switch is closed in the circuit of Fig. 7-17, an arc voltage will occur upon melting of the fuse. The instantaneous arc voltage must exceed the instantaneous supply voltage in order to force the fault current down to zero. When the fault current has been reduced to zero, the arc will quench abruptly, and the voltage across the fuse will become equal to the circuit supply voltage. Clearly, the fuse will open the circuit when the integrated time function of the voltage across the circuit inductance (referred to $t = 0$) becomes zero, that is, when area A equals area B. However, this theory is only approximately correct for any practical circuit since load current (generally of a much lower value) will already be flowing before the occurrence of a short, giving rise to an a.c. voltage drop across the inductance.

Fuses of a much higher voltage rating than the circuit supply voltage will generate a high peak arc voltage. This means that equality of the voltage-time areas as stipulated in Fig. 7-17 will be attained in a very short time, and the fuse will clear very rapidly with minimum $(I^2t)_{arc}$-values. In other words, application of a high fuse voltage rating minimizes the $(I^2t)_{cl}$-value passed to the circuit under protection. However, the higher voltage endangers good diodes in parallel branches, unless types with adequate voltage rating are selected. On the other hand, using a fuse with a voltage rating just exceeding the circuit supply voltage might jeopardize diodes under protection because such fuses open the circuit slowly and thus pass an excessive amount of energy before the fault current is interrupted.

A line fuse will produce only small voltage transients across the diodes when opening the circuit, unless rectifier systems protected by individual line fuses operate in parallel from a common supply transformer. It is permissible, therefore, to use line fuses with a comparatively higher voltage rating than the associated branch fuse ratings.

7.6.3 Prospective Current and Virtual Time

As a convenient way of indicating the fuse performance, manufacturers publish data on prospective current and virtual time down to subcycle clearing times. Though these quantities may be useful for cases of moderate overloads involving a long clearing time, they cannot be applied to short-circuit conditions (subcycle blows).

The *prospective current* is defined as the r.m.s. value of the alternating current, or the value of the direct current that would flow in a circuit on the occurrence of a short circuit immediately after the fuse (the fuse

being replaced by a link of negligible impedance), under given voltage conditions and supply network conditions (see Fig. 7-19).[16]

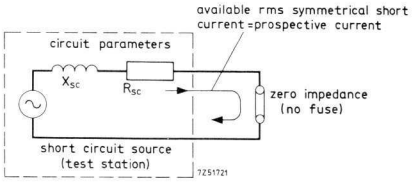


Fig. 7-19 Prospective current.

The *virtual melting time* is the time for which a constant current equal to the prospective current would have to flow in a fuse to produce the same quantity of energy as would be produced if the actual current during the melting time flowed in the fuse for the actual period.[17]

This implies a square current pulse for a subcycle blow, with an amplitude equal to the prospective current level. Since the potential fault current is sinusoidal, the actual melting time may greatly exceed the virtual melting time. The same applies to the real and virtual clearing times. This is illustrated in Fig. 7-20.

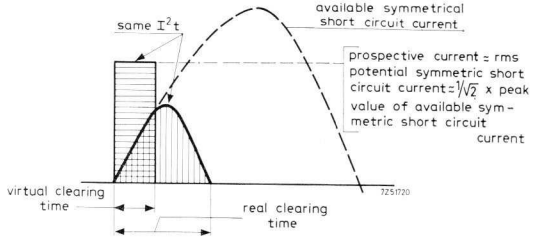


Fig. 7-20 Relationship between real and virtual clearing times.

For long-time blows the prospective current equals the peak value of the symmetric overload current divided by the square root of 2. Thus, the prospective current may be assumed to be alternating, without affecting the definition of the virtual time. In fact, when overload current circulates for many cycles, virtual times and actual times will become equal.

The definition of prospective current and virtual times simplify fuse testing procedures. The difficulty is that for high current levels the potential fault current cannot be determined from an oscillogram because the

fuse will have cut the current before the maximum potential fault current level occurs. However, the virtual times, i.e. the ratio of the corresponding I^2t-values to the square of the prospective current, can be easily determined.

The assumption of zero output impedance in the definition of prospective current (cf. Fig. 7-19) eliminates the effect of variation in fuse impedance between different specimens. For a long-time blow the clearing time and melting time curves will eventually meet. If a fuse clears only after a matter of seconds, addition of one quarter or one half cycle of arcing will have negligible effect on the overall time required for the fuse to clear.

7.6.4 Fusing Sequence

Branch fuse selectivity

Extra diodes built into parallel branches permit continuity of operation should a diode become defective. A branch fuse should then be incorporated in each diode circuit, so that only the faulty diode is isolated (branch fuse selectivity).

The requirements for selectivity imposed upon branch fuses may be derived as follows. When a diode becomes defective (Fig. 7-21), the fault current I_{Lsc} is carried by all good diodes in the opposite leg. It is assumed that due to unequal current distribution, the lower branch is the upper leg takes the major share I_{sc}. This should not affect its associated fuse. Note that with a redundancy of diodes in the system, branch fuses are not intended for diode protection but serve only to disconnect faulty diodes so as to provide continuity of operation for the system as a whole.

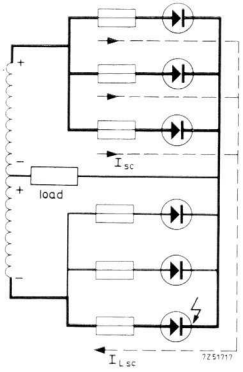


Fig. 7-21 Branch fusing to isolate faulty diode.

The fuse link in series with the forward biased diode carrying the highest current must not start to melt before the end of the short circuit, thus:

$$I_{sc}{}^2 t_{cl} < (i^2t)_m, \tag{7-28}$$

where t_{cl} = actual clearing time of the branch fuse in series with the shorted diode,
$(i^2t)_m$ = rated I^2t-value of each branch fuse.

Due to unequal current distribution, a derating factor f_d must be used (see Section 8.3.3). Thus, for n paralleled diodes, the maximum current share I_{sc} is given by:

$$I_{sc} = I_{Lsc}/nf_d. \tag{7-29}$$

Substitution of eq. (7-29) in condition (7-28) gives:

$$I_{Lsc}{}^2 t_{cl}/n^2 f_d{}^2 < (i^2t)_m.$$

For the fuse in the defective branch to blow, the I^2t-value in this branch must equal the rated fuse $(i^2t)_{cl}$-value:

$$I_{Lsc}{}^2 t_{cl} = (i^2t)_{cl},$$

and

$$(i^2t)_{cl}/(i^2t)_m < n^2 f_d{}^2.$$

Introducing the branch fuse constant:

$$C_f = (i^2t)_{cl}/(i^2t)_m, \tag{7-30}$$

we find the requirement for selectivity:

$$C_f < n^2 f_d{}^2. \tag{7-31}$$

By substituting 0.9 for f_d we arrive at Table 7-3.

Table 7-3. Branch selectivity values.

$n =$	2	3	4	5	6	7
$C_f <$	3.24	7.29	13.0	20.3	29.2	39.7

For a fuse of proper design, and of adequate voltage rating, the branch fuse constant C_f will be about 3, but values exceeding 10 are quite common, requiring at least 3 or 4 paralleled diode branches per leg, depending

on the actual value of C_f. If fewer branches are used, fuses in series with forward-biased diodes may blow when a reverse biased diode shorts, causing shutdown of the entire installation.

Line versus branch fuse selectivity

The line fuse is intended to protect the diodes against external shorts by shutting down the entire installation. Where diode redundancy has been built into the system, branch fuses, operate to disconnect only the faulty diode and ensure continuity of operation. There are two cases to be dis-distinguished:

— external short, at which only the line fuse should blow;
— shorted diode, at which only the branch fuse in series with the defective diode should blow.

At an *external short*, the branch fuse taking the major share I_{sc} of the fault current I_{Lsc}, should not start to melt before the line fuse clears (Fig. 7-22), which leads again to condition (7-28). Substituting eqs (7-29) and (7-30) in condition (7-28) gives for the branch fuse:

$$I_{Lsc}{}^2 t_{cl}/n^2 f_a{}^2 < (i^2t)_{cl}/C_f.$$

When the line fuse clears we have:

$$I_{Lsc}{}^2 t_{cl} = (I^2t)_{cl},$$

where $(I^2t)_{cl}$ is the line fuse clearing I^2t-rating. Introducing for the ratio of the line fuse rating to the branch fuse rating:

$$A = (I^2t)_{cl}/(i^2t)_{cl}, \tag{7-23}$$

we obtain for the selectivity against an external short:

$$A < n^2 f_a{}^2/C_f. \tag{7-33}$$

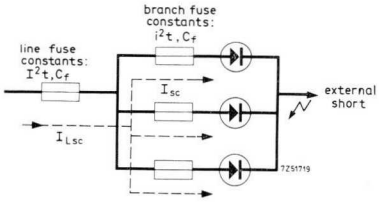


Fig. 7-22 External short blows only the line fuse.

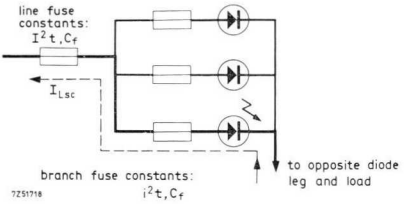


Fig. 7-23 Shorted diode blows only its branch fuse.

This formula states theoretically that when the line fuse current rating has been selected too high, all branch fuses will blow rather than the line fuse on the occurrence of an external short.

At a *shorted diode*, the line fuse link should not start to melt before the branch fuse in series with the shorted diode clears (Fig. 7-23), which leads to the condition:

$$I_{Lsc}{}^2 t_{cl} < (I^2t)_m,$$

where $(I^2t)_m$ is the line fuse melting I^2t-rating. When the branch fuse clears, we have:

$$I_{Lsc}{}^2 t_{cl} = (i^2t)_{cl},$$

whence:

$$(I^2t)_m > (i^2t)_{cl}. \tag{7-34}$$

Introducing the line fuse constant

$$C_F = (I^2t)_{cl}/(I^2t)_m, \tag{7-35}$$

and using eq. (7-32) and condition (7-34), the following condition can be derived for the selectivity against the shorted diode:

$$A > C_F. \tag{7-36}$$

This condition states theoretically that when the line fuse rating has been chosen too low, the line fuse will clear rather than the branch fuse if a diode shorts, thus shutting down the entire installation.

Conditions (7-33) and (73-6) have been elaborated in Table 7-4 for $f_d = 0.9$ and two values of the fuse constants C_F and C_f.

Table 7-4. Line versus branch fuse selectivity values, for $f_d = 0.9$.

n	$C_F = C_f$	ratio A		permissible A-range
		external short	shorted diode	
4	4	< 3.24	> 4	—
5	4	< 5.06	> 4	4 to 5.06
6	4	< 7.29	> 4	4 to 7.29
11	10	< 9.80	> 10	—
12	10	< 11.7	> 10	10 to 11.7
13	10	< 13.7	> 10	10 to 13.7

Comparing Tables 7-3 and 7-4 we may conclude that for 3 diode branches in parallel a fuse with $C_f = 4$ is adequate for branch fuse selectivity.

However, the line versus branch fuse selectivity requires at least 5 parallel diode branches for such types of fuse. Thus, the line versus branch fuse selectivity imposes more severe requirements on the system design than the branch fuse selectivity. For fuses with constants equal to 10, not less than 12 parallel branches would be needed to achieve selectivity. The ultimate circuit design will depend on the ratings of available fuses. Where the required selectivity cannot be obtained in a given circuit design, the number of paralleled diodes branches must be increased *without* altering the ratings of the line and branch fuses. Tables 7-3 and 7-4 may be helpful in the design of practical circuits.

7.6.5 Fuse Requirements

To ensure good coordination between diodes and fuses, a fuse intended to protect diodes should satisfy several requirements.

The fuse should have a *current rating* equal to the r.m.s. value of the rated current passed by the circuit the fuse is intended to protect; where necessary, the next higher current rating may be selected. In six-phase circuitry, some fuse derating may be necessary to obviate aging of the fuse link due to the high value of the current peak factor. A high current peak factor will cause considerable temperature fluctuations in the fusible element, and may lead to permanent alteration of the fuse link properties. This can initiate a long-time blow even though the current rating of the fuse has not been exceeded.

The fuse should have a *voltage rating* at least equal to the voltage supplied to the circuit the fuse is intended to protect. Fuses of a voltage rating just exceeding the circuit supply voltage will exhibit slow circuit-breaking action. The accompanying excessive amount of energy passed to the circuit under protection involves the risk of diodes being damaged. Therefore, preference may be given to high-voltage fuses; their rapid arc quenching results in a lesser amount of energy being dissipated at a short in the circuit under protection.

During current inversion, the *fuse arcing voltages* produce transients across the diodes. These transients should not exceed either the non-repetitive peak reverse voltage rating of conventional diodes, or the minimum breakdown voltage level of controlled avalanche diodes.

When interrupting a fault current, a branch fuse will produce a voltage transient across good diodes in other branches. This may require the use of diodes having a higher voltage rating than required by the application, especially when high-voltage fuses are used. Where n diodes are connected

in series in each branch, and an adequate voltage-sharing network is incorporated, the non-repetitive voltage rating of each diode should be at least $1/n$ times the fuse arcing voltage. Where individual line fuses are used for protection of rectifier systems supplied from a common input transformer, a similar situation will exist and the same condition will apply. Where line fuses are used to protect a rectifier system with no other installations working from the input transformer, the fuse arcing voltage will be hardly perceptible as a transient across the diodes. Therefore, compared to branch fuses, line fuses may be rated for higher voltages without the necessity of correspondingly increasing the non-repetitive voltage rating of the diodes.

The *fuse response* should be rapid, with a clearing time of less than one half power cycle. It should be kept in mind that the actual melting time may greatly exceed the virtual melting time for subcycle blows.

Under no circumstances should the *fuse* $(I^2t)_{cl}$*-rating* exceed — during the relevant clearing time — the total I^2t-rating of the (paralleled) diodes the fuse is intended to protect.

The *current-breaking capacity* of the fuses should be adequate with respect to the maximum prospective current.

If the diode-fuse coordination is critical, manufacturing tolerances should be considered; that is, the maximum value of $(I^2t)_{cl}$ must be taken into consideration. Since the line fuse has a higher current rating than the branch fuse, this requirement applies in particular to the former.

7.6.6 Diode-Fuse Coordination

For adequate diode-fuse coordination the following remarks may be of use.

The fuse voltage rating V_{nom} can be found from Table 7-5, in which V_o denotes the rectifier output voltage. It should be kept in mind that the fuse must be capable of interrupting the voltage between phases for the three-phase bridge and the half-wave rectifier configurations, and twice the voltage per phase for a six-phase half-wave circuit.

Table 7-5. Ratio of the nominal fuse voltage rating V_{nom} to the rectifier output voltage V_o

rectifier configuration	V_{nom}/V_o
single phase bridge circuit	1.11
three-phase bridge circuit	0.74
three-phase half-wave circuit	1.48
six-phase half-wave circuit	1.48

Table 7-5 applies both to single rectifier systems and to systems in which paralleled rectifiers are used.

In most installations either line fuses are employed or a single fuse is inserted in each leg (e.g. bridge rectifier systems) which may consist of a single diode or of paralleled diodes. For these circuits, the fuse r.m.s. current rating I_{nom} follows from Table 7-6, in which I_o is the rectifier output current.

Table 7-6. Ratio of the nominal fuse current rating I_{nom} to the rectifier output current I_o

rectifier configuration	I_{nom}/I_o			
	line fuse		branch fuse	
	resistive load	inductive load	resistive load	inductive load
single-phase bridge	1.1	1.0	0.79	0.71
three-phase bridge	0.82	0.82	0.58	0.58
three-phase half-wave	0.59	0.58	0.59	0.58
six-phase half-wave	0.41	0.41	0.41	0.41

For a parallel bank of n diodes, where each diode is individually protected by a fuse, the appropriate value given in the Table should be divided by n times the derating factor f_d to find the branch fuse r.m.s. current rating.

Table 7-6 can be used for determining line and branch fuses in single rectifier systems and the common line fuse for n_r identical systems working in parallel. The total output current should then taken to be $n_r f_d$ times the output current I_o of each rectifier system.

In single rectifier systems the potential r.m.s. symmetrical line fault current at the transformer secondary which is to be interrupted by the line or branch fuse follows from $I_{Lsc} = aI_o/x$, where a is given by Table 7-7 and x denotes the per unit transformer reactance.

Table 7-7. Factor a for deriving the potential r.m.s. symmetrical line fault current I_{Lsc}.

rectifier configuration	a	
	resistive load	inductive load
single-phase bridge	1.1	1.0
three-phase bridge	0.82	0.82
three-phase half-wave	0.59	0.58
six-phase half-wave	0.41	0.41

In paralleled rectifier systems the common input transformer is rated to deliver a d.c. output current $n_r f_d I_o$. The potential r.m.s. symmetrical line fault current I_{Lsc} to be interrupted by the line or branch fuse, whichever is used, is then given by $an_r f_d I_o/x$, where a also follows from Table 7-7, and n_r again denotes the number of identical paralleled systems.

It should be kept in mind that the use of a single common line fuse is inadequate for protection of individual diodes. Such a fuse must necessarily have a high r.m.s. current rating in order to carry the current of the whole installation. Additional fuses should therefore be employed for individual diode protection. The advantage of using a common line fuse is, however, that fewer fuses need be replaced in the case of an overload or external short.

Diodes require fast-acting fuses. Information on adequate diode-fuse coordination can be made available in the form of tables. It follows from these tables that even with the fast-acting current limiting fuses available, full protection of semiconductor power diodes may not be obtained if they are used at the maximum permissible forward current in rectifier circuits supplied from transformers having the usual 5% to 8% reactance. Where increase of source impedance by adding of chokes or by special transformer design is undesirable because of the resulting poor load regulation, current derating must be applied to prevent damage to diodes at severe shorts.

In many applications interruption of operation due to a very occasional short may be considered acceptable. It is then justifiable to use the diodes at their full current rating and install either branch fuses adequate for the rated r.m.s. diode current or incorporate properly rated line fuses. In a well-designed installation, severe shorts will hardly ever occur. Unless utmost reliability and continuity of operation is imperative, it will be cheaper to replace a few diodes while exchanging fuses during an emergency shutdown than to build a redundancy of diodes into the installation.

8 Series and Parallel Operation of Power Diodes

8.1 Series Operation

Power diodes must be connected in series and/or in parallel in cases where the output requirements of a rectifier installation exceed the ratings of single diodes. However, diodes of the same type always have slightly differing characteristics, so that unequal load sharing can occur.

If power diodes are connected in series, voltage-equalizing networks are required both for conditions of static reverse bias and for transients produced by recovery and stray capacitance effects. Such networks will be greatly simplified (or can even be dispensed with) if controlled avalanche diodes are used, because they ensure adequate voltage sharing under static conditions of reverse bias.

Additional measures, as discussed in Chapter 6, will generally be needed to reduce the effect of switching and load surges to an acceptable level.

In an unequalized chain of series-connected diodes, large differences in voltage across individual diodes will occur owing to the unavoidable spread in characteristics, as illustrated in Fig. 8-1. It will be seen that the equivalent impedances change continuously as the diode series switches from one state to another. When the chain is biased in the reverse direction immediately following forward conduction (state I), a situation of

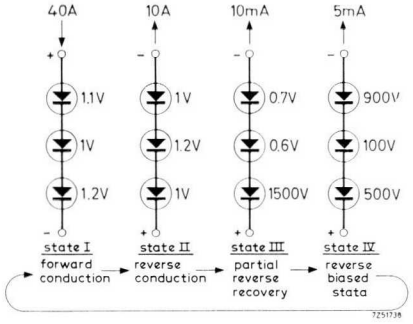


Fig. 8-1 Possible voltage distribution across an unequalised series chain of diodes.

reverse conduction (state II) will occur before reverse recovery starts to take place. Not all diodes will recover in the same time; the unequal

voltage distribution depends on the diode junction capacitance and recovery time. The diode with the smallest stored charge will build up its potential barrier first, thus absorbing the full amount of reverse voltage (state III). During the reverse-biased state (state IV), the differences in leakage resistance (see Fig. 8-2) will again cause poor voltage sharing. Due to the common leakage current, the diode with the highest leakage resistance takes the major portion of the applied reverse voltage.

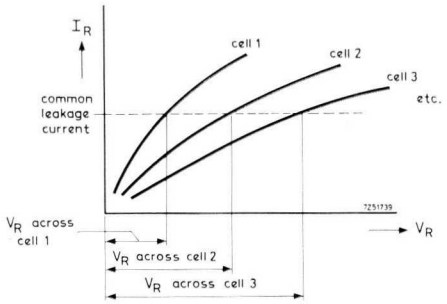


Fig. 8-2 Reverse characteristics illustrating reason for unequal voltage distribution across diodes in series.

The effect of unequal voltage distribution in the reverse-biased state (static condition) is eliminated by shunting across each diode a resistor of 1/3 to 1/10 times the anticipated minimum diode leakage resistance. A parallel capacitor of suitable value is added for each diode to handle dynamic conditions. By absorbing the excess stored charge of those diodes having the longest reverse recovery time, a voltage-sharing action takes place. The capacitors also give sufficient voltage equalization when the diodes switch to their conducting state, a smaller transient then being produced than at reverse recovery.

Controlled avalanche diodes operate as high-value voltage regulator (zener) diodes and thus achieve forced voltage sharing under static conditions without need for equalizing resistors.

8.1.1 Equalizing Networks for Conventional Diodes

Voltage equalization has the advantage of increasing the permissible reverse voltage for the diode chain. Equalizing resistors, shunted across the series-connected diodes, will help to distribute the voltage across the whole chain of n diodes under static conditions of reverse bias. The required value of these resistors can be determined as follows.

Assume all diodes to be shunted by voltage-sharing resistors, each having a nominal value R (Fig. 8-3). Let the tolerance of the resistor be denoted by b and suppose all diodes to have the maximum leakage current except one (D_1). This worst-case consideration may be taken one stage further by assuming that a resistor with the upper tolerance limit, thus with resistance $(1 + b)R$, is shunted across D_1, whereas all others (D_2 to D_n) are shunted by a resistance $(1 - b)R$.

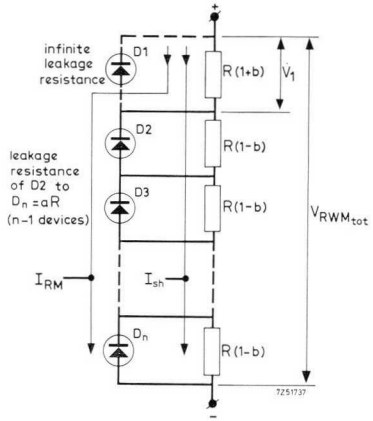


Fig. 8-3 Parallel resistors to equalize voltage distribution in reverse biased state.

For convenience we shall introduce a as the ratio of the minimum diode leakage resistance to the nominal value of the shunting resistor. The resistance R_p formed by the parallel connection of the minimum leakage resistance of any diode and its shunting resistor $(1 - b)R$ is thus given by:

$$R_p = \frac{a(1-b)R^2}{(1-b+a)R} = \frac{a(1-b)R}{1-b+a}. \tag{8-1}$$

Now the relation between the voltage V_1 across diode D_1 and the total crest working reverse voltage, $V_{RWM\ tot}$, imposed across the chain, can be expressed by:

$$\frac{V_1}{V_{RWM\ tot}} = \frac{(1+b)R}{(1+b)R + a(n-1)(1-b)R/(1-b+a)} = \frac{1+b}{1+b+a(n-1)(1-b)/(1-b+a)}. \tag{8-2}$$

The voltage across D_1 must not exceed the maximum crest working reverse voltage rating $V_{RWM\,max}$. Substituting $V_{RWM\,max}$ for V_1 and solving eq. (8-2) for n gives:

$$n \geqslant 1 + \frac{(1+b)(1-b+a)}{a(1-b)} \cdot \frac{V_{RWM\,tot} - V_{RWM\,max}}{V_{RWM\,max}}. \tag{8-3}$$

By neglecting the b^2 term, this condition reduces to:

$$n \geqslant 1 + \frac{1+a(1+b)}{a(1-b)} \cdot \frac{V_{RWM\,tot} - V_{RWM\,max}}{V_{RWM\,max}}. \tag{8-4}$$

Now, to find the value of R, we derive from Fig. 8-3:

$$V_1 = (b+1)R(I_{RM} + I_{sh}) \leqslant V_{RWM\,max}, \tag{8-5}$$

where I_{RM} = maximum anticipated leakage current at the crest working reverse voltage $V_{RWM\,max}$ at maximum junction temperature,

I_{sh} = current in shunt resistors.

According to Fig. 8-3:

$$\frac{I_{sh}}{I_{RM}} = \frac{aR}{(1-b)R} = \frac{a}{1-b}. \tag{8-6}$$

whence

$$I_{RM} + I_{sh} = \frac{1+a-b}{1-b} \cdot I_{RM}. \tag{8-7}$$

Substituting eq. (8-7) in condition (8-5) gives:

$$R \leqslant \frac{V_{RWM\,max}}{I_{RM}} \cdot \frac{1-b}{(1+a-b)(1+b)}, \tag{8-8}$$

or, to a good approximation, again neglecting b^2:

$$R \leqslant \frac{V_{RWM\,max}}{I_{RM}} \cdot \frac{1-b}{1+a(1+b)}. \tag{8-9}$$

The power rating of the shunt resistors can be found from:

$$P_R = V_{R\,rms}^2/R, \tag{8-10}$$

where $V_{R\,rms}$ denotes the r.m.s. value of the diode reverse voltage. This

voltage across the diodes and equalizing resistors is non-sinusoidal, and the following formulae will apply in calculating the required resistor power rating. For a two-phase half-wave rectifier and a single-phase bridge circuit we have:

$$P_R = 0.25\ V_{RWM}{}^2{}_{\max}/R, \tag{8-11}$$

and for three- and six-phase rectifier circuits:

$$P_R = 0.4\ V_{RWM}{}^2{}_{\max}/R. \tag{8-12}$$

When a reverse bias is applied to the chain, those diodes which have the shortest reverse recovery time (minimum charge stored in the centre layer) will block the reverse voltage first. In addition to absorbing the full reverse voltage, the recovered diodes will prolong the recovery time of the slower diodes because the flow of reverse current — which removes the excess stored charge — is impeded. To achieve voltage sharing under dynamic conditions, capacitors must therefore be shunted across each diode. The capacitors serve as low-impedance sources taking up the excess of stored charge, thus minimizing the reverse recovery time for all diodes and preventing build-up of an excessive voltage across the fastest ones.

The largest transient voltage will develop across the diode with the shortest recovery time (minimum stored charge $Q_{\min}$). The voltage V across this diode equals $(Q_{\max} - Q_{\min})/C_j$, where $Q_{\max}$ denotes the maximum stored charge and C_j the junction capacitance. This explains why increasing the effective capacitance by external means reduces the hole storage recovery transient voltage. With external capacitors added, the situation is as shown in Fig. 8-4. Since charge carriers of opposite

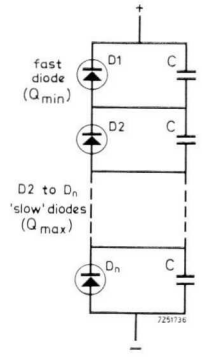


Fig. 8-4 Parallel capacitors to equalize voltage distribution during transition from forward conducting to reverse blocking state.

polarity will neutralize across all other capacitors, the reverse voltage across diode D_1 (having the minimum stored charge) is:

$$V = (Q_{max} - Q_{min})/C,$$

where C is the shunted capacitance, neglecting the junction capacitance. Because the permissible repetitive peak reverse voltage $V_{RRM\ max}$ must not be exceeded, C is given by:

$$C = (Q_{max} - Q_{min})/V_{RRM\ max}.$$

The situation is actually more complicated than outlined above because stray capacitances exist between the diode heat sinks and earth (Fig. 8-5). When a reverse voltage is applied, the stray capacitances C_{h1} to C_{hn} will not be charged at an equal rate; the charge rate decreases for capacitances nearer to the earthed end of the chain. A maximum overvoltage swing

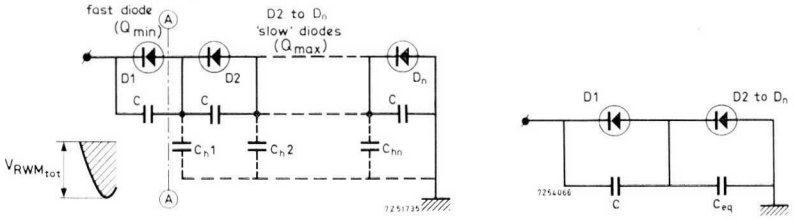


Fig. 8-5 Equivalent circuit of series chain of diodes mounted on a heat sink showing stray capacitances from heat sink to earth.

occurs across capacitor C in parallel with D_1, and thus the worst-case condition will exist when D_1 has the shortest recovery time. After D_1 has recovered, the recovery current flowing through the other diodes charges the capacitor across D_1 to a transient voltage:

$$V_{t1} = (Q_{max} - Q_{min})/C. \tag{8-14}$$

The remainder of the circuit-imposed crest working reverse voltage $V_{RWM\ tot}$ will be distributed across *all* diodes including D_1, thus generating a transient voltage across D_1 of

$$V_{t2} = \frac{C_{eq}}{C + C_{eq}}(V_{RWM\ tot} - V_{t1}) = \frac{C_{eq}}{C + C_{eq}}\left(V_{RWM\ tot} - \frac{Q_{max} - Q_{min}}{C}\right), \tag{8-15}$$

where C_{eq} denotes the equivalent total capacitance from cathode of D_1

to earth (Fig. 8-5b). The total reverse transient voltage V_t across D_1 is the sum of V_{t1} and V_{t2} and must not exceed $V_{RRM\ max}$, which may be expressed by:

$$V_t = \frac{Q_{max} - Q_{min}}{C} + \frac{C_{eq}}{C + C_{eq}} \left(V_{RWM\ tot} - \frac{Q_{max} - Q_{min}}{C} \right) \leqslant V_{RRM\ max}. \tag{8.16}$$

Introducing the capacitance ratio factor

$$d = C_{eq}/(C + C_{eq}), \tag{8-17}$$

condition (8-16) reduces to:

$$(1 - d)\,(Q_{max} - Q_{min})/C + dV_{RWM\ tot} \leqslant V_{RRM\ max}. \tag{8-18}$$

The stray capacitance C_h from heat sink to earth may be derived from Fig. 8-6. The graph of Fig. 8-7 represents the capacitance ratio factor d

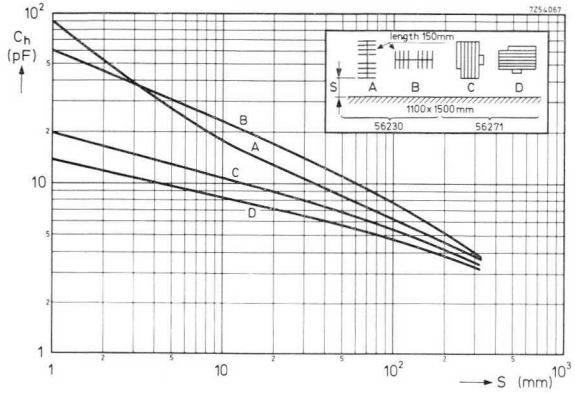
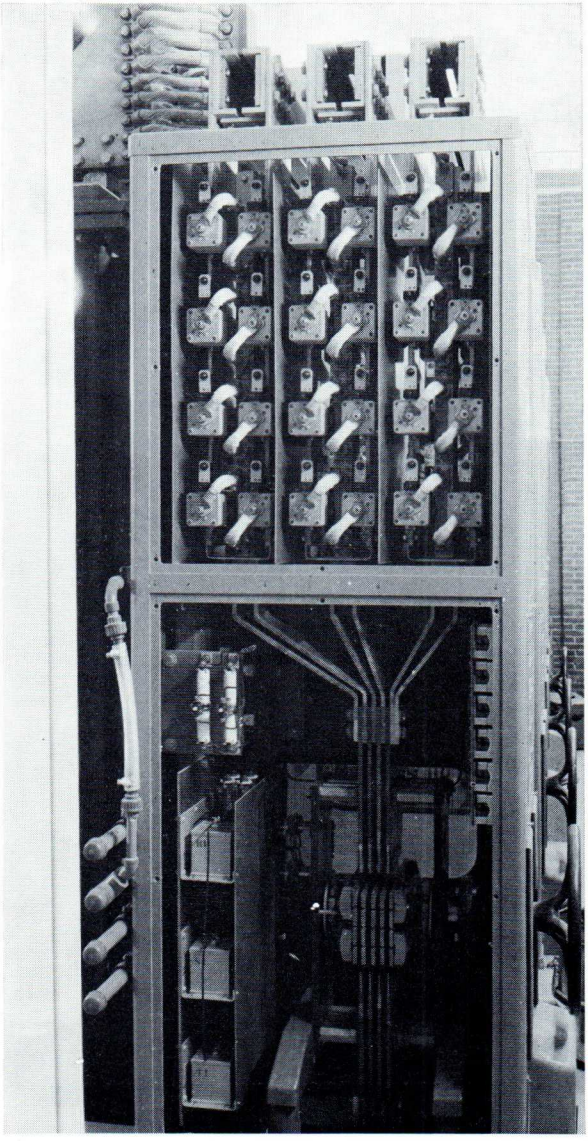


Fig. 8-6 Graph illustrating stray capacitance from heat sink to earth.

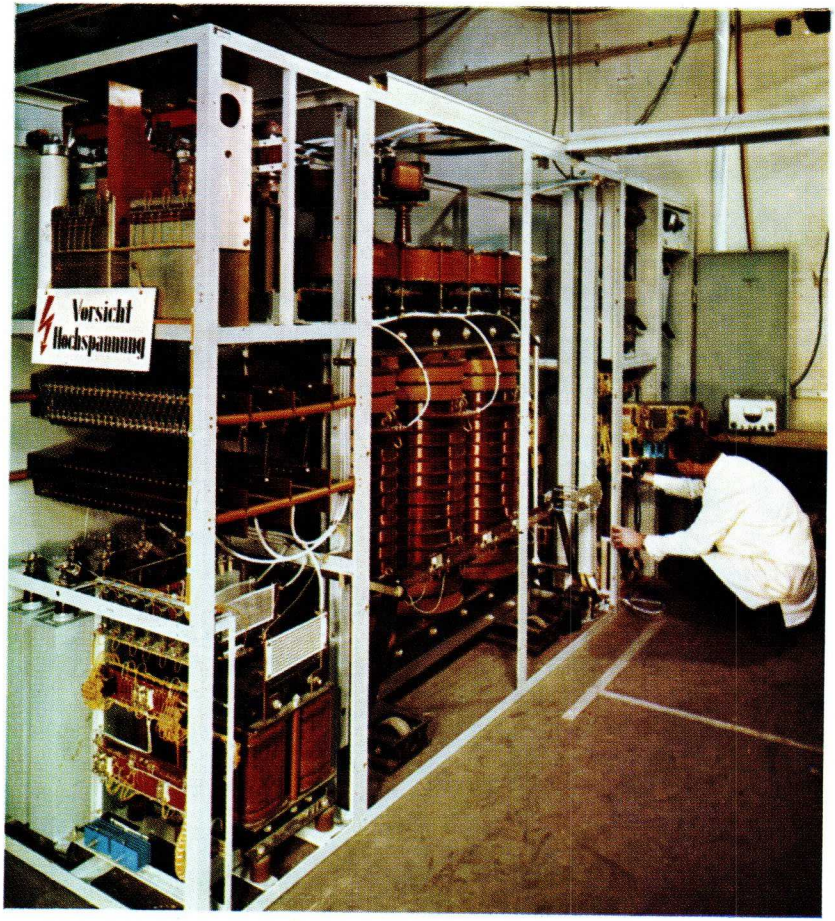
versus the number n of diodes in series, the parameter being the ratio of the shunted capacitance C to the stray capacitance C_h. Calculation of the required value of C can be simplified as follows. By putting $C_h = 0$ and $C_{eq} = C/(n - 1)$, eq. (8-17) reduces to (cf. Fig. 8-7 for $C/C_h = \infty$):

$$d = 1/n. \tag{8-19}$$

This equation will hold true to a good approximation for most practical cases because, generally, C_h is negligible with respect to C. Substituting eq. (8-19) in condition (8-18) gives:



Part of an 850 V, 120 kA water-cooled rectifier installation (by courtesy of the aluminium works "Aluminium Delfzijl N.V." - The Netherlands).



H.T. supply for a klystron television transmitter 40/8 kW. The rectifier arrangement shown in the middle of the frame in the foreground is equipped with avalanche diodes Types BYX25-1000, (by courtesy of SEL-Germany).

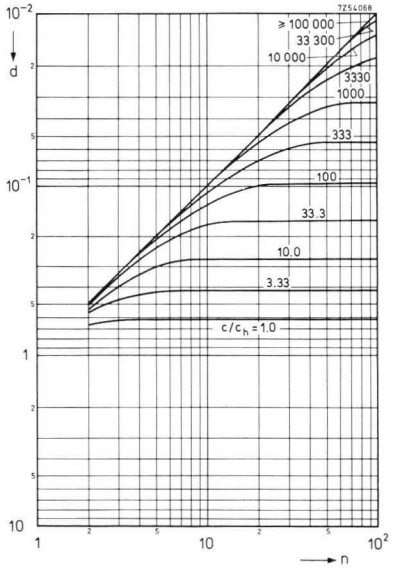


Fig. 8-7 Capacitance ratio factor (d) vs. number of diodes in series (n).

$$C \geqslant (n-1)\,(Q_{\max} - Q_{\min})/(nV_{RRM\ \max} - V_{RWM\ \mathrm{tot}}). \qquad (8\text{-}20)$$

If C_h is not negligible, the value of C as calculated from condition (8-20) must be verified against condition (8-18), d being derived from Fig. 8-7.

The stored charge limits for various series of diodes can be found in Table 8-1.

Table 8-1 (Spread in reverse recovery charge Q of our rectifier diodes)

type	$I_{F_{av}}$ (A)	$Q_{\min}$ (μC)	$Q_{\max}$ (μC)
BYX 13-series	20	12	40
BYX 14-series	150	60	250
BYX 23-series *	100	30	120
BYX 27-series *	250	75	300
BYX 32-series	100	30	120
BYX 33-series	250	75	300
BYY 22-series	10	8	28
BYZ 10-series	6	0.1	5
BYZ 14-series	40	17	70

* controlled avalanche types

The maximum permissible transient voltage may be readily determined as follows. A transient voltage V_t superimposed on the crest working reverse voltage applied to the circuit will distribute equally across the capacitive network (cf. Fig. 8-5), resulting in a voltage per diode of dV_t, where d is the capacitance ratio factor. This value must not exceed the difference in repetitive peak and working voltage rating, so the maximum permissible transient on the crest working reverse voltage is:

$$V_{t\,\max} = (V_{RRM\,\max} - V_{RWM\,\max})/d. \tag{8-21}$$

Example

A chain of diodes in a three-phase rectifier system is to carry 100 A and must withstand a reverse voltage of 5.45 kV at the nominal line voltage. The current decay rate during commutation, di/dt, is 0.005 A/μs per ampere. The line voltage fluctuations are taken to be ± 10%. The spacing between the horizontally heat sinks and the chassis is 90 mm. Design a voltage sharing network in the case of diodes BYY77 or BYY78 from the BYX32-series being used.

From the data sheet it is seen that $V_{RWM\,\max} = 1200$ V and $V_{RRM\,\max} = 1600$ V. At $V_{RWM\,\max} = 1200$ V and $T_{j\,\max} = 190$ °C, $I_{RM} = 7$ mA. At an overvoltage of 10%:

$$V_{RWM\,\mathrm{tot}} = 1.1 \times 5.45 = 6 \text{ kV}.$$

Assume the resistance ratio factor a to be 5 and resistors with a tolerance b of 0.05 to be used. Thus, from condition (8-4):

$$n \geqslant 1 + \frac{1 + 5(1 + 0.05)}{5(1 - 0.05)} \cdot \frac{6000 - 1200}{1200} = 6.27,$$

which means that seven diodes must be connected in series. The actual value of a is found by substituting $n = 7$ in condition (8-4), which yields $a = 2.7$.

From condition (8-9):

$$R \leqslant \frac{1200}{0.0077} \cdot \frac{1 - 0.05}{1 + 2.7(1 + 0.05)} = 42300.$$

It is thus safe to choose 39 kΩ resistors. Their power rating is, from eq. (8-12):

$$P_R = 0.4 \times 1200^2/39000 \approx 15 \text{ W}.$$

Now the capacitance value must be found. For diodes BYY77/78, at $I_{FAV} = 100$ A, we find from Table 8-1 (for the BYX32-series) $Q_{\max} - Q_{\min} = 120 - 30 = 90$ μC, whence from condition (8-20):

$$C \geqslant (7 - 1)90 \cdot 10^{-6}/(7 \times 1600 - 6000) = 0.104 \text{ μF}.$$

Capacitors of 120 nF may therefore be used.

For a horizontally mounted heat sink of the extrusion type 56230 of 150 mm length, mounted at 90 mm from the chassis, the capacitance C_h is, from Fig. 8-6, 8 pF. Hence

$$C/C_h = 120 \times 10^{-9}/8 \times 10^{-12} = 15 \times 10^3$$

corresponding according to Fig. 8-7 to $d = 0.142$. Substituting these values in condition (8-18) gives:

$$V_{RRM\ max} \geqslant (1 - 0.142)90 \times 10^{-6}/120 \times 10^{-9} + 0.142 \times 6000 = 1495\ \text{V}.$$

Since $V_{RRM\ max} = 1600$, this condition is satisfied.

The maximum permissible transient voltage superimposed on the crest working reverse voltage is, from eq. (8-21):

$$V_{t\ max} = (1600 - 1200)/0.142 = 2820\ \text{V}.$$

8.1.2 Equalizing Networks for Controlled Avalanche Diodes

Controlled avalanche diodes require no parallel resistors for static voltage sharing because under static conditions the inherent properties will force equal voltage distribution across all diodes connected in series. The reverse recovery current of the slower diodes will continue to flow through the faster diodes operating in their avalanching region until all diodes have to act as low-impedance source for the diode with the longer recovery time. However, capacitive elements will still be required in cases where the repetitive reverse power ratings may be exceeded during reverse recovery. The required capacitance is determined in the following way.

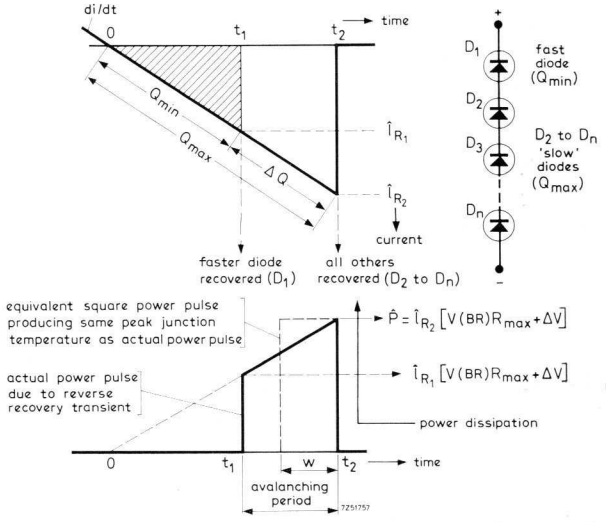


Fig. 8-8 Reverse recovery phenomenon occurring in series chain.

Fig. 8-8 shows idealized waveforms for the diode reverse recovery

phenomenon occurring in a series chain. To simplify the analysis, a triangular waveform of the reverse recovery current i_R is assumed with ideal cut-off effect at the end of the recovery cycle. Diode D_1 is assumed to have a minimum stored charge $Q_{\min}$ when the anode current passes zero, while all other diodes are assumed to have maximum stored charge $Q_{\max}$. Diode D_1 will have recovered at time t_1, and the surplus charge $Q_{\max} - Q_{\min}$ must be absorbed by D_1 during its avalanching period from t_1 to t_2, at which time *all* diodes have recovered. Maximum dissipation will occur in D_1 at the maximum anticipated breakdown voltage $V_{(BR)R\,\max}$. Since the breakdown voltage rises with temperature, this dissipation should be calculated for the maximum permissible junction temperature. Moreover, the additional voltage drop ΔV due to the dynamic resistance in the avalanching region must be taken into account. The maximum energy dissipated in D_1 is therefore:

$$P = \int_{t_1}^{t_2} i_R \{V_{(BR)R\,\max} + \Delta V\}\, \mathrm{d}t. \tag{8-22}$$

Since the integral of $i_R\, \mathrm{d}t$ represents the surplus stored charge $Q_{\max} - Q_{\min}$, we may write:

$$P = \{V_{(BR)R\,\max} + \Delta V\}\,(Q_{\max} - Q_{\min}). \tag{8-23}$$

The current decay rate is (see Fig. 8-8):

$$\mathrm{d}i/\mathrm{d}t = \hat{\imath}_{R1}/t_1 = \hat{\imath}_{R2}/t_2, \tag{8-24}$$

where $\hat{\imath}_{R2}$ denotes the peak recovery current through diodes D_2 to D_n and $\hat{\imath}_{R1}$ that through the fastest diode D_1. By using eq. (8-24), we find for the stored charge:

$$Q_{\min} = \hat{\imath}_{R1} t_1/2 = t_1^2(\mathrm{d}i/\mathrm{d}t)/2, \tag{8-25}$$

and

$$Q_{\max} = \hat{\imath}_{R2} t_2/2 = t_2^2(\mathrm{d}i/\mathrm{d}t)/2. \tag{8-26}$$

Solving t_1 and t_2 from eqs (8-25) and (8-26) gives:

$$t_1 = \{2Q_{\min}/(\mathrm{d}i/\mathrm{d}t)\}^{\frac{1}{2}}$$

and (8-27)

$$t_2 = \{2Q_{\max}/(\mathrm{d}i/\mathrm{d}t)\}^{\frac{1}{2}}.$$

The peak value $\hat{P}$ of the power pulse occurring in D_1 owing to reverse recovery transients is:

$$\hat{P} = \hat{\imath}_{R2}\{V_{(BR)R\,\max} + \Delta V\}, \tag{8-28}$$

where $\hat{\imath}_{R2}$ follows from eqs (8-24) and (8-26):

$$\hat{\imath}_{R2} = (2Q_{\max} \cdot \mathrm{d}i/\mathrm{d}t)^{\frac{1}{2}}. \tag{8-29}$$

The actual power pulse will now be replaced by a square pulse of same amplitude $\hat{P}$ and width w (Fig. 8-8). To produce the same peak junction temperature as in the actual case, the pulse width must be:

$$w = \{2/(\mathrm{d}i/\mathrm{d}t)\}^{\frac{1}{2}} \cdot \frac{4{Q_{\max}}^{3/2} - 3{Q_{\max}}^{1/2}Q_{\min} - {Q_{\min}}^{3/2}}{9Q_{\max}}. \tag{8-30}$$

Rearranging this expression, we obtain the following general formula (see Fig. 8-9):

$$\{w(\mathrm{d}i/\mathrm{d}t)/(Q_{\max}\}^{1/2} = \sqrt{(2/9)}\,\{4 - 3Q_{\min}/Q_{\max} - (Q_{\min}/Q_{\max})^{3/2}\}. \tag{8-31}$$

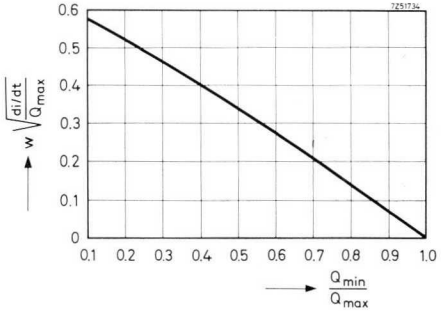


Fig. 8-9 Plot of $w\sqrt{(d_i/d_t)}/Q_{max}$ *against* Q_{min}/Q_{max}.

If the reverse transient is large (high value of the current decay rate $\mathrm{d}i/\mathrm{d}t$), the diode can store only part of the surplus charge $Q_{\max} - Q_{\min}$. This means that if the diode, according to its ratings, is capable of storing $Q_{\max} - Q_{\text{rated}}$, a capacitance C may be required to absorb the remaining charge $Q_{\text{rated}} - Q_{\min}$ (see Fig. 8-10). This capacitance is given by:

$$C = (Q_{\text{rated}} - Q_{\min})/\{V_{(BR)R\ \max} + \Delta V\}. \tag{8-32}$$

External transients will be shared evenly by all diodes connected in series. However, a capacitor of larger value than given by C in eq. (8-22) will be needed to store the additional amount of energy generated by such transients. For calculating the capacitance required in the case of external transients the reader is referred to Chapter 6.

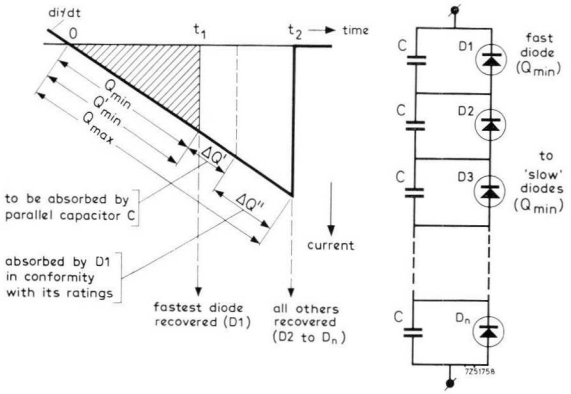


Fig. 8-10 Action of parallel capacitor.

Example

A chain of diodes has to carry 80 A and withstand a reverse voltage of 2.5 kV. The current decay rate $di/dt = 0.13$ A/μs. Design the voltage sharing network for BYX23-1000 controlled avalanche diodes (requiring no voltage equalizing resistors).

The following data apply: $I_{FAV} = 100$ A; $V_{RWM\ max} = 1000$ V; $V_{(BR)R} = 1250$ to 1600 V at $T_j = 25$ °C.

At $di/dt = 0.13$ A/μs ($< 0.005 I_{FAV}$), $Q_{min} = 10$ μC and $Q_{max} = 45$ μC.

Since

$$n = V_{RWM\ tot}/V_{RWM\ max} = 2500/1000 = 2.5,$$

three diodes will have to be connected in series. According to the data sheet the maximum reverse breakdown voltage is 1600 V at $T_j = 25$ °C and $i_R = 10$ mA. As seen from the reverse characteristic of the diode, an increase of the junction temperature to 190 °C will shift this characteristic upward over 250 V, thus at $T_j = 190$ °C.:

$$V_{(BR)R\ max} = 1600 + 250 = 1850 \text{ V}.$$

From eq. (8-29):

$$\hat{\imath}_{R2} = (2Q_{max} \cdot di/dt)^{1/2} = (2 \times 45 \times 0.13)^{1/2} = 3.42 \text{ A}.$$

From the reverse characteristic for the diode at $T_j = 190$ °C we find $\Delta V = 140$ V for $\hat{\imath}_{R2} = 3.42$ A, whence from eq. (8-28):

$$P = \hat{\imath}_{R2}\{V_{(BR)R\ max} + \Delta V\} = 3.42(1850 + 140) \text{ watts} = 6.8 \text{ kW}.$$

For $Q_{min}/Q_{max} = 10/45 = 0.22$ we find from Fig. 8-9:

$$w\{(di/dt)/Q_{max}\}^{1/2} = 0.515,$$

which gives:

$$w = 0.515\{Q_{max}/(di/dt)\}^{1/2} = 0.515(45/0.13)^{1/2} = 9.6 \text{ μs}.$$

From the repetitive peak reverse power curve for $T_j = 190$ °C it can be seen that during 9.6 μs a reverse power pulse of 8.1 kW can be carried. No parallel capacitor is therefore required.

The following example deals with a case where a parallel capacitor cannot be dispensed with.

Example

The chain of diodes is to carry 100 A and withstand a reverse voltage of 2.5 kV. The current decay rate $di/dt = 0.35$ A/μs. Design the voltage sharing network for three BYX23-1000 controlled avalanche diodes connected in series ($I_{FAV} = 100$ A; $V_{RWM\,max} = 1000$ V; $V_{(BR)R} = 1250$ to 1600 V at $T_j = 25$ °C).

At $di/dt = 0.35$ A/μs ($< 0.005 I_{FAV}$) it follows that $Q_{min} = 23$ μC and $Q_{max} = 90$ μC. The data sheet shows that at $T_j = 190$ °C, $V_{(BR)R\,max} = 1850$ V, as in the preceding example.

From eq. (8-29):

$$\hat{\imath}_{R2} = (2Q_{max} \cdot di/dt)^{1/2} = (2 \times 90 \times 0.35)^{1/2} = 7.95 \text{ A}.$$

From the reverse characteristic for $\hat{\imath}_{R2} = 7.95$ A at $T_j = 190$ °C, we find $\Delta V = 270$ V, whence, from eq. (8-28):

$$\hat{P} = \hat{\imath}_{R2}\{V_{(BR)R\,max} + \Delta V\} = 0.795(1850 + 270) \text{ watts} = 16.9 \text{ kW}.$$

For $Q_{min}/Q_{max} = 23/90 = 0.255$ we find from Fig. 8-9:

$$w\{(di/dt)/Q_{max}\}^{1/2} = 0.495,$$

whence

$$w = 0.495\ \{Q_{max}/(di/dt)\}^{1/2} = 0.495(90/0.35)^{1/2} = 8.0\ \mu\text{s}.$$

According to the repetitive peak reverse power curve for $T_j = 190$ °C, a pulse of up to 8.6 kW peak reverse power is permissible during 8.0 μs, so that a parallel capacitor must be used.

At $\hat{P} = 16.9$ kW and $T_j = 190$ °C the permissible pulse width $w_{rated} = 1.25$ μs, whence:

$$w_{rated}\{(di/dt)/Q_{max}\}^{1/2} = 1.25(0.35/90)^{1/2} = 0.078.$$

From Fig. 8-9 we find for this value $Q_{rated}/Q_{max} = 0.89$, whence

$$Q_{rated} = 0.89 Q_{max} = 0.89 \times 90 = 80.1\ \mu\text{C}.$$

The capacitor must absorb:

$$Q_{rated} - Q_{min} = 80.1 - 23 = 57.1\ \mu\text{C},$$

whence, from eq. (8-32):

$$C = (Q_{rated} - Q_{max})/\{V_{(BR)R\,max} + \Delta V\} = 57.1/(1850 + 270) = 26.9 \text{ nF},$$

which suggests that a 27 nF capacitor would suffice. However, it must still be checked whether, with this capacitance, the repetitive peak reverse power rating is not exceeded at the *minimum* reverse breakdown voltage. From the data sheet it is seen that $V_{(BR)R\,min} = 1250$ V at $T_j = 25$ °C. Increase of the junction temperature to 190 °C will shift the reverse characteristic upward over 250 V, thus, at $T_j = 190$ °C.:

$$V_{(BR)R\,min} = 1250 + 250 = 1500 \text{ V}.$$

Again, for $\Delta V = 270$ V, and in analogy with eq. (8-28):

$$P = \hat{\imath}_{R2}\{V_{(BR)R\,min} + \Delta V\} = 7.95(1500 + 270) = 14.1 \text{ kW}.$$

The charge absorbed by the capacitor at $V_{(BR)R\,\min}$ is:

$$Q_{\text{rated}} - Q_{\min} = C\{V_{(BR)R\,\min} + \Delta V\} = 0.027(1500 + 270) = 47.8\ \mu\text{C}.$$

Hence

$$Q_{\text{rated}} = 23 + 47.8 = 70.8\ \mu\text{C},$$

which gives

$$Q_{\text{rated}}/Q_{\max} = 70.8/90 = 0.786.$$

For this value we find from Fig. 8-9:

$$w_{\text{rated}}\{(\text{d}i/\text{d}t)/Q_{\max}\}^{1/2} = 0.15\ \mu\text{s},$$

whence

$$w_{\text{rated}} = 0.15\{Q_{\max}/(\text{d}i/\text{d}t)\}^{1/2} = 0.15(90/0.35)^{1/2} = 2.4\ \mu\text{s}.$$

From the repetitive peak reverse power curve it is seen that the diodes can carry only 13.2 kW peak reverse power during 2.4 μs at $T_j = 190\ ^\circ\text{C}$, which is too low. A slightly larger capacitor will therefore have to be used. Putting $C = 33$ nF and repeating the calculation for the minimum reverse breakdown voltage shows that this capacitance is adequate for absorbing the reverse power pulse.

The need for a parallel capacitor may be circumvented by using controlled avalanche diodes of a lower voltage classification, the peak reverse dissipation then being smaller. This is illustrated by the following example.

Example

Choosing BYX-400 controlled avalanche diodes, seven of them must be connected in series to withstand 2.5 kV reverse voltage. Current decay rate $\text{d}i/\text{d}t = 0.35$ A/μs. For these diodes $V_{(BR)R} = 500$ to 800 V at $T_j = 25\ ^\circ\text{C}$. From the data sheet it is seen that $V_{(BR)R\,\max} = 800$ V at $T_j = 25\ ^\circ\text{C}$. An increase of T_j to 190 °C shifts the reverse characteristic upward over 110 V, whence at $T_j = 190\ ^\circ\text{C}$:

$$V_{(BR)R\,\max} = 800 + 110 = 910\ \text{V}.$$

As in the preceding example, $\hat{\imath}_{R2} = 7.95$ A. From the reverse characteristic for $T_j = 190\ ^\circ\text{C}$ and $\hat{\imath}_{R2} = 7.95$ A it is seen that $\Delta V = 90$ V. Hence, from eq. (8-28):

$$P = \hat{\imath}_{R2}\{V_{(BR)R\,\max} + \Delta V\} = 7.95(910 + 90) = 7.95\ \text{kW}.$$

As in the preceding example, $w = 8.0$ μs. From the repetitive peak reverse power curve (for $T_j = 190\ ^\circ\text{C}$) it can be seen that a peak reverse power pulse of 8.6 kW can be carried during 8.0 μs. No capacitor will therefore be needed in this case.

8.2 Parallel Operation

When power diodes are connected in parallel, proper current distribution should be ensured. The use of controlled avalanche diodes does not ensure this; it merely shares the energy dissipated to a limited extent during reverse transients. To help equalize the current, several techniques are

available, including selection of matched diodes, current and temperature derating, and forced current sharing.

When several diodes are connected in parallel, the total current rating of the parallel bank is by no means equal to the sum of the individual current ratings, because of the unavoidable spread in forward characteristics. As all paralleled diodes are subject to the same instantaneous forward voltage, the diode with the lowes forward resistance will take the greatest current share. Histograms, illustrating the spread in forward characteristics of the BYZ14 are shown in Fig. 8-11 for two values of forward current. True enough, by using matched diodes, equal current sharing is possible. However, matching of diodes poses problems both to the manu-

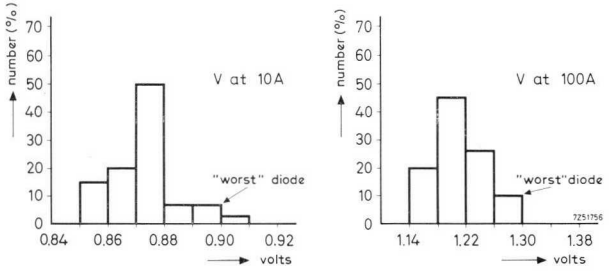


Fig. 8-11 Histogram showing spread in forward characteristics of BYZ14 diodes.

facturer and to the user. For the latter it may be difficult to replace diodes in a bank consisting of many matched paralleled diodes. Matching should be carried out for forward voltage at two distinct current levels to achieve reliable current sharing under both normal and fault conditions. Because matching would be impaired if voltage unbalance were present, care must be exercised to equalize resistances and inductances of the parallel paths; diode temperature differences must also be eliminated. Good equalization of temperature differences can be achieved by mounting the diodes close together on a common heat sink, but this may complicate the design of the rectifier.

The phenomenon of unequal current sharing is represented in Fig. 8-12. Clearly, if I_{tot} is twice the rated forward current, diode D_1 will work beyond its current rating. This effect is worsened by the increase of junction temperature occurring under operating conditions, since around the rated current level the forward voltage decreases as temperature rises. The characteristics of both diodes will shift toward lower forward voltages,

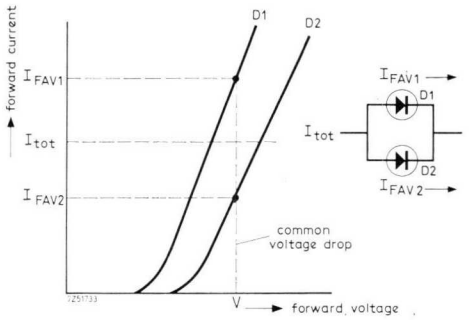


Fig. 8-12 Forward characteristics showing reason for unequal current distribution in diodes connected in parallel.

but the shift will be greatest for the diode D_1, causing this to take a still greater portion of overall forward current (Fig. 8-13), unless the individual characteristic show only minor deviations.

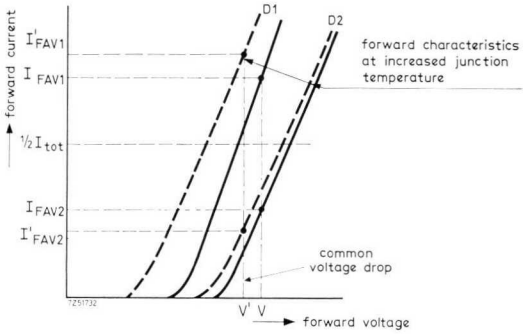


Fig. 8-13 Effect of temperature on forward characteristics.

8.2.1 Current and Temperature Derating

Plots of power loss versus average forward current, as shown in the data sheets, are valid for the worst conditions of maximum anticipated forward voltage drop. A diode having a lower forward voltage drop can obviously carry an average forward current in excess of its specified value without its power rating being exceeded.

Excessive dissipation in any diode can be obviated by *current derating*, that is, using diodes in excess of the number given by the ratio of the total

current to the maximum permissible knee current per diode. The derating is expressed in terms of the factor:

$$f_d = 1 - S + S/n, \tag{8-33}$$

in which n denotes the number of paralleled diodes and S the derating constant for the particular application.

For the derating constant S a value of 0.2 is recommended to run less than 0.1 % risk of overloading any non-matched diode in a parallel bank by excessive dissipation, which gives $f_d = 0.8 + 0.2/n$. The maximum permissible current per diode then becomes:

$$I_{FAV} = f_d I_{FAV\ max} = (0.8 + 0.2/n) I_{FAV\ max}, \tag{8-34}$$

where $I_{FAV\ max}$ is to be found from the data sheet. The total current for the whole bank of diodes is:

$$I_{tot} = nI_{FAV} = (0.8n + 0.2) I_{FAV\ max}. \tag{8-35}$$

A fuse, connected in series with each diode for individual protection, acts as a small series resistance and so will improve current sharing to some extent. In that case S may be reduced to 0.15, which gives $f_d = 0.85 + 0.15/n$.

Example

Calculate the maximum permissible current for ten BYX14 diodes in parallel, operating at maximum junction temperature; the diodes are protected individually by fuses. The rated average forward current is 150 A.

From eq. (8-35), substituting 0.15 for S:

$$I_{tot} = (0.85n + 0.15) I_{FAV\ max} = (0.85 \times 10 + 0.15)150 = 1295 \text{ A}.$$

Occasionally, *temperature derating*, rather than current derating, may be applied. Though a cooling system may be adequate for operation of a single diode at its full rating, the maximum temperature of a diode with low forward resistance may be exceeded if it is paralleled with others. If, however, the base-to-ambient thermal resistance is substantially reduced, the maximum permissible junction temperature of the diodes exhibiting the lowest forward resistance will not be exceeded. The maximum current is thus allowed to attain the rated current per diode, times the number of diodes in parallel. A saving is effected by dispensing with the need for extra diodes; on the other hand, the larger heat sinks or increased forced-air cooling required may not be acceptable.

8.2.2 Forced Current Sharing Methods

Forced current sharing means producing equal current distribution across diodes connected in parallel. The total permissible current than equals the rated current, times the number of paralleled diodes, so no current derating is necessary.

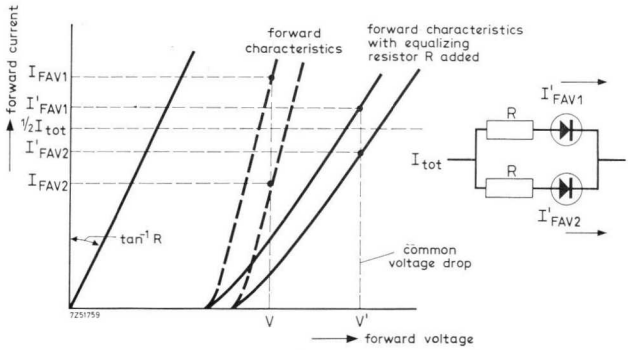


Fig. 8-14 Effect of series resistors on forward characteristics.

Inserting equal resistances in each diode branch reduces the effect of the spread in forward characteristic, thus improving current equalization (Fig. 8-14). The resistor tolerances must be low (usually $\pm$ 5%). Forced sharing by this method obviously increases the power losses, and will affect both system efficiency and load regulation. Adequate current sharing by series resistors requires 1.5 V drop across the resistor at the rated crest working forward current. Thus, for BYX33 diodes (I_{FRM} = 1250 A) the resistors should have a value of 1.5/1250 = 1.2 mΩ. If fuses are installed in each branch, their resistance (e.g. 0.25 mΩ for the fuse to protect the BYX33 should clearly be subtracted from the calculated value of the resistor. All other resistances in the rectifier circuit must be kept to a minimum, or at least equalized, so as not to defect the effect of the series resistors.

The preferred method of current sharing uses balancing reactors, since little power loss or increased current dependence is incurred. The prin-

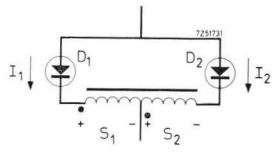
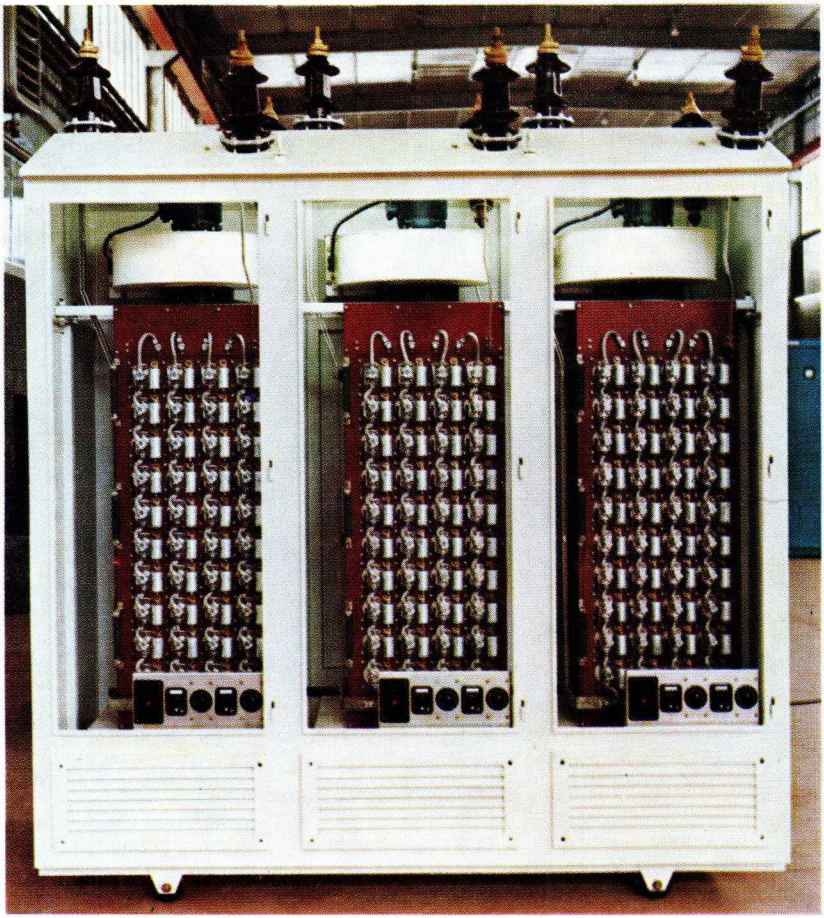
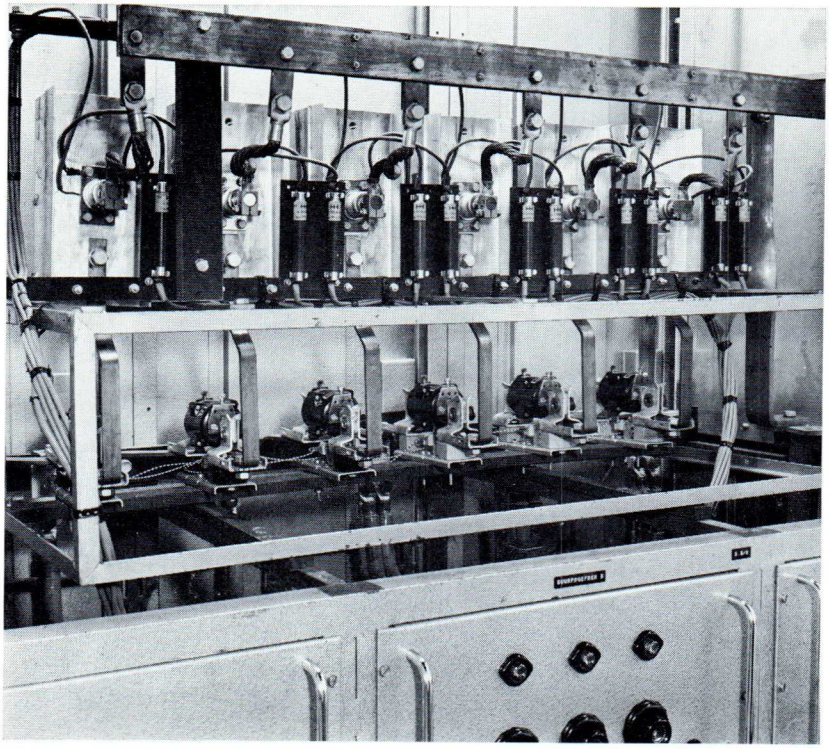


Fig. 8-15 Current sharing using balancing reactors.



Silicion diode power rectifier for traction purposes. Output power 3600 kW per unit. Nominal rectified current 1000 A (by courtesy of BMB Società Italiana Elettronica Industriale Montebello, Vicenza, Italy).



Diodes undergoing life test in the laboratory.

ciple of this technique is depicted in Fig. 8-15. If diode D_1 has the lowest threshold, it will start conducting first. Current I_1 sets up a counter-e.m.f. across both windings S_1 and S_2 as shown, reducing the forward voltage across D_1, and forcing D_2 to conduct. When the conduction period ceases, I_2 will decrease first (D_2 having the higher threshold). This again generates a counter-e.m.f. as indicated, increasing the conduction period of D_2 and reducing that of D_1. The result is that D_1 and D_2 carry substantially equal currents.

The following empirical formula gives the recommended inductance L (in mH) of *each* winding in terms of the diode crest working forward current:

$$L = 20\,000/\omega_s I_{FRM}. \tag{8-36}$$

The most important magnetic requirements for a balancing reactor are high saturation flux density and low residual flux density, to obtain the largest change in total flux per cycle. The core must be capable of generating a current-balancing voltage throughout the conduction period without saturation. The core may have an air gap to return the flux density to a low level upon completion of each conduction period; alternatively a reset winding may be used to reverse the flux before the start of the next period.

In a single-phase circuit (conduction angle 180°) the total flux developed during each conduction period equals the product of the forward voltage mismatch (conservatively 0.5 V) and the conduction period $1/2f_s$. For a six-phase supply (conduction angle 60°) the conduction period equals $1/6f_s$.

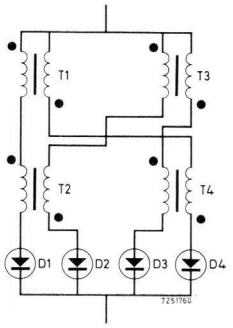
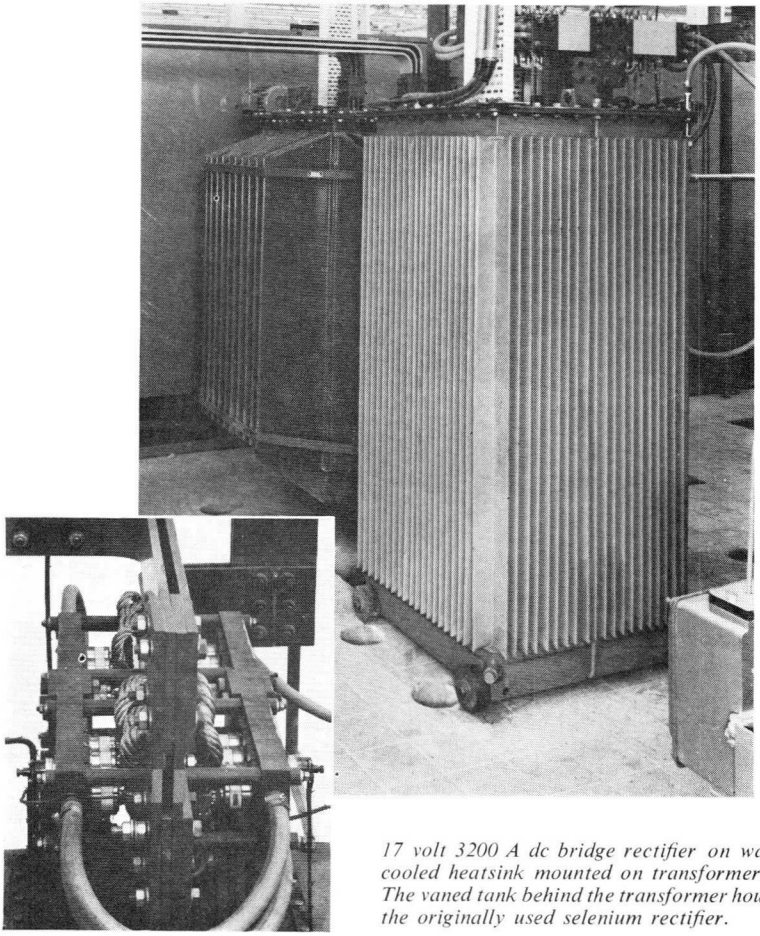


Fig. 8-16 Current balancing for more than two diodes.

A balancing reactor scheme for more than two diodes in parallel is shown in Fig. 8-16. When one diode starts to conduct, a voltage is generated in the reactors, which forces the other diodes to conduct. Say, diode D_1 starts conducting first (lowest threshold) then D_4 and D_2 start conducting through T_1 and T_2 respectively; voltages thus generated in both T_4 and T_3 start conduction in D_3. Where more than a few parallel paths are required, current balancing by reactors will prove most satisfactory, despite the cost and the transients produced during commutation.



17 volt 3200 A dc bridge rectifier on water cooled heatsink mounted on transformer. The vaned tank behind the transformer houses the originally used selenium rectifier.

9 Survey of Rectifier Circuits

Each rectifier configuration has its own characteristic properties; the following is a guide to rectifier systems for particular applications.

To avoid confusion, we shall first lay down the terminology used. The number of phases is taken equal to the number of secondary transformer windings supplying voltages whose waveforms are mutually shifted in time. This implies that a rectifier using a centre tap on a single transformer winding is called a two-phase rectifier because the two secondary voltages are 180° apart*. The part of the cycle during which current is supplied by a phase depends on how and where the diodes are connected. The term "half-wave" is used when current flows through the corresponding winding in one direction only. The term "full-wave" is used when the current flows through the winding in each direction alternately.

The selection of a particular rectifier circuit is governed by factors such as circuit economy, efficiency and the ratings of available diodes.

In low-power circuits, if a low ripple frequency and a fairly high ripple content are acceptable, supply from a single-phase mains (single-phase or two-phase rectifying circuits) may be adequate. But if higher output power is required, supply from three-phase mains (using three-phase or six-phase rectifying circuits) will be preferable because of the lower ripple factor and higher conversion efficiency (see Section 9.2.1) even though the commutation losses are greater.

When the available a.c. supply voltage is adequate, some rectifier circuits may be connected directly to it without a transformer (this is both money- and space-saving) provided precautions are taken to make the system safe for the user.

9.1 Rectifier Systems

The most common rectifier systems will now be discussed in brief, assuming the load to be purely resistive. Distinction is made between

* Many sources describe a two-phase system as one in which there are two voltages anyone of which is displaced in phase by 90° with respect to the other.

half-wave rectifiers, full-wave rectifiers and rectifiers incorporating an interphase transformer.

9.1.1 Half-wave Rectifiers

Half-wave rectifiers have in common that the average diode current per phase is:

$$I_{FAV} = I_o/n, \tag{9-1}$$

in which I_o denotes the direct output current and n the number of phases.

The r.m.s. diode current amounts to:

$$I_{F\ \mathrm{rms}} = (1/\sqrt{n})I_{o\ \mathrm{rms}}, \tag{9-2}$$

where $I_{o\ \mathrm{rms}}$ denotes the r.m.s. value of the output current.

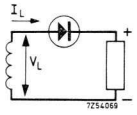


Fig. 9-1 Single-phase half-wave.

Fig. 9-1 shows the *single-phase half-wave circuit*. The conduction angle of the diode is 180°. Since $n = 1$, it follows from eqs (9-1) and (9-2):

$$I_{FAV} = I_o, \quad I_{F\ \mathrm{rms}} = I_{o\ \mathrm{rms}},$$

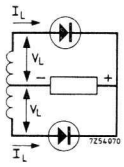


Fig. 9-2 Two-phase half-wave.

In the two-phase half-wave circuit of Fig. 9-2. (not to be confused with the single-phase full-wave circuit discussed below, (cf. Fig. 9-5) the two opposed phases have one point in common, so that the transformer secondary is normally a single center-tapped winding. The conduction angle of the diodes is again 180°. According to eqs (9-1) and (9-2):

$$I_{FAV} = I_o/2, \quad I_{F\ \mathrm{rms}} = (1/\sqrt{2})I_{o\ \mathrm{rms}}.$$

Fig. 9-3 shows the three-phase half-wave circuit in which the conduction angle of the diodes is 120°.

$$I_{FAV} = I_o/3, \quad I_{F\ \mathrm{rms}} = (1/\sqrt{3})I_{o\ \mathrm{rms}}.$$

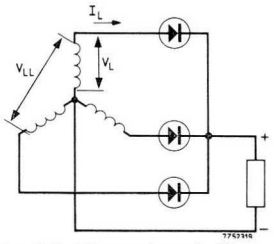


Fig. 9-3 Three-phase half-wave.

In the *six-phase half-wave circuit* of Fig. 9-4 the conduction angle of the diodes is 60°.

$$I_{FAV} = I_o/6, \quad I_{F\ \mathrm{rms}} = (1/\sqrt{6})I_{o\ \mathrm{rms}}.$$

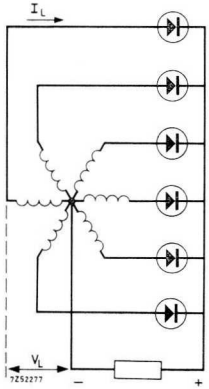


Fig. 9-4 Six-phase half-wave.

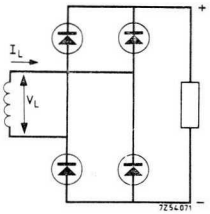


Fig. 9-5 Single-phase full-wave.

9.1.2 Full-wave Rectifiers

Fig. 9-5 shows the circuit of the single-phase full-wave rectifier; the conduction agle of the diodes is 180°. The average diode current and the r.m.s. diode current are identical to those of the two-phase half-wave circuit, namely:

$$I_{FAV} = I_o/2, \quad I_{F\ \mathrm{rms}} = (1/\sqrt{2})I_{o\ \mathrm{rms}}. \tag{9-3}$$

In the *three-phase full-wave circuit* the secondary transformer winding may be connected either in star (Fig. 9-6) or in delta (Fig. 9-7). Both rectifier configurations are fundamentally the same, so that the data quoted below is identical, provided that the transformer secondary line

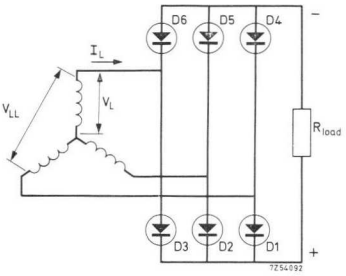


Fig. 9-6 Three-phase full-wave (star connected secondary).

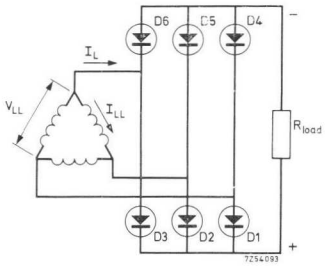


Fig. 9-7 Three-phase full-wave (delta connected secondary).

voltages are the same; the phase voltage of the delta-connected secondary must therefore be $\sqrt{3}$ times the phase voltage of the star-connected secondary. Expressions for the average diode current and the r.m.s. diode current are identical to those of the three-phase half-wave circuit, that is:

$$I_{FAV} = I_o/3, \quad I_{F\,\mathrm{rms}} = (1/\sqrt{3})I_{o\,\mathrm{rms}}.$$

9.1.3 Rectifiers with Interphase Transformer

The transformer of a rectifier for supply from the three-phase mains may be provided with two separate three-phase secondaries linked by an interphase transformer. In this way two complete paralleled three-phase rectifying systems, mutually shifted in phase, are obtained. The interphase transformer prevents a conducting diode in one three-phase secondary from making a diode in the other secondary non-conducting. The interphase transformer operates as an inductive divider balancing the differences in instantaneous voltage outputs. This principle may be applied both to half-wave and to full-wave rectifiers.

Fig. 9-8 shows the *three-phase double-star half-wave circuit*. One set of three-phase supply voltages is shifted 60° relative to the other to provide a six-phase output. However, the conducting angle of the diodes approaches 120° owing to the presence of the interphase transformer. The average diode current and the r.m.s. diode current are respectively:

$$I_{FAV} = I_o/6, \quad I_{F\,\mathrm{rms}} = (1/2\sqrt{3})I_o.$$

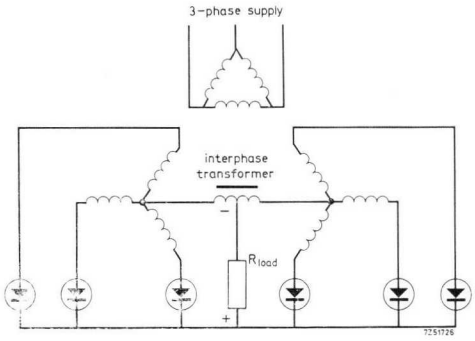


Fig. 9-8 Three-phase half-wave double star with interphase transformer.

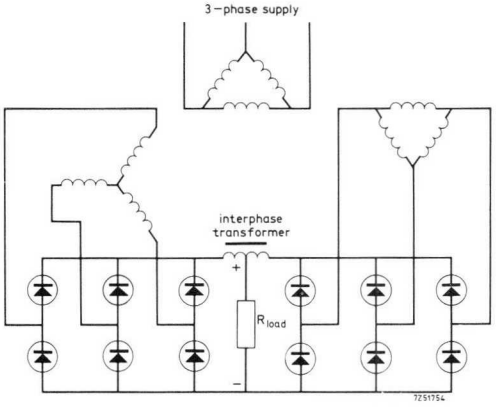


Fig. 9-9 Three-phase full-wave star delta with interphase transformer.

The three-phase star-delta full-wave circuit is shown in Fig. 9-9. The phase voltage of the delta-connected secondary is $\sqrt{3}$ times the phase voltage of the star-connected secondary. The two sets of supply voltage are mutually shifted 30° to produce a 12-phase output, thus providing an almost ripple-free output voltage, but the conduction angle of the diodes is very nearly 120°. The average diode current and the r.m.s. diode current are:

$$I_{FAV} = I_o/6, \quad I_{F\,\mathrm{rms}} = (1/2\sqrt{3})I_{o\,\mathrm{rms}}.$$

9.2 Important Rectifier Characteristics

9.2.1 Conversion Efficiency, Form Factors, Ripple Factors

In an ideal rectifier system all a.c. input power is converted into d.c. output power. In practice the a.c. power is converted only partially, some of the remainder being dissipated as an a.c. component, the ripple. Its magnitude is referred to as the ripple content; the smaller the ripple content, the better the a.c./d.c. conversion, which is expressed in terms of the conversion efficiency, η_c. The conversion efficiency is equal to the d.c. output power as a fraction of the active a.c. input power of the rectifier system. A smoothing filter across the rectifier output will reduce the ripple and hence boost the conversion efficiency of the system, provided the filter itself introduces no losses.

In the following analysis the conversion efficiency is calculated for a purely *resistive* load R_{load} (see Fig. 9-10), it being assumed that the rectifier system is free of ohmic losses, that all resistances in supply lines and

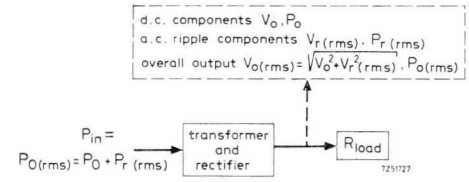


Fig. 9-10 A.C. and d.c. components in a rectifier system.

transformer windings and losses in the diodes are negligible, and that no smoothing filters are used.

Under these conditions the r.m.s. input power can be expressed by:

$$P_{in} = P_{o\,\mathrm{rms}} = P_o + P_{r\,\mathrm{rms}}$$
$$= V_{o\,\mathrm{rms}}^2/R_{load} = V_o^2/R_{load} + V_{r\,\mathrm{rms}}^2/R_{load}, \qquad (9\text{-}4)$$

in which

P_{in} = r.m.s. input power,
$P_{o\,\mathrm{rms}}$ = r.m.s. output power (total),
P_o = d.c. output power,
$P_{r\,\mathrm{rms}}$ = r.m.s. ripple power (in the load),
$V_{o\,\mathrm{rms}}$ = r.m.s. output voltage (total)
V_o = d.c. output voltage
$V_{r\,\mathrm{rms}}$ = r.m.s. ripple voltage (across the load).

Hence:

$$1 + V_{r\,\mathrm{rms}}^2/V_o^2 = V_{o\,\mathrm{rms}}^2/V_o^2. \tag{9-5}$$

Introducing the output voltage ripple factor

$$F_{rv} = V_{r\,\mathrm{rms}}/V_o, \tag{9-6}$$

and the output voltage form factor

$$F_{fv} = V_{o\,\mathrm{rms}}/V_o, \tag{9-7}$$

gives:

$$F_{fv} = \sqrt{(1 + F_{rv}^2)}. \tag{9-8}$$

For values of F_{rv} much smaller than unity, eq. (9-8) reduces to:

$$F_{fv} = 1 + F_{rv}^2/2. \tag{9-9}$$

The conversion efficiency η_c can be expressed by:

$$\eta_c = P_o/P_{in} = P_o/(P_o + P_{r\,\mathrm{rms}}) = V_o^2/(V_o^2 + V_{r\,\mathrm{rms}}^2),$$

or

$$\eta_c = 1/(1 + F_{rv}^2) = 1/F_{fv}^2. \tag{9-10}$$

Similarly, expressing all quantities in terms of current instead of voltage, we find for the output current ripple factor:

$$F_{ri} = I_{r\,\mathrm{rms}}/I_o, \tag{9-11}$$

and for the output current form factor:

$$F_{fi} = I_{o\,\mathrm{rms}}/I_o. \tag{9-12}$$

Hence:

$$F_{fi} = \sqrt{(1 + F_{ri}^2)}. \tag{9-13}$$

If F_{ri} is much smaller than unity, eq. (9-13) reduces to:

$$F_{fi} = 1 + F_{ri}^2/2. \tag{9-14}$$

The conversion efficiency may thus also be expressed by:

$$\eta_c = 1/(1 + F_{ri}^2) = 1/F_{fi}^2. \tag{9-15}$$

The form factors for the voltage and current are the same for a resistive load, and so are the two ripple factors. Table 9-1 summarizes for the several rectifier configurations (under the conditions presumed) the form factors, the ripple factors and the resulting conversion efficiency.

Table 9-I

rectifier configuration	$F_{rv} = F_{ri}$	$F_{fv} = F_{fi}$	η_c
single-phase half-wave	1.210	1.57	0.407
two-phase half-wave	0.484	1.11	0.813
three-phase half-wave	0.183	1.02	0.963
six-phase half-wave	0.042	~1.00	0.998
single-phase full-wave	0.484	1.11	0.813
three-phase full-wave	0.042	~1.00	0.998
three-phase double-star half-wave	0.042	~1.00	0.998
three-phase double-star or star-delta full-wave	0.010	~1.00	1.000

Since the waveform of the output voltage does not depend on the type of load, the values of the output voltage ripple factor F_{rv} and of the output voltage from factor F_{fv} quoted in Table 9-1 are also applicable with an *inductive* load.

If the ratio of the load's inductive reactance to resistance is large at the fundamental ripple frequency, then almost pure d.c. flows through the load. The conversion efficiency approaches unity and the output current form factor F_{fi} approaches zero.

9.2.2 Commutation Voltage Drop

When a ripple current flows through the load the calculation of the commutation voltage drop becomes very complex. We shall therefore confine our attention to the case of pure d.c. flowing through the load.

The commutation losses are due to the current transfer from one phase to the next (commutation) taking a finite time because the transformer and line leakage inductance (leakage reactance X_{LL}) oppose a sudden current rise and decay. As a result, the diode in one phase starts to conduct before the current in the preceding phase has decayed to zero; the period during which both diodes conduct is termed the commutation time. The output voltage waveform is modified during the commutation time, causing some loss of average output, so that the effect of transformer leakage is to create a commutation voltage drop. The resulting loss in output voltage is proportional to the number of phases.

In addition, at conduction angles of 60° or less, a limit may be imposed on the d.c. output current by the maximum repetitive peak current which is then apt to surpass the diode ratings even though the average current is well within the specified value. In the case of supply from the three-phase mains this difficulty might be circumvented by connecting an inter-

phase transformer between two three-phase secondaries. The conduction angle of the diodes can be almost doubled in this way.

The commutation or current transfer from phase 1 to the succeeding phase 2 starts when the corresponding line voltages become equal that is, when $V_{L2} = V_{L1}$ (see Fig. 9-11*a*).

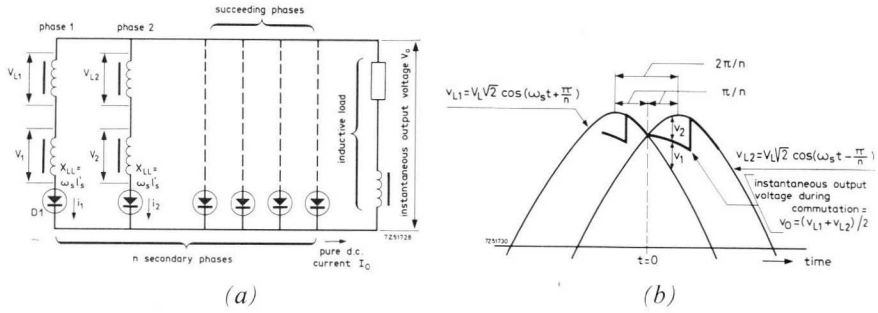


Fig. 9-11 Commutation in a polyphase rectifier system.

The following analysis assumes equal values of X_{LL} for all phases. The voltage which forces the current i_1 in phase 1 down and the current i_2 in phase 2 up is given by $v_{L2} - v_{L1}$. However, the decay of i_1 is opposed by an instantaneous voltage v_1 induced in half the line-to-line reactances due to the change of current flow during commutation, and the rise of i_2 is opposed by a similar instantaneous voltage v_2. Because pure d.c. current is assumed to flow, the rise of i_1 and the decay of i_2 are conjugate, which means that $\mathrm{d}i_2/\mathrm{d}t = -\mathrm{d}i_1/\mathrm{d}t$ and $|v_1| = |v_2|$. Thus, during commutation, the instantaneous rectifier output voltage is:

$$v_o = (v_{L1} + v_{L2})/2. \tag{9-16}$$

The commutation period ceases as soon as i_1 has dropped to zero, which causes a jump in the output voltage (cf. Fig. 9-11*b*), since, after commutation, the load voltage follows V_{L2}. The jump in output voltage is restricted by transformer resonance phenomena.

The currents occurring during commutation are derived by applying Kirchhoff's law to the circuit consisting of phases 1 and 2:

$$\Sigma\, v = 0 = v_{L1} - (X_{LL}/\omega_s)\,(\mathrm{d}i_1/\mathrm{d}t) - \\ - v_{L2} + (X_{LL}/\omega_s)\,(\mathrm{d}i_2/\mathrm{d}t). \tag{9-17}$$

The sum of the phase currents i_1 and i_2 clearly equals the d.c. output current:

$$i_1 + i_2 = I_0. \tag{9-18}$$

Assuming commutation to start at $t = 0$, and denoting the number of secondary phases by n gives:

$$\left.\begin{aligned} v_{L1} &= V_L\sqrt{2} \cdot \cos(\omega_s t + \pi/n), \\ v_{L2} &= V_L\sqrt{2} \cdot \cos(\omega_s t - \pi/n). \end{aligned}\right\} \tag{9-19}$$

Substituting eqs (9-18) and (919) in eq. (9-17) and integrating the resulting differentials gives:

$$i_1 = I_o - V_L\sqrt{2} \cdot \sin(\pi/n) \cdot (1 - \cos \omega_s t)/X_{LL}, \tag{9-20}$$

and

$$i_2 = V_L\sqrt{2} \cdot \sin(\pi/n) \cdot (1 - \cos \omega_s t)/X_{LL}, \tag{9-21}$$

During commutation both D_1 and D_2 will be conductive causing a short-circuit current to flow between phases 1 and 2 as a result of the commutation voltage $v_{L2} - v_{L1}$, and limited by $2X_{LL}$. Thus, the peak steady-state fault current per line is:

$$I_{LM\,sc} = (v_{L2} - v_{L1})_{max}/2X_{LL},$$

whence from eq. (9-19)

$$I_{LM\,sc} = V_L\sqrt{2} \cdot \sin(\pi/n)/X_{LL}. \tag{9-22}$$

Rewriting eqs (9-20) and (9-21) and introducing eq. (9-22) gives:

$$i_1 = I_o - I_{LM\,sc} + I_{LM\,sc} \cos \omega_s t, \tag{9-23}$$

and

$$i_2 = I_{LM\,sc} - I_{LM\,sc} \cos \omega_s t. \tag{9-24}$$

These equations are plotted in Fig. 9-12. Since the fault current stops when diode D_1 in Fig. 9-11 ceases to conduct ($i_1 = 0$) the current does not reach the value given by eq. (9-22), as shown in broken line.

During commutation the instantaneous output voltage follows from eq. (9-19):

$$v_o = (v_{L1} + v_{L2})/2 = V_L\sqrt{2} \cdot \cos(\pi/n) \cdot \cos \omega_s t, \tag{9-25}$$

(from which it is seen that v_o is part of a cosine function as shown by the broken line in Fig. 9-12 representing the voltages).

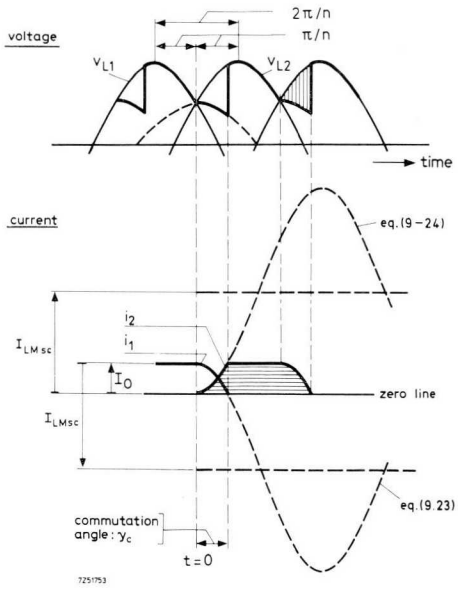


Fig. 9-12 Current and voltage during commutation.

Commutation ceases when the current in the preceding phase is reduced to zero. Therefore, the commutation angle γ_c is derived by making eq. (9-20) equal to zero and solving it for $\omega_s t = \gamma_c$, which gives:

$$\cos \gamma_c = 1 - I_o X_{LL} / V_L \sqrt{2} \cdot \sin(\pi/n). \tag{9-26}$$

The commutation voltage drop represented by the vertically hatched area in Fig. 9-12 is derived as follows. The height of this area at any instant equals the instantaneous voltage induced in half the phase-to-phase leakage reactance X_{LL}, that is:

$$v_1 = -L_s'(\mathrm{d}i_1/\mathrm{d}t).$$

The commutation voltage drop is:

$$V_c = (n/2\pi) \int_0^{\gamma_c} v_1 \cdot d\omega_s t. \tag{9-27}$$

Substituting the first derivative of eq. (9-20) in eq. (9-27), solving the integral and substituting eq. (9-26) gives:

$$V_c = n I_o X_{LL} / 2\pi. \tag{9-28}$$

This expression shows that the commutation voltage drop is proportional to the number of phases, to the load current and to the line-to-line leakage reactance.

Neglecting the commutation voltage drop, the rectifier d.c. output voltage V_{o0} at zero load would equal the area enclosed between the time axis and the curve representing the sinusoidal output pulses (see Fig. 9-12):

$$V_{o0} = (n/2\pi) \int_{-\pi/n}^{+\pi/n} V_L\sqrt{2} \cdot \cos \omega_s t \cdot \mathrm{d}\omega_s t = (n/\pi) V_L\sqrt{2} \cdot \sin(\pi/n). \quad (9\text{-}29)$$

From eqs (9-28) and (9-29) the per unit commutation voltage drop is:

$$\varepsilon_c = V_c/V_{o0} = I_o X_{LL}/2V_L\sqrt{2} \cdot \sin(\pi/n). \quad (9\text{-}30)$$

Introducing this expression into eq. (9-26) yields:

$$\cos \gamma_c = 1 - 2\varepsilon_o. \quad (9\text{-}31)$$

9.2.3 The Rectifier Constant K

Eq. (9-28) shows that the commutation voltage drop is proportional to the line-to-line leakage reactance X_{LL} as measured between successive secondary phases with the transformer primary short-circuited. On the other hand, the available fault current with all secondary phases short-circuited is determined by the leakage reactance X_L caused by the leakage inductance of each individual phase.

The available short-circuit kVA-value equals $1/x$ times the rated kVA-value, where x denotes the per unit transformer impedance per phase or, in other words, x equals X_L divided by the rated a.c. load per secondary phase.

If the windings of a secondary phase are on a single core leg, X_L and X_{LL} are equal, whereas due to the effect of mutual inductance X_L will differ from X_{LL} when the windings of a secondary phase are distributed over several legs.

The ratio of the per unit commutation voltage drop ε_c to the per unit transformer impedance per phase, x, is a characteristic of the type of rectifier configuration, and is termed the rectifier constant

$$K = \varepsilon_c/x. \quad (9\text{-}32)$$

Hence, from eq. (9-31), if pure d.c. flows through the load:

$$\cos \gamma_c = 1 - 2Kx. \quad (9\text{-}33)$$

The rectifier constant K is specified in Table 9-2 for several rectifier configurations (with inductive load).

Table 9-2

rectifier configuration	K
two-phase half-wave	0.707
three-phase half-wave	0.866
six-phase half-wave	1.5
single-phase full-wave	0.707
three-phase full-wave	0.5
three-phase double-star half-wave	0.5

This table illustrates that K and hence the commutation voltage drop increases with the number of phases. Because the per unit impedance per phase is usually dictated by the permissible fault current level, the load regulation will deteriorate as the number of phases is increased, although the ripple will be reduced.

Example
The transformer impedance per secondary phase in a six-phase half-wave rectifier is 5% of the rated a.c. load. Calculate the commutation angle γ_c and the per unit commutation voltage drop ε_c.

From Table 9-2 it is seen that $K = 1.5$ whilst $x = 0.05$. Hence, from eq. (9-32):

$$\varepsilon_c = Kx = 1.5 \times 0.05 = 0.075 = 7.5\%.$$

From eq. (9-33):

$$\cos \gamma_c = 1 - 2Kx = 1 - 2 \times 0.075 = 0.85,$$

which gives $\gamma_c = 31°47'$.

To improve the load regulation, several systems in parallel, coupled via interphase transformers, could be used. With this method, provided the mutual phase shift angles between the supply voltages of the three-phase supply are correct, both the output ripple and the number of commutations per cycle for each system can be reduced. This gives improved load regulation at a given transformer impedance per secondary phase, as may be seen from the value of K for the three-phase double-star half-wave configuration.

Example
The transformer impedance per secondary phase is as given in Example 1. To improve the load regulation a three-phase double-star half-wave rectifier circuit is used.

Table 9-2 shows that $K = 0.5$ in this case; x being again 0.05. This gives from eq. (9-32):

$$\varepsilon_c = Kx = 0.5 \times 0.05 = 0.025 = 2.5\%,$$

whilst from eq. (9-33):

$$\cos \gamma_c = 1 - 2Kx = 1 - 2 \times 0.025 = 0.95,$$

corresponding to $\gamma_c = 18°12'$, which is a substantial improvement.

The three-phase full-wave configuration gives a performance comparable to the three-phase double-star half-wave circuit in this respect.

9.3 Design Considerations - Single Phase Mains Input Rectifiers

9.3.1 General

The single phase mains which is the most readily available source of power, is sufficient for the supply of many low and medium power rectifiers. The single phase mains input rectifier is, in general, a simpler and cheaper installation than the equivalent three phase type, although reduction of the ripple content in the rectifier output is more difficult.

If a transformer is used to supply the power to the single-phase half-wave circuit, the secondary of the transformer carries unidirectional current each time the diode conducts. The transformer has to be rated at the maximum r.m.s. current that flows through the rectifier; the utility factor of the transformer is low. This unidirectional current can lead to core saturation, which in turn leads to increases in magnetising current and hysteresis loss, and introduction of harmonics in the secondary voltage. The regulation and conversion efficiency of the single-phase half-wave circuit is low. Because of the disadvantages this circuit is normally only used direct from the mains, for low currents (e.g. radio and TV receivers).

Although the two-phase half-wave rectifier uses only two diodes compared to four for the single-phase full-wave rectifier, the transformer kVA rating required for the former is greater, and the cost of this transformer is the principal drawback of the two-phase half-wave circuit.

The single-phase full-wave circuit is the more widely used of the two. It is generally used wherever the desired output voltage should be approximately equal to the r.m.s. supply voltage. The two-phase half-wave circuit is used more for low-voltage applications; this is because in a full wave circuit the output current flows through at least two diodes thus giving a greater forward voltage drop than in the half wave circuit.

It is important to know the type of load — resistive, capacitive, or inductive — when determining the values of the components used in the installation. The following sections deal with the calculations necessary to design an installation for each of these three load types.

9.3.2 Rectifiers with Resistive Loads

Design of the single phase mains input rectifier with resistive load is fairly straight-forward. To illustrate, we shall take as an example the single-phase full-wave type rectifier, and calculate the voltage and current relationships, the transformer rating, and the ripple. This data is listed in Table 9-3 for the other types of rectifier.

Voltages. The instantaneous rectifier output voltage v_o at instant t is expressed by:

$$v_o \simeq \frac{2}{\pi} V_{oM} - \frac{4}{3\pi} V_{oM} \cos 2\,\omega_s t. \tag{9-34}$$

The peak value of the output voltage V_{oM} equals the peak value $\sqrt{2}V_L$ of the input voltage. The output voltage V_o in terms of V_{oM} is, from eq. (9-34):

$$v_o = \frac{2}{\pi} V_{oM} = 0.636\, V_{oM}.$$

The output voltage V_o in terms of the r.m.s. output voltage $V_{o\,\mathrm{rms}}$ is derived from:

$$V_{o\,\mathrm{rms}} = \sqrt{\left(\frac{1}{2\pi}\int_0^{2\pi} V_{oM}^2 \sin^2\omega_s t \, \mathrm{d}(\omega_s t)\right)},$$

$$= V_{oM}\sqrt{\left(\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1}{2} - \frac{\cos 2\,\omega_s t}{2}\right)\mathrm{d}(\omega_s t)\right)}$$

$$= \frac{V_{oM}}{\sqrt{2}},$$

so that

$$V_o = 0.636\sqrt{2}\, V_{o\,\mathrm{rms}} = 0.9\, V_{o\,\mathrm{rms}}.$$

Table 9-3 Idealized rectifier circuit performance (part 1a)

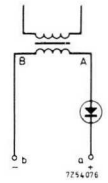
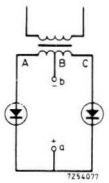
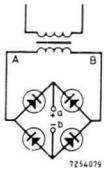
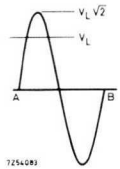
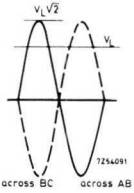
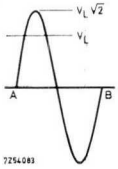
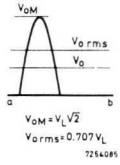
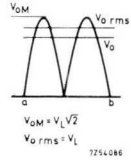
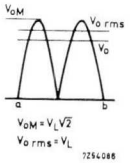
	single-phase half-wave	two-phase half-wave	single-phase full-wave
type of rectifier circuit			
secondary input voltage per phase			
output voltage across *a-b*			
output voltage pulses per cycle (*N*)	1	2	2

Table 9-3 Idealized rectifier circuit performances (part 1b)

		single-phase half-wave	two-phase half-wave	single-phase full-wave
output voltage				
d.c. output voltage V_o		$0.45V_L$	$0.90V_L$	$0.90V_L$
r.m.s. output voltage $V_{o\,\mathrm{rms}}$		$1.57V_o$	$1.11V_o$	$1.11V_o$
peak output voltage V_{oM}		$3.14V_o$	$1.57V_o$	$1.57V_o$
output current				
average current per rectifier leg I_{FAV}		I_o	$0.5\ I_o$	$0.5\ I_o$
$I_{F\,\mathrm{rms}}$ per rectifier leg	R	$1.57I_o$	$0.785I_o$	$0.785I_o$
	L		$0.707I_o$	$0.707I_o$
I_{oM} per rectifier leg	R	$3.14I_o$	$1.57I_o$	$1.57I_o$
	L		I_o	I_o
transformer rating				
secondary r.m.s. voltage per transformer leg V_L		$2.22V_o$	$1.11V_o$ (to center tap)	$1.11V_o$ (total)
secondary r.m.s. current per transformer leg I_L	R	$1.57I_o$	$0.785I_o$	$1.11I_o$
	L		$0.707I_o$	I_o
secondary volt amperes VA_s	R	$3.48V_oI_o$	$1.74V_oI_o$	$1.23V_oI_o$
	L		$1.57V_oI_o$	$1.11V_oI_o$
primary voltage per transformer leg (transf. ratio 1 : 1)		$2.22V_o$	$1.11V_o$	$1.11V_o$
primary current per transformer leg (transf. ratio 1 : 1)	R	$1.57I_o$	$1.11I_o$	$1.11I_o$
	L		I_o	I_o
primary volt amperes VA_p	R	$3.48V_oI_o$	$1.23V_oI_o$	$1.23V_oI_o$
	L		$1.11V_oI_o$	$1.11V_oI_o$
primary line current I_L	L		I_o	I_o
fundamental ripple frequency f_r		f	$2f$	$2f$
percentage ripple $100V_{fr\,\mathrm{rms}}/V_o$		111	47.2	47.2
circuit imposed crest voltage		$3.14V_o$	$3.14V_o$	$1.57V_o$
		$1.41V_L$	$2.82V_L$	$1.41V_L$

R = resistive load L = inductive load f = supply frequency

In the calculation of the above circuit performances, the rectifier forward voltage drop and the transformer impedance have been ignored. Figures for primary transformer volt ampere ratings neglect magnetizing current.

Table 9-3 Idealized rectifier circuit performance (part 2a)

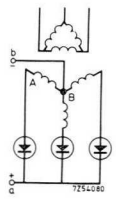
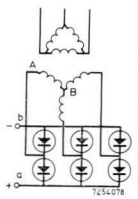
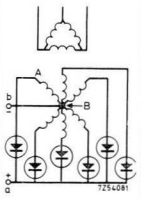
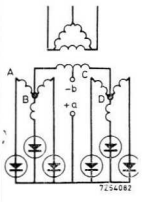
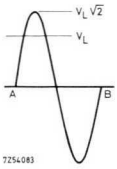
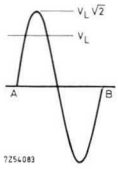
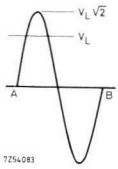
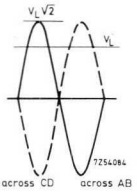
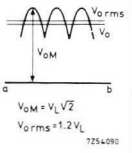
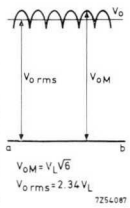
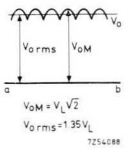
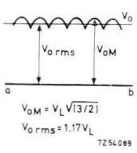
	three-phase half-wave	three-phase full-wave	six-phase half-wave	double-star with inter-phase transf.
type of rectifier circuit				
secondary input voltage per phase				
output voltage across *a-b*				
output voltage pulses per cycle (N)	3	6	6	6

Table 9-3 Idealized rectifier circuit performances (part 2b)

		three-phase half-wave	three-phase full-wave	six-phase half-wave	double-star with interphase transf.
output voltage					
d.c. output voltage V_o		$1.17V_L$	$2.34V_L$	$1.35V_L$	$1.17V_L$
r.m.s. output voltage $V_{o\,\mathrm{rms}}$		$1.02V_o$	V_o	V_o	V_o
peak output voltage V_{oM}		$1.21V_o$	$1.05V_o$	$1.05V_o$	$1.05V_o$
output current					
average current per rectifier leg I_{FAV}		$0.333I_o$	$0.333I_o$	$0.167I_o$	$0.167I_o$
$I_{F\,\mathrm{rms}}$ per rectifier leg	R	$0.588I_o$	$0.577I_o$	$0.408I_o$	$0.293I_o$
	L	$0.577I_o$	$0.577I_o$	$0.408I_o$	$0.289I_o$
I_{oM} per rectifier leg	R	$1.21I_o$	$1.05I_o$	$1.05I_o$	$0.525I_o$
	L	I_o	I_o	I_o	I_o
transformer rating					
secondary r.m.s. voltage per transformer leg V_L		$0.855V_o$ (to neutral)	$0.428V_o$ (to neutral)	$0.74V_o$ (to neutral)	$0.855V_o$ (to neutral)
secondary r.m.s. current per transformer leg I_L	R	$0.588I_o$	$0.816I_o$	$0.408I_o$	$0.293I_o$
	L	$0.577I_o$	$0.816I_o$	$0.408I_o$	$0.289I_o$
secondary volt amperes VA_s	R	$1.50V_oI_o$	$1.05V_oI_o$	$1.81V_oI_o$	$1.50V_oI_o$
	L	$1.48V_oI_o$	$1.05V_oI_o$	$1.81V_oI_o$	$1.48V_oI_o$
primary voltage per transformer leg (transf. ratio 1 : 1)		$0.855V_o$	$0.428V_o$	$0.740V_o$	$0.855V_o$
primary current per transformer leg (transf. ratio 1 : 1)	R	$0.484I_o$	$0.816I_o$	$0.577I_o$	$0.408I_o$
	L	$0.471I_o$	$0.816I_o$	$0.577I_o$	$0.408I_o$
primary volt amperes VA_p	R	$1.24V_oI_o$	$1.05V_oI_o$	$1.28V_oI_o$	$1.05V_oI_o$
	L	$1.21V_oI_o$	$1.05V_oI_o$	$1.28V_oI_o$	$1.05V_oI_o$
primary line current I_L	L	$0.817I_o$	$1.410I_o$	$0.817I_o$	$0.707I_o$
fundamental ripple frequency f_r		$3f$	$6f$	$6f$	$6f$
percentage ripple $100V_{fr\,\mathrm{rms}}/V_o$		17.7	4.0	4.0	4.0
circuit imposed crest voltage	L	$2.09V_o$	$1.05V_o$	$2.09V_o$	$2.42V_o$
		$2.45V_L$	$2.45V_L$	$2.83V_L$	$2.83V_L$

R = resistive load L = inductive load f = supply frequency

In the calculation of the above circuit performances, the rectifier forward voltage drop and the transformer impedance have been ignored. Figures for primary transformer volt ampere ratings neglect magnetizing current.

The total transformer secondary r.m.s. voltage per phase is given by:

$$V_L = \frac{V_o}{0.9} = 1.11\ V_o,$$

and the crest working voltage is:

$$V_{RWM} = \sqrt{2}V_L = 1.57\ V_o.$$

In terms of $V_{o\ \text{rms}}$,

$$V_{RWM} = \sqrt{2}\ V_{o\ \text{rms}} = 1.414\ V_{o\ \text{rms}}.$$

Currents. The output current waveform is the same as the output voltage waveform for resistive load.

The output current I_o in terms of I_{oM} is given by

$$I_o = \frac{2\ V_{oM}}{\pi R_{load}} = 0.636\ I_{oM}.$$

The output current I_o in terms of $I_{o\ \text{rms}}$ is given by:

$$I_o = 0.9\ \frac{V_{o\ \text{rms}}}{R_{load}} = 0.9\ I_{o\ \text{rms}}.$$

The total direct current is supplied via two pairs of diodes, so that the average current per diode leg is:

$$I_{FAV} = I_o/2.$$

The total r.m.s. current is supplied via two pairs of diodes, so that r.m.s. current per diode leg is

$$I_{F\ \text{rms}} = \frac{I_{o\ \text{rms}}}{\sqrt{2}} = \frac{I_o}{0.9\sqrt{2}} = 0.785\ I_o.$$

The peak current per diode leg is:

$$I_{oM} = \frac{V_{oM}}{R_{load}} = \frac{I_o}{0.636} = 1.57\ I_o.$$

Transformer Rating. The transformer secondary r.m.s. current is given by:

$$I_{L\ \text{rms}} = \sqrt{2}\ I_{o\ \text{rms}} = 1.11\ I_o.$$

The VA product of the secondary winding is:

$$VA_{2n} = V_L I_L = 1.23\ V_o I_o.$$

If the primary to the secondary transformer ratio is N, then the VA product of the primary winding is:

$$VA_{1n} = V_L N \times (I_L/N) = V_L I_L = 1.23\, V_o I_o.$$

The utility factor F_{pin} is defined as the ratio of the output power to the volt-amp rating of the transformer. This factor indicates how efficiently the transformer winding is used in a particular circuit.
For the full-wave bridge circuit:

$$\text{Secondary utility factor } F_{p2} = \frac{V_o I_o}{VA_{2n}} = 0.813.$$

$$\text{Primary utility factor } \quad F_{p1} = \frac{V_o I_o}{VA_{1n}} = 0.813.$$

Percentage Ripple. If it is assumed that the amplitudes of the higher harmonics are small compared to that of the fundamental ripple frequency f_r, then:

$$\%\text{ripple} = \frac{\text{fundamental r.m.s. ripple voltage}}{\text{d.c. output voltage}}.$$

From eq. (9.34) the r.m.s. harmonic component at fundamental frequency $V_{r\,\text{rms}}$ (which is twice the supply frequency for this circuit) will be $1/\sqrt{2}$ times the fundamental peak harmonic voltage:

$$V_{r\,\text{rms}} = \frac{4}{3\pi} \cdot \frac{V_{oM}}{\sqrt{2}}.$$

Thus the percentage ripple (r.m.s. load ripple voltage to d.c. output voltage ratio in percent) can be expressed:

$$\%\text{ ripple} = \frac{100\, V_{r\,\text{rms}}}{V_o} = \frac{4}{3\pi} \cdot \frac{V_{oM}}{\sqrt{2}} \cdot \frac{\pi}{2\, V_{oM}} \cdot 100 = 47.2.$$

9.3.3 Rectifiers with Capacitive Loading

The most common method of reducing the ripple at the output of the rectifier is to make the load capacitive. The size of capacitor which should be used to obtain a certain reduction in ripple for a particular circuit may be found from the method described below. The single-phase half-wave circuit with capacitive loading shown in Fig. 9-13 is the simplest rectification circuit giving continuous load current. In the absence of the

capacitor C the rectifier delivers power to the load R_{load} only during the positive half cycle, and the output voltage and load current periodically fall to zero.

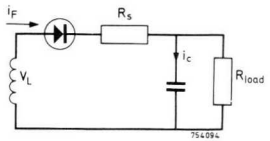


Fig. 9-13 Single-phase half-wave rectifier with capacitive load.

With the capacitor C in the circuit, the capacitor charges to nearly the crest value of the applied supply voltage on the first positive half cycle. Thus, the capacitor acts as a reservoir storing up energy. When the applied voltage falls below the crest value, the capacitor voltage is higher than the applied voltage, and thus the diode is reverse biased. The capacitor now partly discharges into the load until such time as the applied voltage exceeds the capacitor voltage again. The diode is then forward biased and the capacitor recharges to the crest value of the applied voltage. The diode then ceases to conduct, as previously explained, and the cycle is repeated.

The idealised current waveforms for the circuit, after steady state has been established, are shown in Fig. 9-14. Because of the charging and discharging of the capacitor, the voltage across it does not remain constant and the ripple has the same frequency as that of the applied voltage. The series resistor R_s is included in the circuit to limit the peak current through the diode on initial switch-on. The current through the diode charging the capacitor flows in pulses which are large in amplitude requiring an expensive capacitor filter to reduce the ripple to a reasonably low value.

The performance of the two-phase half-wave (Fig. 9-15) and single-phase full-wave (Fig. 9-16*a*) circuits is the same, so the voltage and current waveforms for both are shown in Fig. 9-16*b*. However it must be pointed out that, for a given output voltage, the diodes used in the two-phase half-wave circuit must have a rated V_{RWM} of twice that of diodes used in a single-phase, full-wave circuit.

In the single-phase full-wave circuit the applied alternating voltage is rectified, and the output smoothed by the capacitor filter in a manner similar to that described for the single-phase half-wave circuit. More

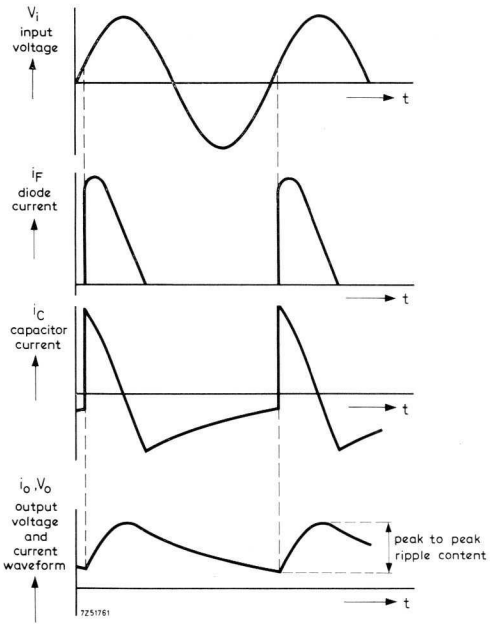


Fig. 9-14 Idealised waveforms of circuit in Fig. 9-13.

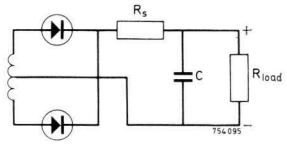


Fig. 9-15 Two-phase half-wave rectifier with capacitive load.

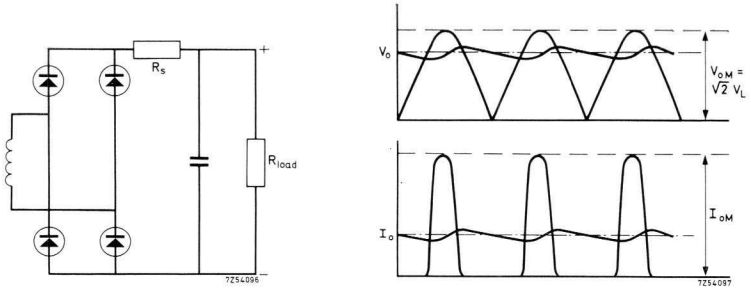


Fig. 9-16 (a) Single-phase full-wave rectifier with capacitive load; (b) Idealised waveforms of circuits in Fig. 9-15 and Fig. 9-16a.

efficient smoothing is obtained however, because the capacitor has to supply the load current for a shorter period, and therefore the capacitor voltage changes by a smaller amount. This means that the d.c. voltage available at the output is greater than that for the single-phase half-wave circuit, and the ripple voltage is smaller. The ripple frequency is twice that of the applied voltage frequency.

The two-phase half-wave circuit operates in a similar manner. The diodes conduct alternately and therefore the current flows through each half of the transformer secondary alternately. The diodes must withstand a crest working voltage which is equal to the crest value of total secondary transformer voltage.

Design Method. The graphs produced by *Schade* [17] have proved to yield sufficiently accurate results, and for most designs they are fairly simple to use. Some observations must first be made regarding several of the parameters before we go on to describe Schade's method in detail.

In modern silicon diodes the forward voltage drop, V_F, is small and varies little with current; thus, we can without substantial loss of accuracy make V_F constant and equal to the value that occurs when the diode is subjected to the maximum average current.

The maximum crest working voltage of the diodes must not be surpassed; transients occur on mains supplies and the designer should guard against these (if necessary by placing RC damping circuits across the diodes).

The peak inrush current is large with a capacitively-loaded rectifier, because the capacitor in its discharged state, is a short circuit across the output; the current is limited only by the source resistance. The source resistance must thus be a compromise value between the minimum required to keep the peak inrush current below rated level and the maximum for circuit efficiency and regulation requirements.

The repetitive peak current is dependent on the reservoir capacitance. Increasing the latter to improve smoothing of the output voltage results in a reduced conduction angle and an increased peak current level, which must be kept within the repetitive peak forward current ratings of the diode. The transformer leakage reactance has not been taken into account in the analysis. However, this tends to reduce the peak diode current. The maximum ripple current which can be tolerated determines the minimum value of capacitor needed. The total r.m.s. capacitor current, $I_{C\,\mathrm{rms}}$, is related to the diode r.m.s. current $I_{F\,\mathrm{rms}}$, and the d.c. output current, I_o, as follows.

For single-phase half-wave circuits,

$$I_{C\ \mathrm{rms}} = \sqrt{(I_F{}^2{}_{\mathrm{rms}} - I_o{}^2)}, \tag{9-35}$$

and for two-phase half-wave and single-phase full-wave circuits,

$$I_{C\ \mathrm{rms}} = \sqrt{(2\ I_F{}^2{}_{\mathrm{rms}} - I_o{}^2)}. \tag{9-36}$$

The graphs relevant to Schade's method of analysis are presented in Figs 9-17 to 9-21. The graphs of Figs 9-17 and 9-18 give the conversion ratio ($\eta = V_o/V_L\sqrt{2}$) as a function of $\omega_s R_{load} C$ for the various circuits.

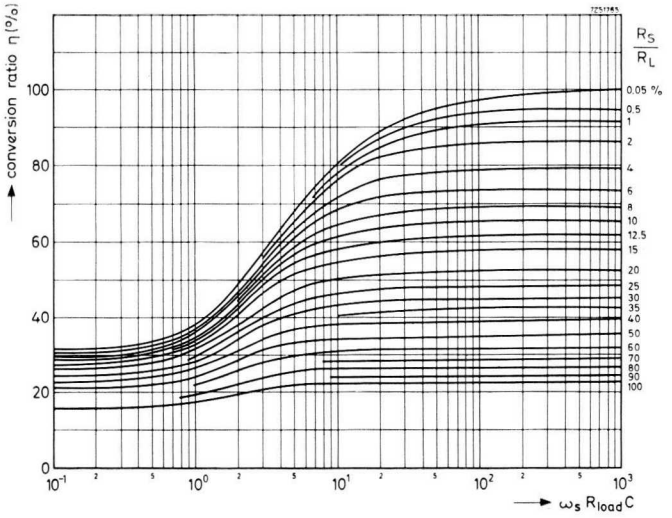


Fig. 9-17 $\eta = f(\omega_s R_{load} C)$ *(single-phase half-wave).*

The conversion ratio (η) depends on the value of R_s/R_{load}. For good regulation the value of $\omega_s R_{load} C$ should be selected to give operation on the flat portion of the curves. Fig. 9-19 gives information on the minimum value of $\omega_s R_{load} C$ that must be used to reduce the ripple to a desirable figure. Figs 9-20 and 9-21 give, respectively, the ratio of r.m.s. to average current per diode, and the ratio of peak repetitive to average current per diode, plotted as functions of $n\omega_s R_{load} C$. These ratios are dependent on the value of $R_s/nR_{load}\%$. The steps in the calculation are given below, in the order in which they are to be performed.

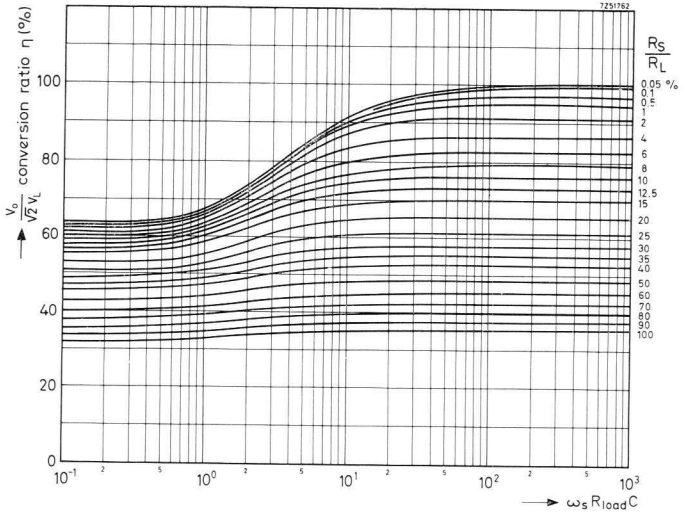


Fig. 9-18 $\eta = f(\omega_s R_{load} C)$
(single-phase full-wave and two-phase half-wave).

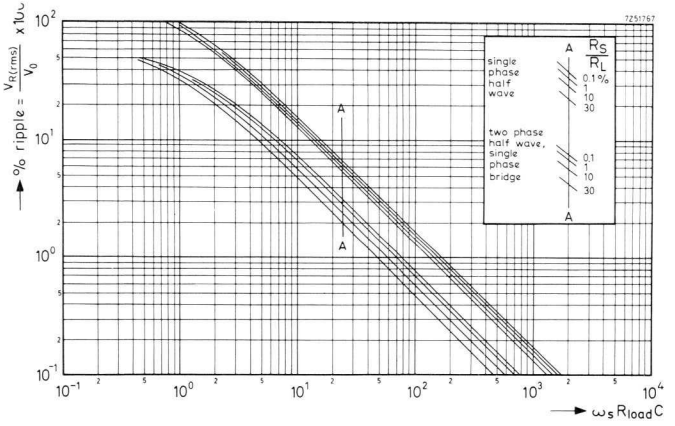


Fig. 9-19 Ripple % $= f(\omega_s R_{load} C)$.

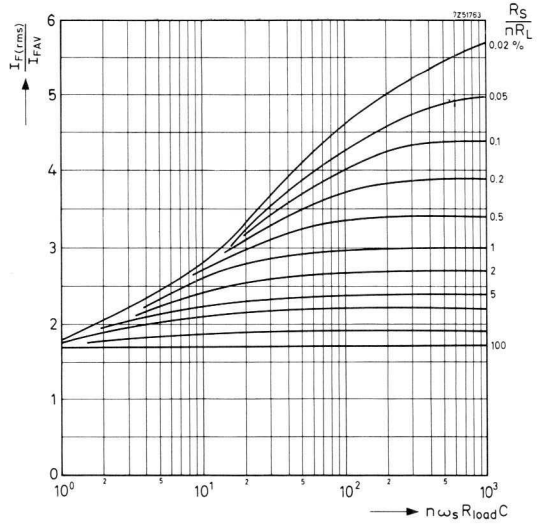


Fig. 9-20 $I_{F\ rms}/I_{FAV} = f(n\omega_s R_{load} C)$
n = 1 for half-wave
n = 2 for single-phase full-wave and two-phase half-wave.

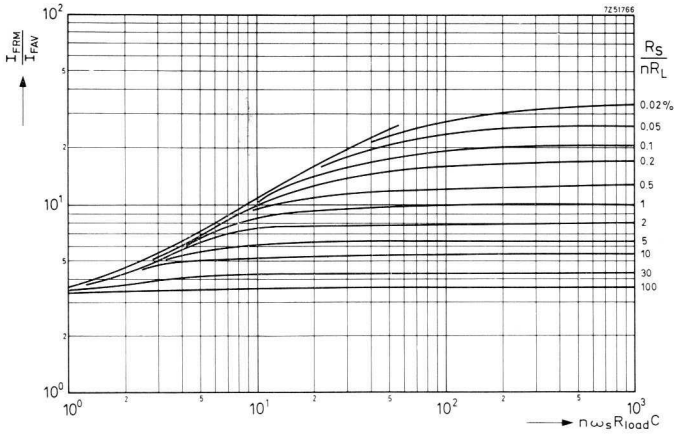


Fig. 9-21 $I_{FRM}/I_{FAV} = f(n\omega_s R_{load} C)$
n = 1 for single-phase half-wave
n = 2 for single-phase full-wave and two-phase half-wave.

Table 9-4 Design examples of rectifier circuits with capacitor Input Filter.

	single-phase half-wave	single-phase full-wave	two-phase half-wave
Requirement			
V_o	150 V	300 V	120 V *
I_o	1.5 A	2.0 A	2.0 A *
%ripple	$\leqslant 1\%$	$\leqslant 1\%$	$\leqslant 1.3\%$ *
f_s	50 Hz	50 Hz	50 Hz
Solution of step:			
1. $R_{LOAD} = V_o/I_o$	100 Ω	150 Ω	60 Ω
2. R_s	6 Ω	9 Ω	3.6 Ω
3. R_s/R_{LOAD}	6%	6%	6%
4. $\omega_s R_{LOAD}$ (Fig. 9-19)	150	66	50
C calculated	4780 μF	1400 μF	2660 μF
C practice	5000 μF	1800 μF	3000 μF
$\omega_s R_{LOAD} C$ corrected	157	85	56.5
5. $V_o/(V_L/2)$ from Fig.:	9-17	9-18	9-18 *
$V_o/(V_L/2)$	0.73	0.82	0.82
6. $V_L/2$ calculated	205 V	366 V	146.5 V *
V_L calculated	145 V	258 V	103.5 V
7. V_{RWM} found	205 V	366 V	293 V *
8. $n\omega_s R_{LOAD} C$	157	170	113
R_s/nR_{LOAD}	6%	3%	3%
$I_{F\ rms}/I_{FAV}$ (Fig. 9-20)	2.34	2.6	2.6
I_{FAV}	1.5 A	1.0 A	1.0 A
$I_{F\ rms} = F_{Ff} \times I_{FAV}$	3.51 A	2.6 A	2.6 A
9. Suitable diodes	BYX38-600	BYX38-1200	BYX38-900
10. I_{FRM}/I_{FAV} (Fig. 9-21)	6.2	7.5	7.5
I_{FRM} calculated	9.3 A	7.5 A	7.5 A
11. $I_{FSM} = V_L/2/R_s$	34.2 A	40.7 A	41.2 A
12. Transformer primary	230 V	230 V	230 V
$N = 230/V_L$	1.585	0.892	2.22 *
r_p	1.5 Ω	1.6 Ω	1.6 Ω *
r_s	2.0 Ω	2.0 Ω	1.2 Ω
then transformer resistance referred to secondary is			
$r_s + (r_p/N^2)$	2.6 Ω	4.0 Ω	1.5 Ω
V_{FAV} at I_{FAV} =	1.0 V	0.95 V	0.95 V
$r_r = V_{FAV}/I_{FAV}$	0.67 Ω	2×0.95 Ω	0.95 Ω
resistance in secondary =			
$r_s + (r_p/N^2) + r_r = r_{tot}$	3.27 Ω	5.9 Ω	2.45 Ω
External series resistance must be $R_s - r_{tot}$ =	2.73 Ω	3.1 Ω	1.15 Ω
Select $R_s - r_{tot}$ =	3.0 Ω	3.0 Ω	1.0 Ω
I_L	3.51 A	$2.6 \times 1/2 = 3.68$A	2.6 A *
V_L	145 V	258 V	103.5 V
$VA_{2n} = V_L I_L$	508 VA	950 VA	269 + 269 VA
Power rating of series resistor	37 W	40.6 W	13.6 W
13. r.m.s. ripple current $I_{c\ rms}$	3.18 A (eq. 9-35)	3.54 A (eq. 9-36)	3.09 A (eq. 9-36)

* Half of secondary winding.

1. Determine the value of R_{load};
2. Assume a value of R_s (usually between 1% and 10% of R_{load});
3. Calculate $R_s/R_{load}\%$;
4. From the percentage ripple graph against $\omega_s R_{load} C$ (Fig. 9-19) determine the value of $\omega_s R_{load} C$ required to reduce the ripple to a desired value for $R_s/R_{load}\%$ determined in (3). Calculate the required value of C;
5. From the η against $\omega_s R_{load} C$ curves for the appropriate circuit (Fig. 9-17 or 9-18) determine the conversion ratio for the value of $\omega_s R_{load} C$ determined in (4) and $R_s/R_{load}\%$ determined in (3);
6. Determine the values of $V_L/2$ and V_L, using information from (5);
7. Determine the crest working reverse voltage that the diodes must withstand;
8. Determine the r.m.s. current per diode from Fig. 9-20;
9. Select the diode to be used;
10. Check the peak repetitive current per diode from Fig. 9-21;
11. Check the peak inrush current I_{FSM} given by $V_L/2/R_s$. If the value obtained exceeds diode ratings, then R_s must be increased and the design procedure repeated;
12. Design the transformer and adjust the value of R_s accordingly, taking into account the transformer resistance and the forward resistance of the diode at the average current;
13. Check r.m.s. ripple current through smoothing capacitor C;
14. Design the R-C damping circuit as recommended in the diode data sheets;
15. Determine heat-sink size to allow operation at anticipated ambient temperature (refer to the diode data sheets).

The design of the three types of capacitor input filter rectifier circuits based on the above-mentioned procedure is given in Table 9-4.

R-C Damping Circuit and Heat sink

The R-C circuit intended to suppress transients can be designed by adopting the following procedure (cf. section 6.4.1.1). It may be paralleled with either the primary or the secondary of the transformer (see diode data sheets).

The damping circuit components determined by using the expressions below are suitable for suppressing transients up to $2\,V_{RWM}$. Consider the single-phase full-wave rectifier circuit.

If the damping circuit is connected to the primary of the transformer, then:

$$C_1 = 200(I_{mag}/V)\ \mu F \quad \text{and} \quad R_1 = (150/C_1)\ \Omega$$

where

V = transformer primary r.m.s. voltage

I_{mag} = magnetising primary r.m.s. current.

From the above table, the primary r.m.s. current = 3.68/0.892 = 4.13 A.

If I_{mag} = 10% of primary r.m.s. current, then:

$$C_1 = 200(0.413/230) = 0.36\ \mu F.$$

Select C_1 = 0.5 μF, then:

$$R_1 = 150/0.5 = 300\ \Omega.$$

If the damping circuit is connected to the secondary,

$$C_2 = \frac{225(I_{mag}N^2)}{V}\ \mu F \text{ and } R_2 = (200/C_2)\ \Omega,$$

where:

$$N = \frac{\text{transformer primary r.m.s. voltage}}{\text{transformer secondary r.m.s. voltage}}.$$

Therefore:

$$C_2 = \frac{225 \times 0.413}{230} \cdot (230/258)^2 = 0.31\ \mu F.$$

Select C_2 = 0.5 μF, then R_2 = 400 Ω.

Heat-sink

From the BYX38 data, for 1 A average current, a diode mounted on a heat sink with a thermal resistance of 19.4 °C/W ($R_{th\ mb-h} + R_{th\ h-a}$ = 20 °C/W) can be operated up to an ambient temperature of 100 °C. If these fins are stacked to produce the bridge rectifier assembly, then the area of the heat sink should be approximately 16 cm² (one face: see Fig. 5-12). A heat sink 4 cm × 4 cm should be satisfactory.

Performance

The output curves for the 3 examples of Table 9-4 are shown in Fig. 9-22. From these curves it can be seen that the output voltage rated load current is within 2% of the design value.

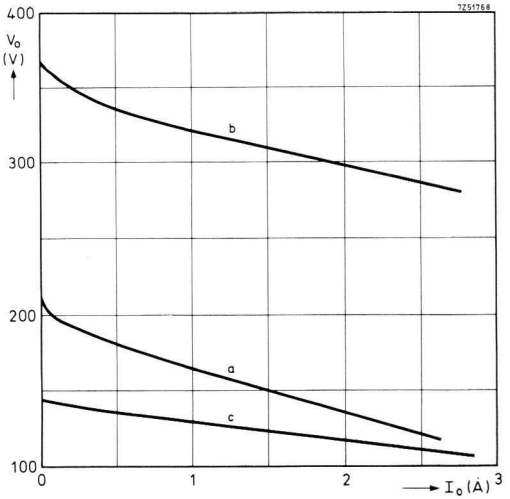


Fig. 9-22 Regulation curves of circuits from Table 4
(a) single-phase, half-wave
(b) single-phase, full-wave
(c) two-phase, half-wave.

9.3.4 Rectifiers with LC smoothing filters

General

A capacitively loaded rectifier circuit has the limitations that for high load currents a large smoothing capacitor is necessary to carry the heavy ripple current; also high inrush and repetitive peak currents flow through the diodes. These limitations may be overcome by the use of a choke input filter which forms an inductive load for the rectifier.

The single-phase half-wave circuit cannot be used with a choke input filter, as it would require an infinite value of inductance to cause current to flow throughout the cycle.

For the two-phase half-wave circuit of Fig. 9-15 and the single-phase full-wave circuit of Fig. 9-16, R_s is replaced by a series choke L.

The action of the choke is to reduce the peak and r.m.s. value of the current and to reduce the ripple voltage. The choke-input filter, however, requires a higher applied voltage than the capacitor-input filter to produce the same output voltage.

Below are discussed the operation of, and calculations for, the choke-input filter.

Rectifier Output Voltage (Smoothing Filter Input)

Consider the single-phase full-wave circuit shown in Fig. 9-23 and the waveforms shown in Fig. 9-24. The rectified voltage is applied to the choke-input filter. This voltage may be expressed as a series containing a d.c. component and harmonic components. The crest value of the output voltage V_o is equal to $V_L\sqrt{2}$ in this circuit.

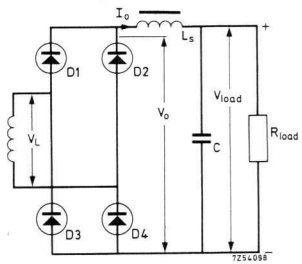


Fig. 9-23 Single-phase, full-wave rectifier with choke input.

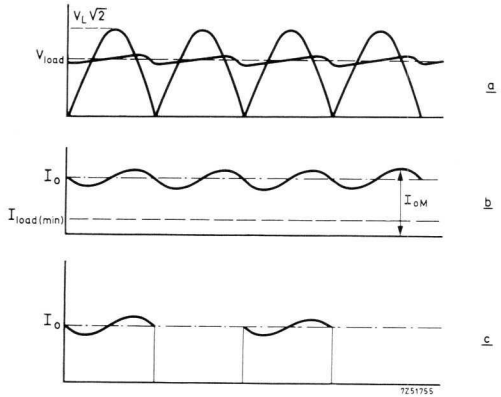


Fig. 9-24 Idealised waveforms of single-phase, full-wave rectifier. with choke input
(a) output voltage
(b) current through L_s
(c) current through rectifier (D_1 and D_2) or (D_3 and D_4).

The rectified voltage can be approximated to a d.c. term plus a harmonic at the fundamental ripple frequency, assuming that the amplitudes

of the higher harmonics are negligible. Therefore, as shown in in section 9.3.2, the rectifier instantaneous output voltage before the smoothing filter:

$$v = (2/\pi)V_L/2 - (4/3\pi)V_L/2 \cos 2\omega_s t.$$

The LC Smoothing Filter

The choke input filter should ideally pass only d.c., and block all a.c. components. The filter must allow direct current to flow to the load with minimum power loss, and at the same time present a high impedance to the fundamental and other ripple frequencies. The capacitor shunts the load so as to by-pass the harmonic currents.

The attenuation factor A of the filter with series choke L and shunt capacitor C, is defined as the ratio of the total input impedance of the filter to the impedance of the parallel combination of the shunt capacitor C and load R_{load}. For the choke input filter to function efficiently, the choke reactance at fundamental ripple frequency f_r should be much greater than its d.c. resistance, and the capacitor reactance much lower than the minimum load resistance.

If it is assumed that, the inductance of the choke being L and its resistance R_L,

$$2\pi f_r \gg R_L,$$

and

$$1/2\pi f_r C \ll R_{load\ \min},$$

then:

$$A = \frac{2\pi f_r L - 1/2\pi f_r C}{1/2\pi f_r C},$$

therefore:

$$A = 4\pi^2 f_r^2 LC - 1. \qquad (9\text{-}37)$$

The value of the inductance L used in the circuit must be such as to allow the diodes to conduct over one cycle of the fundamental ripple frequency. If the diodes conduct for a shorter period, then the choke input filter behaves more and more like a capacitor-input filter in which the diodes conduct for only a fraction of the cycle. This gives rise to a higher peak-to-average current ratio for the diodes, and gives poor load regulation.

It follows that, for a given current, and for a certain value of inductance,

the diodes will become non-conducting before the cycle is completed. This minimum value of inductance which allows the diodes to conduct over one cycle of the fundamental ripple frequency is termed the critical inductance L_{crit}.

Critical Inductance

From Fig. 9-24 it can be seen that for the diode to conduct throughout the entire fundamental ripple cycle, the amplitude of the negative-going peak ripple current delivered by the rectifier must not exceed the minimum d.c. current required, which occurs with a load of $R_{load\ max}$. Thus:

$$I_{load\ min} = \frac{V_{load}}{R_{load\ max}} = \frac{2\sqrt{2}\,V_L}{\pi}\,\frac{1}{R_{load\ max}}. \tag{9-38}$$

If $2\pi f_r L \gg R_L$, and

$$\frac{1}{2\pi f_r C} \ll R_{load\ min},$$

$$\text{peak a.c. current} = \frac{4}{3\pi}\,V_L\,\frac{\sqrt{2}}{2\pi f_r L}. \tag{9-39}$$

The critical inductance is reached when the peak a.c. current equals the direct current. That is,

$$\frac{4}{3\pi}\,V_L\,\frac{\sqrt{2}}{2\pi f_r L_{crit}} = \frac{2\,V_L}{\pi}\cdot\frac{\sqrt{2}}{R_{load\ max}}$$

therefore:

$$L_{crit} = \frac{R_{load\ max}}{3\pi f_r}. \tag{9-40}$$

For 50 Hz supply frequency and full-wave rectification, $f_r = 100$ Hz, so that the theoretical $L_{crit} = R_{load\ max}/943$. Because of the approximations made, it is necessary to use a higher value of inductance than L_{crit}. In practice, it is found that *the value* of inductance that should be used is about twice the value of L_{crit} and the practical formula becomes:

$$L_{crit} = \frac{R_{load\ max}}{500}. \tag{9-41}$$

It is not possible to maintain the critical value of the inductance over all values of load current. This would require an infinite inductance at

zero load current. Two methods are available to ensure that current flows throughout the cycle, and that good regulation is maintained over a wide range of load currents. These are the use of a bleeder resistance or a swinging choke.

A bleeder resistance is connected across the shunt capacitor to maintain the minimum current that satisfies the critical inductance condition when no additional load is connected (i.e. the bleeder resistance should be not greater than $R_{load\ \max}$ from eq. 9-40). The use of this bleeder also prevents the output voltage from rising to the peak applied voltage in the absence of the load.

The swinging choke method utilises the property of an iron cored inductor whose inductance depends partly on the amount of direct current flowing through it. The choke is designed to have a high inductance at low currents which decreases as the d.c. current is increased. The used of such a choke is therefore very satisfactory for maintaining good regulation over a range of load current and is more efficient than the bleeder resistance method.

Since the inductance varies with the load current, the ripple voltage is no longer independent of the load current. When using a swinging choke, it is necessary to ensure that the inductance does not fall to a very low value at the maximum load current, as this leads to high repetitive peak currents. In practice, the inductance at full load L_F should be such that:

$$L_F = 2\ R_{load\ \min}/943 \approx R_{load\ \min}/500.$$

Ripple Current and Voltage

If $2\pi f_r L \gg R_L$:

$$1/(2\pi f_r C) \ll R_{load\ \min},$$

and

$$2\pi f_r L \gg 1/(2\pi f_r C),$$

then:

$$\text{r.m.s. ripple current } I_{c\ \text{rms}} = \left(\frac{4}{3} \cdot \frac{V_L\sqrt{2}}{\pi} \cdot \frac{1}{\sqrt{2}}\right) \frac{1}{2\pi f_r L}.$$

Since:

$$V_o = 2\ V_L\sqrt{2}/\pi$$

$$I_{c\ \text{rms}} = V_o\ \sqrt{2}/2\pi\ 3f_r L,$$

%ripple = %ripple before filtering $\times$ 1/A.

From Table 9-3, %ripple before filtering = 47.2%.

From eq. (9-37), if $4\pi f_r^2 LC \gg 1$,

then:

$$A \simeq 4\pi^2 f_r^2 LC$$

$$\%\text{ripple} = \frac{47.2}{4\pi^2 f_r^2 LC} = \frac{1.193}{f_r^2 LC} \approx \frac{1200}{f_r^2 LC}. \tag{9-42}$$

For 50 Hz supply frequency and full-wave rectification $f_r = 100$ Hz, therefore:

$$\%\text{ripple} \approx 120/LC, \tag{9-43}$$

where L is in henries and C is in μF.

Minimum Value of Shunt Capacitance

In evaluating the percentage ripple and the attenuation factor of the filter, it has been assumed that the reactance of the capacitor at the fundamental ripple frequency is very much lower than the minimum load resistance. In practice, it is found that satisfactory performance is obtained when the reactance of the capacitor is made less than one-fifth the minimum load resistance. That is,

$$\frac{1}{2\pi f_r C} \leqslant R_{load\ \min}/5.$$

Therefore:

$$C \geqslant \frac{5\times 10^6}{2\pi} \frac{1}{f_r R_{load\ \min}}\ \mu\text{F}$$

$$\geqslant \frac{796\,000}{f_r R_{load\ \min}}\ \mu\text{F} \approx \frac{800\,000}{f_r R_{load\ \min}}\ \mu\text{F}. \tag{9-44}$$

Because of the nature of the circuit, the capacitor will resonate with the inductor at a certain frequency. At this frequency the output impedance will be greater than the capacitor reactance. Therefore, when a non-linear load is applied, precautions must be taken to ensure the output impedance of the filter is small at the fundamental ripple frequency.

Multi-section Filter

When it is required to reduce the ripple voltage across the load to a very low value, a single-section choke input filter may require large values of

inductance and capacitance, which may lead to an uneconomic filter design. In this case, the same reduction can be achieved by using a multi-stage filter with smaller value inductors and capacitors. It can be shown that optimum smoothing is achieved when all stages are identical.

Fig. 9-25 shows the attenuation factor A plotted against f_r^2LC for 1, 2 and 3-stage filters. A suitable arrangement can therefore be selected by studying the filter characteristics. For an attenuation factor between 23 and 160, the two-stage filter is the most economic, but above 150, a three-stage filter is more suitable.

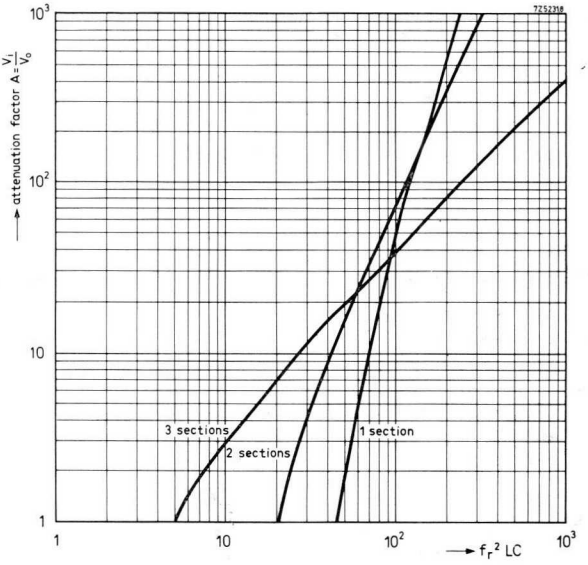


Fig. 9-25 Attenuation factor $A = f(f_r^2LC)$.

Example

A single-phase, full-wave circuit to supply 0 to 4 A at 200 V is required. The ripple is to be less than 0.5 %, $f = 50$ Hz choke resistance 7.5 Ω, and the diode voltage drop approximately 1 V.

Let the bleeder current = 0.5 A, therefore the bleeder resistance $R_b = 200/0.5 = 400$ Ω.

The external load at maximum current = $R_{load\ min} = 200/4 = 50$ Ω.

At zero load current, the total circuit resistance 400 + 7.5 = 407.5 Ω.

From eq. (9-41):

$$L_{crit} = R_{load\ max}/500 = 407.5/500 = 0.815 \text{ H}.$$

The relationships between a.c. and d.c. voltages and currents are given in Table 9-3 for circuits without filters. The values given for inductive load circuits can also be used for choke input filter circuits.

In order to use the relationship of the idealised circuits (Table 9-3), V_o must be greater than the d.c. output required to allow for voltage drop across choke and diodes. That is:

V_o = direct output voltage required + voltage drop across choke + voltage drop across diodes.

Therefore:

$$V_o = 200 + 7.5(4 + 0.5) + (2 \times 1) \simeq 236 \text{ V}.$$

From Table 9-3:

$$V_{o\,\text{rms}} = 1.11\ V_o = 262 \text{ V}.$$

From eq. (9-44):

$$C \geqslant 800\,000/f_r R_{load\,\min}\ \mu\text{F}.$$

For a bridge rectifier circuit, $f_r = 100$ Hz, therefore

$$C \geqslant 800\,000/100 \times 50 \simeq 160\ \mu\text{F}.$$

From eq. (9-43), for ripple to be less than 0.5%

$$LC \geqslant 120/0.5,$$

therefore:

$$LC > 240.$$

If $L = 1$ H, then $C \geqslant 240\ \mu$F, so that a practical value of $C = 240\ \mu$F is suitable.

From Table 9-3, the crest working voltage that the diodes must withstand $= 1.57$, $V_o = 1.57 \times 236 = 370$ V.

With allowance made for transients, BYX38/100 diodes should operate satisfactorily in this circuit.

From Table 9-3 $I_{FRM} = 1.0\ I_o$ for a pure inductive load. From Fig. 9-24 it can be seen that I_{FRM} is greater than I_o but not as large as the peak current with a resistive or capacitive load.

The maximum repetitive peak current per diode $I_{FRM} < 1.57\ I_o$, therefore,

$$I_{FRM} < 1.57 \times 4.5 < 7.6 \text{ A}.$$

The transformer rating can be determined by a procedure similar to that shown for the capacitor input filter rectifier circuits.

The transformer resistance must be taken into account, and the transformer ratio determined accordingly to give 262 V r.m.s. on the secondary.

For a primary voltage of 230 V, primary winding resistance $r_p = 1\ \Omega$, and secondary winding resistance $r_s = 1\ \Omega$, the transformer ratio is:

$N = V_{PL}/V_L = 230\{262 + (r_s + r_p/N^2)I_o\} = 0.843.$

Secondary volt-amp rating $= 230/0.943\ I_o = 1230$ VA.

The R-C damping circuit and heat sink must be designed according to the procedure given for the capacitor input filter rectifier circuits.

The voltage regulation curve for a circuit built with these components is shown in Fig. 9-26, from which it can be seen that the output voltage at full load current is within 3% of the specified value. It can also be seen that the bleeder resistance is functioning correctly, since the current at which the voltage starts to rise rapidly is about one-half of the bleeder current.

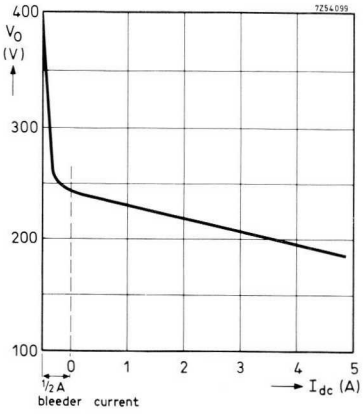


Fig. 9-26 Voltage regulation curve of single-phase, full-wave rectifier with choke input

9.5 Three-phase Rectifier Circuits

9.4.1 General: Mains Input

There are many advantages in using a polyphase rectifier system for high-power conversion:

— higher output voltage for the same voltage input;
— higher fundamental ripple frequency and lower ripple voltage thus necessitating little or no smoothing;
— higher conversion efficiency.

For three-phase circuits, the primary windings of the transformer are generally connected in delta (with the exception of the three-phase double-star configuration without interphase reactor described below) to suppress harmonics. In the following explanation of the circuits the secondary winding is always star-connected but delta connection could be used in the three-phase full-wave circuit.

For the power normally required from a three-phase circuit, the losses introduced by a filter would be too great. A choke input filter may be a practical proposition where only a small current is required, but at high currents the size of the shunt capacitor required would be enormous and it would have to carry a large ripple current.

For the sake of completeness, the values of critical inductances and

Table 9-5 Choke Input Filter Performance

	two-phase half-wave and single-phase full-wave	three-phase half-wave	three-phase full-wave
percentage ripple (%)			
general formula	$\frac{1.193}{f_r^2 LC}$	$\frac{0.45}{f_r^2 LC}$	$\frac{0.102}{f_r^2 LC}$
50 Hz supply frequency	$\frac{119.3}{LC}$	$\frac{20}{LC}$	$\frac{1.133}{LC}$
critical inductance L_{crit} (H)			
general formula	$\frac{R_{load\ max}}{3 f_r}$	$\frac{R_{load\ max}}{3 f_r}$	$\frac{R_{load\ max}}{3 f_r}$
50 Hz supply frequency	$\frac{R_{load\ max}}{943}$	$\frac{R_{load\ max}}{3770}$	$\frac{R_{load\ max}}{33000}$
rms ripple current $I_{o\ rms}$ (A)			
general formula	$\frac{V_o}{13.3 f_r L}$	$\frac{V_o}{35.5 f_r L}$	$\frac{V_o}{155 f_r L}$
50 Hz supply frequency	$\frac{V_o}{1330 L}$	$\frac{V_o}{5310 L}$	$\frac{V_o}{46500 L}$

$R_{load\ max}$ in Ω, C in μF and L in H

various other relevant details have been given in Table 9-5. These values may be derived by a procedure similar to that described for the single-phase mains input circuits.

Three-phase half-wave, three-phase full-wave, six-phase half-wave, and three-phase double-star rectifier systems will be discussed in the following paragraphs. For a general survey of these circuits refer to section 9.1.

9.4.2 Description of the Circuits

The three-phase half-wave arrangement (three-phase star), is shown in Fig. 9-27. The secondary winding is star-connected, and the star point is used as a common load terminal.

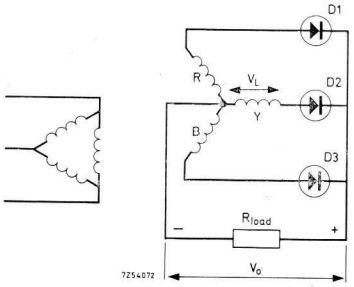


Fig. 9-27
Three-phase, half-wave rectifier.

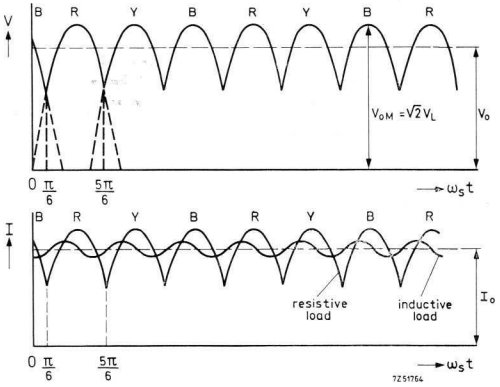


Fig. 9-28
Idealised waveforms of three-phase, half-wave rectifier.

The operation can best be understood by analysing the idealised waveforms shown in Fig. 9-28. Suppose that the voltage of phase R is most positive. Diode D_1 will therefore conduct when $\omega_s t = \pi/6$, and the current will flow through the load and return to the transformer via the neutral point. Diode D_1 will continue to conduct until the voltage of phase Y goes more positive than that of phase R at $\omega_s t = 5\pi/6$. The current will now be transferred from D_1 to D_2. D_2 will conduct for the next 120°, and then the current will be transferred to D_3 for the next 120°. In this manner, each diode conducts in turn over 120°.

The ripple frequency is three times the supply frequency.

The conversion efficiency of this circuit is high in comparison with single-phase circuits, and the ripple voltage is reduced to little more than one-third of that obtained in the single-phase full-wave circuit. The transformer utility factor is, however, poor in comparison to the three-phase full-wave rectifier, and the circuit is used only where low-voltage conversion is required.

Three-phase full-wave rectifier

The three-phase full-wave circuit is shown in Fig. 9-29. It is one of the most widely-used circuits for high-power conversion with semiconductor power diodes.

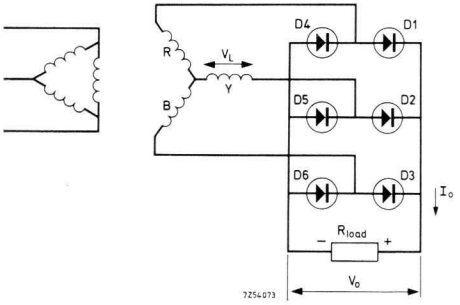


Fig. 9-29
Three-phase, full-wave rectifier.

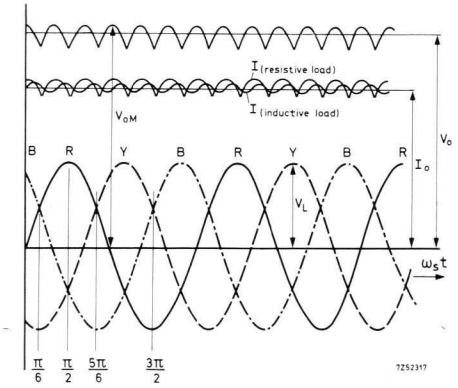


Fig. 9-30
Idealised waveforms of three-phase, full-wave rectifier.

Consider the circuit in conjunction with the waveforms shown in Fig. 9-30. If phase R is most positive, diode D_1 will start conducting when $\omega_s t = \pi/6$. The current flows through D_1 to the load and returns to the transformer through D_5 or D_6 depending on which phase, Y or B, is the more negative. At $\omega_{st} = \pi/6$, phase Y is the most negative and return current will flow through D_5. At $\omega_{st} = \pi/2$, phase B goes more negative and return current will then flow through D_6. At $\omega_{st} = 5\pi/6$, phase Y goes more positive and the current is therefore transferred from D_1 to D_2. Each diode conducts for 120° per cycle, and the current is commutated every 60°.

The ripple voltage is small, and the ripple frequency is six times the supply frequency. This circuit has the highest transformer utility factor, and it therefore requires least a.c. power to obtain a specified direct voltage and current.

The circuit finds application in the charging of high-voltage batteries, industrial power supplies, electrolytic plant operating at all except very low voltages, and generally where efficient high-power conversion is required.

Six-phase half-wave rectifier

The circuit for the six-phase half-wave system, which is also known as a six-phase star circuit, is shown in Fig. 9-31. Connecting the centre taps of the transformer secondary to a common star point gives a six-phase supply.

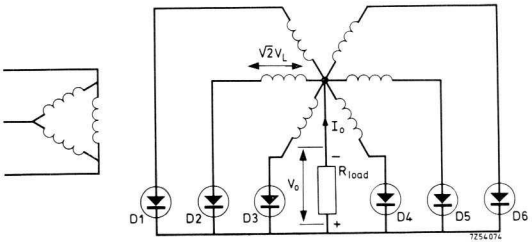


Fig. 9-31
Six-phase, half-wave rectifier (six-phase star).

The waveforms for this circuit are shown in Fig. 9-32. Each diode conducts for 60°, and the ripple frequency is six times the supply frequency. This system has higher conversion efficiency than the three-phase half-wave circuit. However, it has the lowest secondary utility factor of any three-phase circuit. The conversion efficiency is high, and equal to that of the three-phase full-wave circuit.

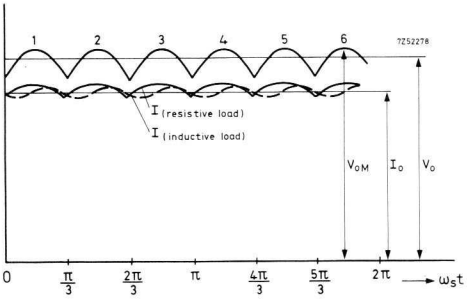


Fig. 9-32
Idealised waveforms of six-phase, half-wave rectifier.

The chief attraction of the circuit is that all diodes are connected to a common terminal, and therefore can simply be mounted on one heat sink. It is generally used for low-power conversion only, because of the poor secondary utility factor of the transformer.

Three-phase double-star rectifier

The three-phase double-star rectifier with interphase reactor is shown in Fig. 9-33. It has, in effect, two star-connected secondaries. The voltages of the two star points are displaced by 180°. The star points of the two windings are connected together by a centre-tapped interphase reactor.

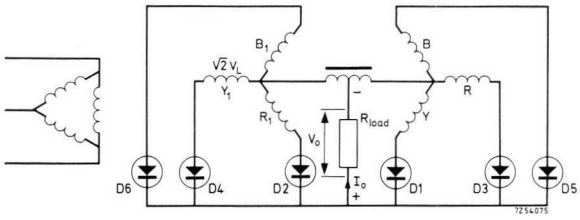


Fig. 9-33 Three-phase, double-star rectifier with interphase transformer.

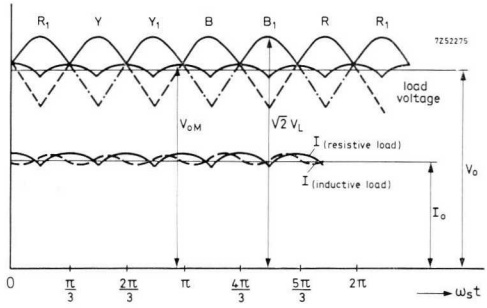


Fig. 9-34 Current flow in circuit of Fig. 9-33.

At any instant, current is carried by two phases — one in each star — as shown in Fig. 9-34. The return current is divided between the two secondaries by the interphase reactor. Thus the instantaneous output voltage is the average of the instantaneous voltages of the two secondaries that are conducting. The variation in the d.c. current produces a third harmonic e.m.f. at one anode and subtracts from that of the other, thus

holding the two at a common voltage. At low d.c. currents, a transition point is reached when the current is too small to produce the third harmonic e.m.f., and the circuit reverts to the six-phase half-wave system, giving a sudden rise in the output voltage.

The circuit has a six-phase ripple, but a three-phase voltage ratio. Its use reduces the secondary current per phase to approximately half that of the six-phase half-wave circuit, therefore diodes with a smaller peak current rating can be used, although their peak reverse voltage needs to be somewhat greater.

The arrangement is generally used where the cost of the interphase reactor is offset by the saving in cost of diodes having relatively low current ratings. It is frequently used for low-voltage high-current electrolytic plants. The utility factor of both primary and secondary is high, but that of the secondary is lower than that of the three-phase bridge circuit by a factor of $\sqrt{2}$.

The rating of the interphase reactor can be calculated as follows. If it is assumed that, in the process of holding the phase voltages of the two star circuits at a common value, a triangular waveform appears across the reactor, the crest value of this waveform will be V_{max}. The frequency is three times the supply frequency. The voltage across the reactor is at its maximum when the phase voltage of one star connection is at its maximum. The phase voltage of the other star connection is displaced by $\pi/3$, and therefore is at half maximum when the maximum voltage appears across the reactor. Thus:

$$V_{max} = V_L\sqrt{2} - V_L\sqrt{2}/2 = (\sqrt{2}/2)V_L.$$

The maximum value of the triangular waveform is $V_L/\sqrt{6}$. Since V_o/V_L is 1.17 (see Table 9-3), it follows that the r.m.s. voltage rating of the reactor is:

$$\frac{V_o I_o}{2(1.17\sqrt{6})} = 0.174\ P_0.$$

9.4.3 Losses

In larger installations which would normally use a three-phase mains input rectifier, losses become important, both as regards power wastage and output voltage drop (regulation). Some of the more important losses are discussed briefly below.

Voltage Regulation. The voltage regulation depends on three main factors: transformer copper loss, voltage drop across the diodes, and the commutation voltage drop.

Transformer Copper Losses. The reduction in output voltage due to transformer copper loss can be calculated as follows:
Voltage drop due to copper loss =

$$V_K = \frac{\text{transformer copper loss in watts } P_K}{I_o}. \tag{9-46}$$

The value of P_K may be obtained from the short-circuit test on the transformer.

Losses in Diodes. The loss due to the forward voltage drop across a diode is generally small, especially with silicon devices, which have a voltage drop of only one or two volts. An accurate value for any particular type can be obtained from the forward characteristic of the power diode.

The effect of this loss will depend on how many diodes are used in series. In particular, it should be noted that in a bridge circuit with one diode per leg, the forward voltage drop is that due to two diodes in series.

Commutation Voltage Loss. The voltage drop due to commutation, v_{com}, increases with an increase in the number of phases and an increase in load current. In order to keep the commutation loss to a minimum, the commutation reactance must be limited to a small value, bearing in mind that under short-circuit conditions the short-circuit current which is limited by the commutation reactance must not exceed the surge current rating of the diode in cases where no protective elements have been incorporated. The commutation loss is given by:

$$V_{com} = m_2 X_L I_0 / 2\pi \tag{9-47}$$

where:
m_2 = number of commutation (output pulses) per power cycle
X_L = transformer reactance per phase
I_o = d.c. load current

Total Volt Drop. With all these losses taken into account, the direct voltage V_o appearing across the load V is given by:

$$V_o = V_{ideal} - \frac{m_2 X_L I_o}{2} - P_K/I_o - V_{FAV} \times \text{number of diodes in series},$$

where:
V_{FAV} = forward voltage drop per rectifier,
V_{ideal} = d.c. output of loss-free rectifier.

Power Losses. The main power losses in the installation will be in the transformer (core loss and copper loss) and in the diodes. The transformer losses can be estimated by performing two tests, described below.

For the "open-circuit test", the secondary is open-circuited, and the current and power at nominal line voltage and frequency are measured. The current $I_{(oc)}$ is the sum of the magnetising current and core loss components. The power indicated, $W_{(oc)}$, represents the core loss and copper loss. The latter is small, since $I_{(oc)}$ is small compared with the full-load current and may therefore be neglected.

In the "short-circuit test", either the primary or secondary is short-circuited and the voltage is gradually increased to circulate the rated current through the winding. The short-circuit voltage V_{sc} necessary to circulate the full load current is measured. The power reading W_{sc} in the test represents the copper loss I^2R and a small core loss that may be ignored.

From the above tests the performance of the transformer may be calculated as follows.

Transformer rating	VA_n (volt)
Transformer connection	Delta-star
Nominal primary voltage	V_{PL} volts
Nominal secondary voltage	V_L
Open-circuit test on star side at nominal voltage V_L	
Core loss = $W_{(oc)}$	
No-load current = $I_{(oc)}$	
Short-circuit test on delta side with secondary short-circuited	
Short-circuit voltage V_{sc}	Copper loss $P_K = W_{sc}$ watts at rated current
Primary line current	$I_{PL} = VA_n/\sqrt{3}V_{PL}$

Primary phase current = $I_{PL}/\sqrt{3}$
Copper loss per phase = $W_{sc}/3$ watts.
Reactance e.m.f. per phase at current $I_p/\sqrt{3} = V_x = \sqrt{(V_{sc}^2 - W_{sc}\sqrt{3}/3\,I_p)}$
Therefore p.u. reactance = V_x/V_{PL} 100 $\times$ p.u. (9-48)

Circuit efficiency

$$\%\text{efficiency} = \frac{\text{output}}{\text{output} + \text{losses}} 100 = \left(1 - \frac{\text{losses}}{\text{output} + \text{losses}}\right)100, \tag{9-49}$$

where losses $W_{(oc)} + W_{sc} + I_o V_{FAV} \times$ number of diodes in series.

Example

Design a three-phase rectifier circuit to supply 90 A. Suppose the available diodes have a peak-reverse working voltage rating (V_{RWM}) of 400 V. The transformer has a percentage reactance of 5% and a copper loss of 900 W.

The design of suitable three-phase full-wave and six-phase circuits is summarised below. (The three-phase full-wave calculation is detailed and the corresponding six phase result given in brackets.)

Three-phase full-wave circuit. The maximum r.m.s. phase voltage that may be applied V_L, is obtained by dividing the diode peak reverse working voltage V_{RWM} by the factor (V_{RWM}/V_L) given in Table 9-3. Thus,

$$V_L = 400/2.45 = 163 \text{ V.} \qquad (141.4 \text{ V})$$

The ideal d.c. output voltage, V_{ideal} is obtained by dividing V_L by the appropriate factor:

$$V_{ideal} = V_L/0.428 = 380 \text{ V.} \qquad (191.2 \text{ V})$$

The average current per rectifier leg is one third of the total, or 90/3 = 30 A, (15 A), and is the diode average current I_{FAV}. A diode which will meet the above ratings is the BYY15 (BYX13-800).

The voltage losses are as follows:

Diode voltage drop (average current) is 0.98 (from Data Sheets).

Total drop is twice this, or 2 V approximately. (0.96 V)

Commutation volt drop from eq. (9-47):

$$V_{com} = m_2 X_L I_o/2\pi = 3 \times 0.05 \times 163/2\pi = \sim 4 \text{ V.} \qquad (6.75 \text{ V})$$

Transformer copper loss volt drop (eq. (9-46)) is:

$$V_k = P_k/I_o = 900/90 = 10 \text{ V.} \qquad (10 \text{ V})$$

Approximate voltage available at rectifier output:

$$V_o = V_{ideal} - V_{losses} = 380 - 2 - 4 - 10 = 364 \text{ V.} \qquad (173 \text{ V})$$

The output power is thus:

$$P_o = V_o \cdot I_o = 364 \times 90 = 32.8 \text{ kW.} \qquad (15.6\text{kW})$$

9.4.4 Comparison of Three-phase Circuit Performances

Table 9-3 includes the performance of the commonly-used three-phase rectifier circuits. In evaluating the results in these table, it has been assumed that the transformer and diodes are ideal. The table, however, gives a good indication of the relative merits of the circuits, and may be used for comparing the kilowatts per rectifier available from various circuits. This is best illustrated by an example. Assume that the diodes rated at a crest working voltage of 400 V and with a current of 20 A are available. Table 8 below compares the single-phase full-wave and three-phase full-wave bridge circuits.

Table 9-6 Comparison of Circuits
(Using diode ratings of $V_{RWM} = 400$ V, $I_{FAV} = 20$ A)

	single-phase full-wave	three-phase full-wave
number of diodes employed From Table 9-3	4	6
output voltage V_o	$\frac{400}{1.57} = 255$ V	$\frac{400}{1.05} = 380$ V
output current I_o	$2 \times 20 = 40$ A	$3 \times 20 = 60$ A
power available $V_o I_o$	$255 \times 40 = 10.2$ kW	$380 \times 60 = 22.8$ kW
d.c. Kilowatts per diode	$\frac{10.2}{4} = 2.55$ kW	$\frac{22.8}{6} = 3.8$ kW

From the above results, it is apparent that better use of diodes is made in the three-phase bridge circuit.

10 Use in Battery Chargers

10.1 Introduction

Battery chargers for undemanding applications (for instance overnight charging of car batteries for private use) do not require means for regulating current or voltage. However, because the power fed into a battery falls off progressively with rising battery voltage, the total charging time can be minimized; in fact, an optimum discharge/charge cycle can be devised for any given set of economic factors. This will necessitate careful control of the charging process so as to shorten the time on charge and lengthen the battery life. There is, therefore, a requirement for charging equipment, employing thyristors or other control elements with associated regulating circuitry to keep output parameters constant, despite power line fluctuations and load variations.

Having an extremely low internal resistance, cells cannot exercise any current limiting action, and the output side of a charging set should therefore embody an element (a series resistance or reactance) that will keep the charge current within the rated level. This would also serve the purpose of making the charge current more or less independent of a.c. supply fluctuations and battery voltage.

The following observations may be helpful in suggesting the appropriate rectifier system for any particular application. (For full rectifier data refer to Table 9-3.) Firstly, let us consider the advantages of the full-wave rectifiers over the half-wave systems. (The same arguments apply to a three-phase full-wave when compared with its six-phase half-wave counterpart.)

— The secondary current flows (through the total secondary) in each direction on alternate half cycles, thus providing better utilization of the secondary windings. This results in a lower transformer kVA rating per kW output power, and where higher power levels are involved a bridge circuit will accordingly be given preference in view of the saving on transformer cost.

— For a given d.c. output voltage, a full-wave rectifier will necessitate the use of diodes which have a rated crest reverse voltage that is only

one-half of that of diodes used in half-wave circuits. This feature may be an advantage where only low-voltage rectifier diodes are available. Secondly consider the advantage of half-wave over full-wave type rectifiers. In a full-wave circuit two diodes are always in series with the load. The voltage drop through a full-wave rectifier is therefore greater than that through a comparable half-wave rectifier system which embodies only one diode per phase. Thus, a half-wave system may be preferable in very low voltage applications.

The application determines the suitability of a battery type to be used. For the convenience of the reader the properties of the various kinds of cell are summarized in Fig. 10-1 and tables 10-1 and 10-2. The generally

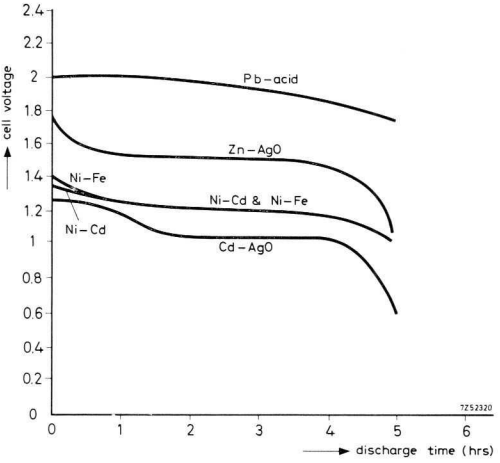


Fig. 10-1 Properties of accumulator cells.

available, inexpensive Pb-acid accummulator is fairly long-lived and therefore suitable for general service. It shows a small gradual voltage decrease during discharge, without any sharp initial fall-off (Fig. 10-1), for which reason it finds many applications in the laboratory. Ni-Cd and Ni-Fe batteries, owing to their ruggedness and long life, are widely used for powering vehicles, the Ni-Cd type being preferred where low ambient temperature may be encountered. The more expensive Zn-AgO and Cd-AgO batteries have a high Wh-output per unit weight and volume and are likely to be the types chosen for space vehicles.

Table 10-1

	temperature °C (°F)	discharge rate	Pb-Acid	Ni-Cd pocket plate	Ni-Cd sintered plate	Ni-Fe	Zn-AgO	Cd-AgO
energy output (Wh) per kilogramme, based on 20% voltage drop	27 (80)	5 hr.	25.1	13.2	33	33	116	54.2
		15 min.	15.0	6.4	21.6	—	86	34.4
	—18 (0)	5 hr.	12	9.2	25.3	—	87	25.6
		15 min.	6.4	3.7	19	—	51	26.6
	—40 (—40)	5 hr.	8.1	7.1	20	—	—	23.5
		15 min.	3.3	2.0	11.7	—	—	—
energy output (Wh) per cu dm, based on 20% voltage drop	27 (80)	5 hr.	51	29	66	71	205	96
		15 min.	30	14	44	—	151	60
	—18 (0)	5 hr.	24	20	51	—	141	81
		15 min.	13	7.9	39	—	96	47
	—40 (—40)	5 hr.	16	15	40	—	—	41
		15 min.	6.7	4	23	—	—	—

Table 10-2

characteristics	Pb-Acid	Ni-Cd pocket-plate	Ni-Cd sintered-plate	Ni-Fe	Zn-AgO	Cd-AgO
open circuit voltage per cell (charged)	2.1 V	1.3 V	1.3 V	1.4 V	1.8 V	1.4 V
time to 50% capacity retention 25 °C (80 °F)	55 days	300 days	300 days	25 days	2 yrs (estimated)	> 2 yrs
50 °C (125 °F)	7 days	17 days	17 days	—	115 days	115 days (estimated)
70 °C (160 °F)	¾ day	4 days	4 days	—	58 days	58 days
cycle life *	250-500	> 2000	> 2000	> 2000	100-250	300-500
major benefits	low cost; generally available good cycle life.	excellent cycle life; reliable; rugged.	excellent cycle life; reliable; rugged. good low temp. charge discharge performance.	excellent cycle life; reliable; rugged.	excellent Wh-output per unit weight and volume.	good-Wh-output per unit weight and volume; good cycle life.
major drawbacks	sulphates in discharged condition	poor high rate and low temp. performance.	high cost.	poor charge retention; poor low temperature perform.	high cost; poor cycle life; poor low temperature perform.	high cost.

* Battery life strongly depends on discharge depth during each cycle.
Upper limits denote cycle life expectancy for shallow discharge cycles.

10.2 Design of Battery Chargers

10.2.1 Resistance as Current-limiting Element

This method is illustrated in Fig. 10-2, which shows the basic circuit diagram for a single-phase half-wave charger together with its output voltage waveform.

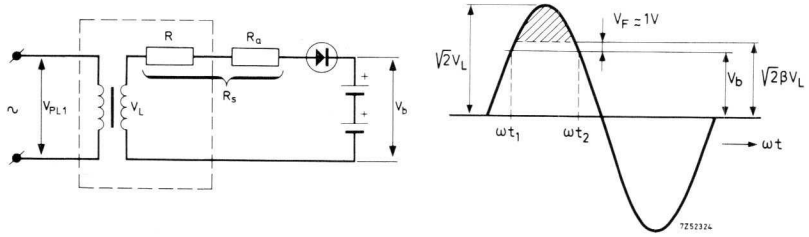


Fig. 10-2 Single-phase, half-wave, battery charger.

The d.c./a.c. voltage ratio β is expressed as:

$$\beta = (V_B + V_{FAV})/V_L\sqrt{2} \approx V_B/V_L\sqrt{2}, \qquad (10\text{-}1)$$

where:

V_B = battery voltage
V_{FAV} = diode forward voltage drop averaged over conduction cycle
V_L = secondary r.m.s. voltage

Where the battery voltage is relatively high, diode voltage drop V_{FAV} can be ignored. The value of β is a matter of compromise. If a value close to unity is chosen, only a low current-limiting resistance will be required and power wastage will be low. On the other hand, a smaller ratio will improve the regulating action of the circuit; that is to say, the charge current will be less affected by supply voltage fluctuations and the gradual rise in battery voltage as charging proceeds. However, the difference between the a.c. crest and the lowest battery voltage is now greater and thus more resistance will be needed to keep the charging current below the permissible level. Thus a low β value involves increased dissipation and a larger transformer, making the charger more bulky. Practical β values range around 0.6 at nominal battery voltage level. As will be clear from Fig. 10-2, in this circuit the diode must be rated for a reverse voltage equal to the sum of maximum battery voltage and crest value of the a.c. supply voltage (neglecting forward voltage drop V_{FAV}):

$$V_{RWM\ max} = V_L\sqrt{2} + V_{B\ max}. \qquad (10\text{-}2)$$

Instantaneous diode current:

$$i_F = \{V_L\sqrt{2} \sin \omega_s t - (V_B + V_{FAV})\}/R_s \tag{10-3}$$

where R_s = total current-limiting resistance.
Substituting eq. (10-1):

$$i_F = V_L\sqrt{2}(\sin \omega_s t - \beta)/R_s. \tag{10-4}$$

Average diode current, on substituting (10-4):

$$I_{FAV} = \frac{1}{2\pi} \int_{wt1}^{wt2} i_F \, \mathrm{d}\omega_s t = \frac{V_L\sqrt{2}}{2\pi R_s} \int_{wt1}^{wt2} (\sin \omega_s t - \beta) \, \mathrm{d}\omega_s t, \tag{10-5}$$

where $\omega_s t_2 - \omega_s t_1$ = diode conduction angle.
On introducing:

$$B = \sqrt{(1 - \beta^2)} - \beta \arccos \beta, \tag{10-6}$$

the above equation becomes:

$$I_{FAV} = V_L \, B\sqrt{2}/\pi R_s. \tag{10-7}$$

Average anode current at short circuit (zero output voltage, hence $\beta = 0$, $B = 1$)

$$I_{FAV\,sc} = V_L\sqrt{2}/\pi R_s.$$

Since β is proportional to battery voltage V_B (ref. eq. (10-1)); neglecting V_{FAV}, while B varies in direct proportion to the average anode current, the normalized charge characteristic can be obtained by plotting B versus β, as has been done in Fig. 10-3, with the practical β-range on an enlarged scale.

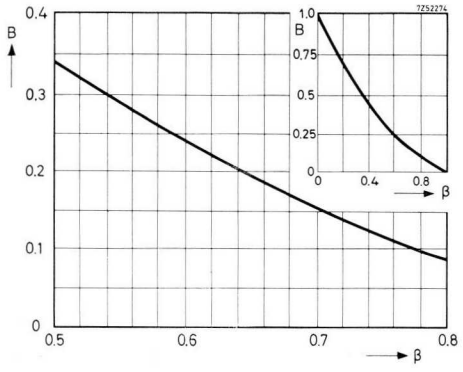


Fig. 10-3
$I_{FAV}/I_{FAV\,sc}(B) = f\{d.c./a.c.$ voltage ratio, $(\beta)\}$.

The total current-limiting resistance (resistance per phase) can be worked out from eq. (10-6):

$$R_s = V_L B\sqrt{2}/\pi I_{FAV} = 0.45\ V_L B/I_{FAV}. \tag{10-8}$$

From Fig. 10-2; $R_a = R_s - R$, where R, the total transformer resistance per phase, is 7% to 10% of R_s. Consequently lumped series resistance $R_a \approx 0.9\ R_s$, or from eq. (10-9):

$$R_a \approx 0.4\ V_L B/I_{FAV}. \tag{10-9}$$

Diode current (r.m.s.):

$$I_{F\ \mathrm{rms}} = \sqrt{\left(\frac{1}{2\pi}\int_{wst1}^{wst2} \omega i_F{}^2 \mathrm{d}\omega_s t,\right)} \tag{10-10}$$

which, on substitution of (10-4) and further manipulation, becomes

$$I_{F\ \mathrm{rms}} = \frac{V_L\sqrt{2}}{R_s}\sqrt{\left\{\frac{(1+2\beta^2)\arccos\beta - 3\beta - 3\beta\sqrt{(1-\beta^2)}}{2\pi}\right\}}. \tag{10-11}$$

Diode current form factor: $F_{fF} = I_{F\ \mathrm{rms}}/I_{FAV}$. From (10-6) and (10-7) we have

$$F_{fF} = \frac{\pi}{B}\sqrt{\left\{\frac{(1+2\beta^2)\arccos\beta - 3\beta\sqrt{(1-\beta^2)}}{2\pi}\right\}}. \tag{10-12}$$

The dissipation in the series resistors is determined by the r.m.s. diode current level. Hence the required series resistor wattage is:

$$P_{Ra} = F_{fF}{}^2 I_{FAV}{}^2 R_a. \tag{10-13}$$

From (10-4), peak diode current:

$$I_{FWM} = V_L\sqrt{2}(1-\beta)/R_s. \tag{10-14}$$

From (10-7) and (10-14), *peak-to-average factor for diode current*:

$$F_F(p/av) = \pi(1-\beta)/B. \tag{10-15}$$

The form factor F_{fF} and peak-to-average factor $F_F(p/av)$ of the single-phase diode current have been plotted against ratio β Fig. 10-4.

Current-limiting resistors give protection against internal shorts. In a charging system equipped with more than one rectifying element, the

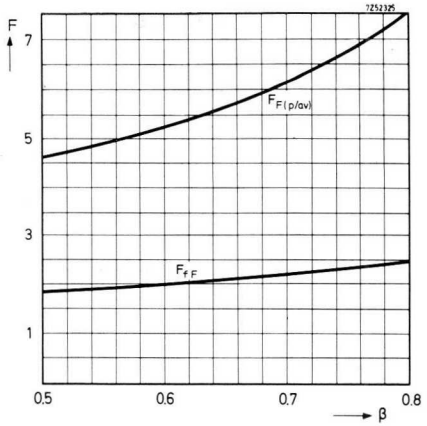


Fig. 10-4 Form factor $F = f(\beta)$.

required resistance should not be lumped into the single line to the battery or batteries under charge, but split up and placed next to the individual diodes. Individual series resistors in a full-wave or multi-phase rectifier operate independently of one another because the only coupling between legs is via the low load resistance. The total charge current is the sum of the current per phase as given by the formulae above.

10.2.2 Reactor as Current-limiting Element

Employment of resistive elements to limit the charge current to rated level necessarily involves power wastage, and thus will not be suitable for larger installations. Incorporating series reactors as loss-free current limiting elements will improve the charger efficiency, but the system power factor will be reduced due to reactive power taken by the series choke.

Reactors may be incorporated per diode (Fig. 10-5a), or a common reactor may be utilized, as depicted in Fig. 10-5b for a two-phase half-

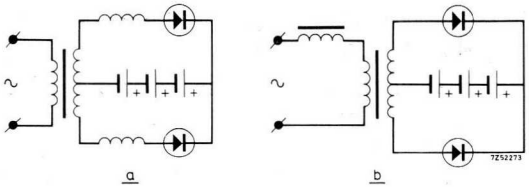


Fig. 10-5 Reactances as current limiting elements: (a) individual diode chokes; (b) single primary choke.

wave system. Diode reactors are liable to magnetic saturation, owing to d.c. and since both phases operate independently, the conduction angle per diode may exceed 180° at low β-values. Under short-circuit conditions, each diode will conduct over almost 360° giving rise to a fairly heavy fault current (Fig. 10-6). Thus, circuits equipped with a reactor in series with

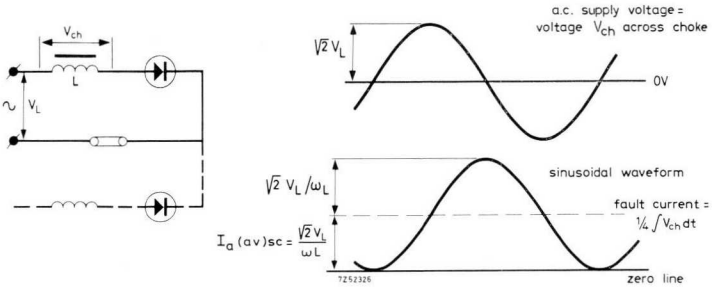


Fig. 10-6 Fault current caused by external short circuit.

each diode will offer poor protection against external shorts. When a primary reactor is used however, each diode will conduct over 180° at most. The fault current stays at a much lower level, because current take-over will occur at 180° intervals. Another benefit is that a symmetric current flows through the common choke, thus eliminating d.c. core saturation.

Voltage and current waveshapes produced in a two-phase half-wave charger rectifier with a primary reactor are shown in Fig. 10-7 for different β-values. Assuming zero circuit losses, the instantaneous primary current may be written

$$i_{PL} = \frac{1}{L}\int v_{ch}\,dt,$$

where v_{ch} = instantaneous choke voltage. Since $\int v_{ch}\,dt$ represents the area between the time function of the choke voltage and the time axis, the two shaded choke voltage areas that lie within each diode conduction interval must be equal (the conduction interval will terminate when the primary current drops to zero).

In Fig. 10-8 the diode conduction angle is plotted vs. β for a rectifier circuit with diode chokes (curve *a*) and for one with a common, primary reactor (curve *b*). At sufficiently high β-values, both circuits will behave

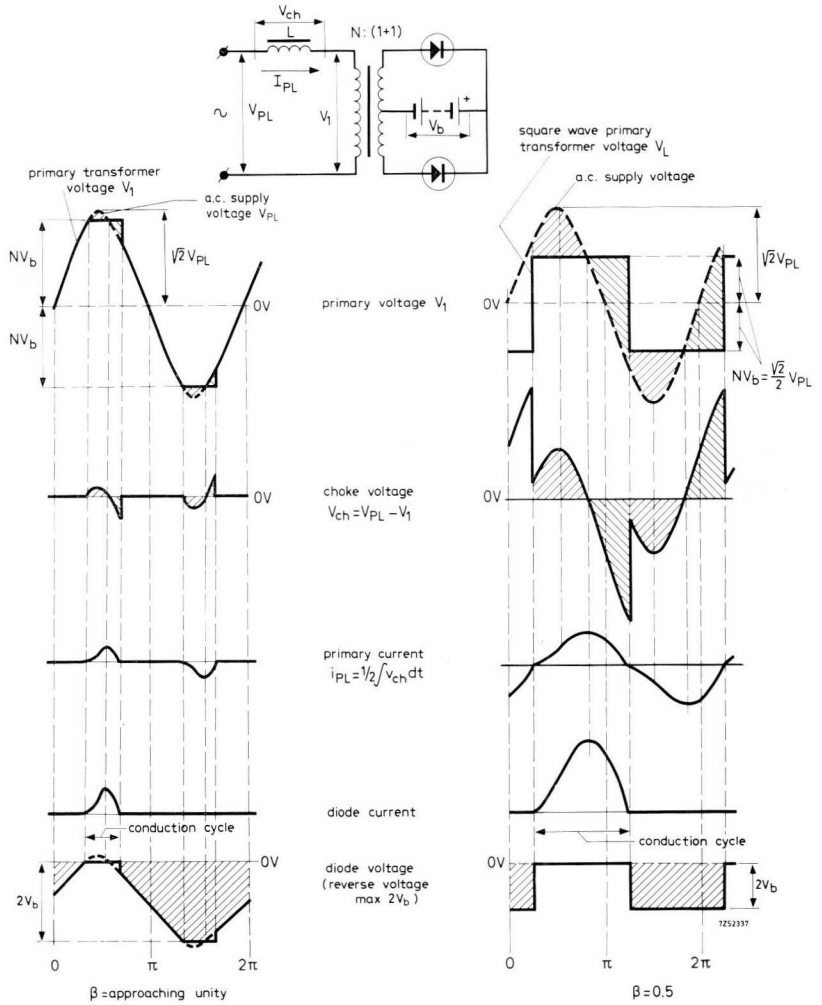


Fig. 10-7 Voltage and current waveforms in two-phase, half-wave battery charges.

in the same fashion because currentless intervals will occur in both cases. However, for β-values below 0.54, the diode conduction cycles will be restricted to 180° in the case of a primary reactor. In these circumstances the primary transformer voltage will be a square wave (see Fig. 10-7), for the diodes operate as switches, connecting the battery voltage across each secondary winding in turn.

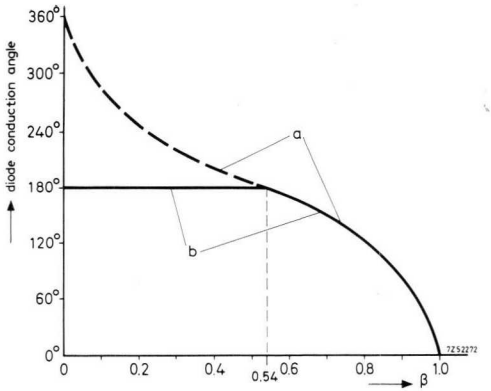


Fig. 10-8 Diode conduction angle = $f(\beta)$: (a) individual diode chokes; (b) single primary choke.

As shown in Fig. 10-7, the diodes must carry a reverse voltage twice max. battery voltage under load conditions; however, their reverse voltage rating should equal twice the peak value of the secondary voltage (no load condition).

$$V_{RWM\ \max} \geqslant 2\ V_L/2. \tag{10-16}$$

The diode current under fault conditions can be calculated as follows.

Primary r.m.s. current I_{PLsc} during a short circuit across the rectifier output amounts to:

$$I_{PLsc} = V_{PL}/\omega_s L_{ch(sc)}, \tag{10-17}$$

where V_{PL} = a.c. supply voltage.

$L_{ch(sc)}$ = effective reactor inductance at fault current.

If the supply transformer operates as an ideal current transformer, the peak value of the steady-state secondary fault current will be

$$I_{LMsc} = P_{PLsc}\, N\, \sqrt{2} = N\, V_{PL}/2/\omega_s L_{ch(sc)}, \tag{10-18}$$

where N = primary-to-secondary turns ratio.

Each diode will conduct during 180° and carry a semi-sinusoidal current. The average diode current under fault conditions will therefore be

$$I_{FAVsc} = N\, V_{PL}/2/\pi\omega_s L_{ch(sc)}. \tag{10-19}$$

Normalized charge characteristic B' vs. β, diode current form factor F_{fF}' and diode current peak-to-average $F_{F(p/av)}$ are shown in Figs 10-9 and 10-10 for practical β-values.

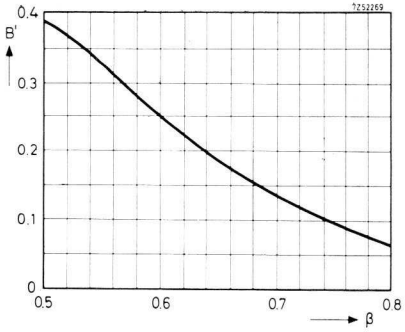


Fig. 10-9 Normalised charge characteristics $(B') = f(\beta)$.

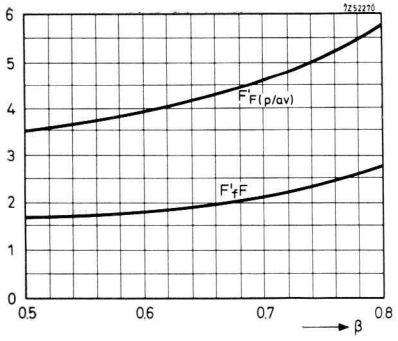


Fig. 10-10 Diode current form factor $(F) = f(\beta)$.

Normalized charge characteristics are illustrated in Fig. 10-11 for all circuits discussed above. The superiority of the system with primary choke in limiting the fault current is clearly demonstrated ($\beta = 0$). For β-values exceeding 0.54, the performance of the three circuits is almost identical.

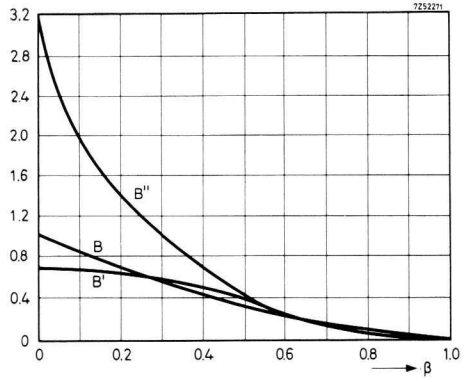


Fig. 10-11 Normalised charge characteristics:
B current limiting using resistors
B′ current limiting using primary choke
B″ current limiting using secondary choke in series with each diode, half-wave circuit.

The above considerations also hold (with good approximation) for systems equipped with a leakage transformer, and for polyphase rectifier chargers provided with a primary reactor.

Practical Design of Primary Reactor. The formulae needed to design the primary reactor are given below. R.M.S. reactor voltage:

$$V_{ch} = \sqrt{(V_{PL}^2 - V_{L1}'^2)}, \tag{10-20}$$

where:

V_{PL} = phase-neutral supply voltage,

V_{L1}' = primary transformer voltage per phase at full load; see eq. (10-33), section 10.3.

Reactor VA rating follows (to a good approximation) from

$$\mathrm{VA}_{n\,ch} = m_1 V_{ch} I_{PL}/2, \tag{10-21}$$

where:

m_1 = no. of primary phases,

I_{PL} = primary current per phase, eqs (10-22), (10-23).

Core weight may be estimated from Fig. 10-12. Core losses are calculated in the manner explained in section 10.3.

Different transformer/choke arrangements are illustrated in Fig. 10-13.

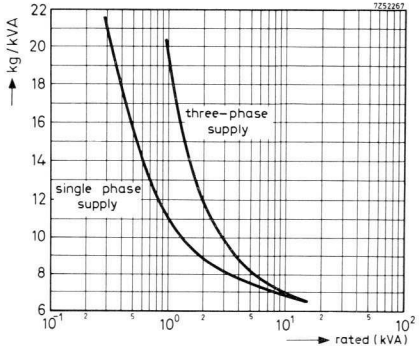
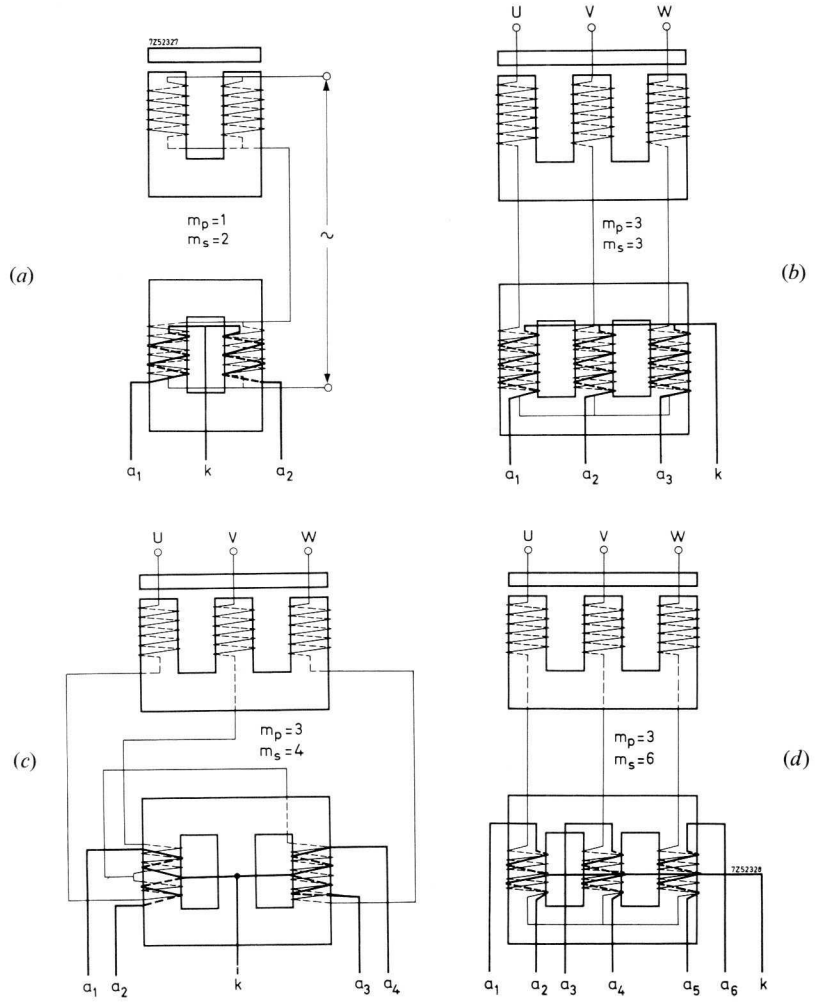


Fig. 10-12 kg/kVA = f(kVA).

10.3 Supply Transformer Design

The primary and secondary voltages and currents, the turns ratio, the VA rating and the core weight of the supply transformer can be determined by using the formulae which follow.



(*a*) (*b*) (*c*) (*d*)

Fig. 10-13 Transformer and choke arrangement: (a) two-phase half-wave; (b) three-phase half-wave; (c) four-phase half-wave; (d) six-phase half-wave.

The primary current per phase, I_{PL}, depends on the number of secondary phases. If the number of secondary phases is 2, 4, 6 or 12,

$$I_{PL} = 1.07\, I_{F\,\mathrm{rms}} \sqrt{2}/N. \qquad (10\text{-}22)$$

If the rectification is half-wave and the number of secondary phases is 1 or 3,

$$I_{PL} = 1.07\, I_F \sqrt{\{(\text{diode current form factor})^2 - 1\}/N}. \quad (10\text{-}23)$$

The coefficient 1.07 allows for the transformer magnetizing current. The secondary voltage per phase V_L (no load) may be obtained from eq. (10-1):

$$V_L = (V_B + V_{FAV})/\beta\sqrt{2} \approx V_B/\beta\sqrt{2}, \quad (10\text{-}24)$$

where:

V_B = battery voltage,

V_{FAV} = voltage drop across diode (approximately 1.5 V), averaged over conduction interval,

$\beta \approx 0.6$ at nominal battery voltage level.

The nominal battery voltage can be taken from the table below.

Table 10-3 Battery voltage per cell

	Pb-acid	Ni-Cd & Ni-Fe
min.	2.0	1.2
nominal	2.2	1.4
max.	2.7	1.8

The no-load primary voltage per phase V_{L1} (using resistors) is:

$$V_{L1} = V_{PL}, \quad (10\text{-}25)$$

where V_{PL} = phase-neutral supply voltage.

Using a primary reactor:

$$V_{L1} = 0.9\, V_{PL}. \quad (10\text{-}26)$$

The coefficient 0.9 allows for the voltage drop across the reactor due to the transformer magnetizing current.

For Scott transformer (4-phase secondary), using primary reactor (Fig. 10-14),

$$V_{L1h} = 1.35\, V_{PL}; \quad (10\text{-}27)$$

and

$$V_{L1v} = 1.56\, V_{PL}. \quad (10\text{-}28)$$

The primary-to-secondary turns ratio N may be derived as follows. When diode resistors are employed,

$$N = V_{PL}/V_L, \quad (10\text{-}29)$$

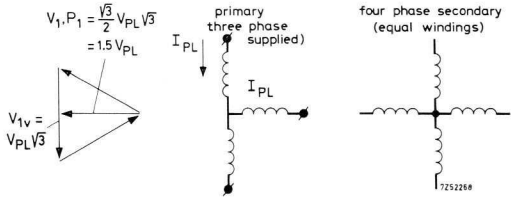


Fig. 10-14 Scott transformer to give four-phase secondary.

where V_L = secondary voltage per phase.

With a primary reactor,

$$N = 0.9\ V_{PL}/V_L. \tag{10-30}$$

For Scott transformer (Fig. 10-14, eq. (10-27)):

$$N = V_{L1h}/V_L = 1.35\ V_{PL}/V_L. \tag{10-31}$$

The primary voltage per phase V_{L1} (full load) with a reactor in the primary circuit is now calculated.

The load current causes an increased voltage drop across the primary reactor, thus reducing the primary transformer voltage. The following formula is sufficiently accurate for most practical cases.

Primary voltage per phase, at full load,

$$V_{L1}{}' = N(V_B + V_{FAV}).$$

Substituting eqs (10-30) and (10-24),

$$V_{L1}{}' = 0.9\ \beta\ V_{PL}\sqrt{2}, \tag{10-32}$$

in which $\beta \approx 0.6$ at nominal battery voltage level.

Primary and secondary transformer ratings will differ in cases where primary and secondary current form factors are not equal.

$$\text{Primary VA-rating} \quad VA_{1n} = m_1 V_{L1} I_{PL}; \tag{10-33}$$

$$\text{Secondary VA-rating} \quad VA_{2n} = m_2 V_L I_L; \tag{10-34}$$

where

m_1 = no. of primary phases
m_2 = no. of secondary phases
V_1 = primary voltage per phase, eqs (10-25) and (10-26)
V_L = secondary voltage per phase, eq. (10-24)
I_{PL} = primary current per phase, eq.s (10-22) and (10-23)
I_L = secondary current per phase = average diode current × current form factor.

For Scott transformer, when using primary reactor, from eqs (10-27) and (10-28) and Fig. 10-17, since primary VA-rating is the sum of VA-ratings per primary winding:

$$VA_{1n} = 2.91\ V_{PL}I_{PL}; \tag{10-35}$$

I_{PL} is derived from eq. (10-22).

The overall transformer VA rating is the arithmetic mean of the primary and secondary VA ratings:

$$VA_n = (VA_{1n} + VA_{2n})/2. \tag{10-36}$$

Core weight may be estimated from Fig. 10-12. At 1 Wb/m^2 (10 000 gauss) peak flux density, core losses are 1.3 to 1.7 watts/kg for transformer sheet 0.35 to 0.5 mm thick, and 2.5 to 3.0 watts/kg for dynamo sheet of the same gauge.

10.4 Design Examples

10.4.1 25V, 6 A Battery Charger

It is required to design a charger for charging four 6 V or two 12 V car batteries at a rated charge current of $I_o = 6$ A. Supply voltage is 220 V a.c., 50 Hz. The circuit in Fig. 10-15 has been adopted.

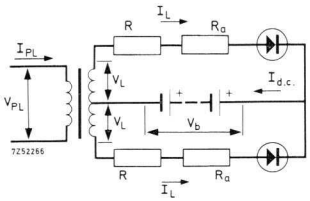


Fig. 10-15 Battery charger, two-phase half-wave.

volts per cell	1.8	2.1	2.7	0
β	0.49	0.57	0.73	0
B'	0.35	0.3	0.13	1
I_o	$\frac{0.35}{0.3}\times 6 = 7$ A	6 A	$\frac{0.13}{0.3}\times 6 = 2.6$ A	$\frac{1}{0.3}\times 6 = 20$ A
$I_{FAV} = \frac{I_o}{2}$	3.5 A	3 A	1.3 A	10 A
$F_{F(p/av)}$	4.6	5	6.4	π *
F_{fF}	1.9	2	2.2	$\pi/2$ *
$I_{FWM} = I_{FAV}F_{F(/av)}$	16 A	15 A	8.3 A	31.4 A
$I_{F\ rms}$	6.65 A	6 A	2.86 A	15.7 A

* semi-sinusoidal current waveform

Step 1: Secondary voltage per phase.
From eq. (10-24) putting $\beta = 0.57$ and taking 2.1 V as the nominal voltage per cell (Pb-acid battery), we find that the secondary voltage will be

$$V_L = (12 \times 2.1 + 1)/0.57\sqrt{2} = 32.5 \text{ V}.$$

Diode currents are worked out in the table on p. 212.
Step 2: Selection of diodes
Peak reverse voltage across each diode from eq. (10-16):

$$2 \times 32.5\sqrt{2} = 92 \text{ V}.$$

Thus, two diodes type BYX42-300 mounted on a common heatsink, will be perfectly adequate for the job even under sustained fault conditions.
General remark: Damping RC elements should be placed across the transformer total secondary terminals. On the basis of the formulas in chapter 6;

$$C = 225 \times 0.07 \times 1.34 \times 3.4/(2 \times 32.5) = 1.1 \ \mu\text{F},$$

take 1 μF and make R equal to 200/1.0 = 200 ohms.
Step 3: Supply transformer VA rating (nominal battery voltage).
Eq. (10-34): $VA_{2n} = 2 \times 32.5 \times 6.0 = 390$ VA.
Eq. (10-29): Turns ratio N = 220/32.5 = 6.8.
Eq. (10-22): Primary current $I_{PL} = 1.07 \times 6.0\sqrt{2}/6.8 = 1.34$.
Eq. (10-33): $VA_{1n} = 1 \times 220 \times 1.34 = 295$ VA.
Eq. (10-36): $VA_n = (390 + 295)/2 = 342$ VA.
Step 4: Series resistor R_a.
From eq. (10-9): $R_a = 0.4(32.5/3)0.3 = 1.3\ \Omega$.
Secondary transformer resistance per phase $0.1\ R_a = 0.13\ \Omega$.
Eq. (10-13): Resistor wattage $P_{Ra} = 6.65^2 \times 1.3 = 57$ W.
(min. battery voltage)
Step 5: Charger efficiency and power factor (nominal battery voltage).
Core weight from Fig. 10-12 for $VA_n = 342$ VA: $20.5 \times 0.342 = 7.0$ kg.
Core losses for 2.5 W/kg specific loss at 1 Wb/m^2 peak flux density: $7.0 \times 2.5 = 17.5$ W.
Secondary copper losses: $2I^2R = 2 \times 6.0^2 \times 0.13 = 9.4$ W.
Primary copper loss will be approximately the same as the secondary copper loss, so the total will be about 20 W.

Total charger losses may now be found as follows:

Core losses	17 W
Transformer copper losses	20 W
Losses in series resistors ($2 \times 6^2 \times 1.3$) =	94 W
Dissipation of diodes type BYX42 at 3 A average current, from spec sheet: (2×4 W)	8 W
Total losses	139 W
Output power: (no. $12 \times 2.1 \times 6$) =	151 W
Required input power	290 W

Efficiency = output/input = 151/290 = 0.52.
Power factor = required input power/$V_{PL}I_{PL}$ = $290/(220 \times 1.34) = 0.98$.

10.4.2 126 V, 15 A Battery Charger

A charger is required for charging a battery consisting of 60 Pb-acid cells, at 15 A rated charge current. In view of the required output power,

a three-phase half-wave rectifier circuit with primary choke will be adopted (Fig. 10-16). Phase-neutral voltage is 220 V a.c., 50 Hz. Because of series inductance $V_1 \simeq 0.9 \times 380/\sqrt{3} \simeq 200$ V.

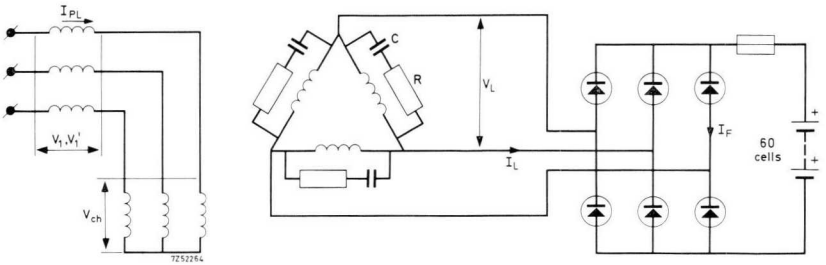


Fig. 10-16 Battery charger, three-phase half-wave.

Step 1: Secondary voltage per phase
From eq. (10-25), putting $\beta = 0.60$ and taking 2.1 V as the nominal voltage per cell, we find that the secondary voltage per phase must be $V_L = (60 \times 2.1 + 1)/0.60\sqrt{2} = 150$ V.
Diode currents are worked out in the table below.

volts per cell	max. 2.7 V	nom. 2.1 V	min. 1.95 V
β from eq. (10-1)	0.77	0.60	0.555
B′ from Fig. 10-9	0.08	0.25	0.32
I_o	$0.08 \times 15/0.25$ = 4.2 A	15 A (rated)	$0.32/15/0.25$ = 19.2 A
$I_{FAV} = I_o/3$	1.4 A	5 A	6.4 A
$F_{F'(p/av)}$ from Fig. 10-10	5.4	4.0	3.7
$F_{fF'}$ from Fig. 10-10	2.5	1.8	1.75
$I_{FWM} = I_{FAV} \times F_{f'(p/av)}$	7.6 A	20.0 A	23.7 A
$I_{F\,rms} = I_L = I_{FAV} \times F_{fF'}$	3.5 A	9.0 A	11.2 A
transformer sec. line current $I_{Frms} \times \sqrt{2}$	5	12.7	15.8 A

Step 2: Selection of diodes
Crest working reverse voltage of diodes must equal the open circuit secondary voltage of the transformer. For safety this is taken as the voltage occurring when full mains voltage appears across the primary.
Open circuit secondary voltage $= 220 \times 150\sqrt{2}/200 = 234$ volts.
To ensure that the diodes can withstand transients that appear on the mains and if the battery is disconnected whilst being charged it is recommended that the types BXY42-900 and 900R are used. The diodes should be mounted on two or three heat-sinks whichever is most convenient.

Damping elements for transient suppression.
Transformer magnetizing current $5.9 - 5.5 = 0.4$ A.
Add V_1 and $V_{CH} = 200 + 220\sqrt{(1 - 0.9^2)} = 200 + 96 = 296$ V.
$C = 225 \times 0.4 \times 1.33^2/296 = 0.538$, take 0.5 μF, then $R = 200/C = 400\ \Omega$.
Step 3: Transformer VA rating (nominal battery voltage)
Eq. (10-34): $VA_{2n} = \sqrt{3} \times 150 \times 12.7 = 330$ VA.
Eq. (10-30): Turns ratio $N = 0.9 \times 200/150 = 1.33$
Eq. (10-23): Primary current I_{PL} = sec. phase current/1.33 = 12.7/1.33 $\sqrt{3}$ = 5.5 A; including magnetising current $= 1.07 \times 5.5 = 5.9$ A.
Eq. (10-33): $VA_{1n} = 3 \times 200 \times 5.9 = 3550$ A.
Eq. (10-36): $VA_n = (3300 + 3550)/2 = 3400$ VA.
Step 4: Choke *VA* rating (nominal battery voltage):
Eq. (10-32): Transformer primary phase voltage at full load:

$$V_1' = 0.9 \times 0.60 \times 220\sqrt{2} = 168 \text{ V}.$$

Eq. (10-37): Choke voltage $V_{ch} = \sqrt{(220^2 - 168^2)} = 143$ V.
Eq. (10-38): $VA_{n(ch)} = (3 \times 143 \times 6.06)/2 = 1300\ VA$.
Step 5: Charger efficiency and power factor (nominal battery voltage):
Transformer core weight from Fig. 10-12 for $VA_n = 3400\ VA$:

$$9 \times 3.843 \simeq 30 \text{ kg}.$$

Transformer core losses for 2.5 W/kg specific loss at 1 Wb/m^2 peak flux density: $34.6 \times 2.5 \simeq 75$ W.
Reactor core weight from Fig. 10-12 for $VA_{ch} = 1300\ VA$: $16 \times 1.3 = 20.8$ kg.
Reactor core losses: $20.8 \times 2.5 \simeq 50$ W.

The total loss account is made up as follows:

Transformer core losses	75 W
Reactor core losses	50 W
Transformer copper loss ($\approx 2.5\%$ of *VA* rating)	85 W
Reactor copper loss ($\approx 3\%$ of *VA* rating)	40 W
Dissipation of diodes type BYX13 at 5 A average current, from spec. sheet: 6×10 W	60 W
Total losses	310 W
Output power: $60 \times 2.1 \times 15$	= 1890 W
Required input power	2200 W

Efficiency = output/intput = 1890/2200 = 0.86
Power factor = required input power/$V_{PL}I_{PL}\sqrt{3} = 2200/380 \times 5.9\sqrt{3} = 0.56$

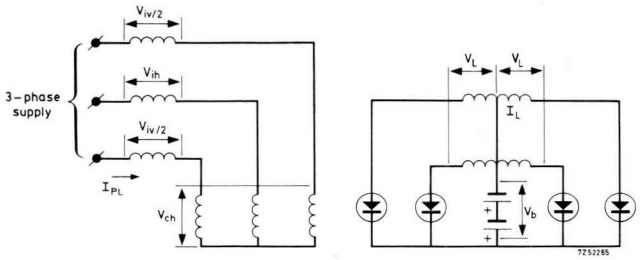


Fig. 10-17 Battery charger, four-phase half-wave.

10.4.3 63 V, 50 A Battery Charger

Equipment is required for charging a battery consisting of 50 Ni-Fe cells, at 50 A rated charge current. The circuit (Scott arrangement) appears in Fig. 10-17. Phase voltage is 220 V, 50 Hz.

Step 1: Secondary voltage per phase
From eq. (10-24), putting $\beta = 0.59$ and taking 1.25 as the nominal voltage level per cell, we find that the secondary voltage per phase must be

$$V_L = (50 \times 1.25 + 1)/0.59\sqrt{2} = 76 \text{ V}.$$

Diode currents are worked out in the table below.

volts per cell	max. 1.7 V	nom. 1.25 V	min. 1.05 V
β from eq. (10-1)	0.80	0.59	0.50
B' from Fig. 10-9	0.065	0.27	0.385
I_o	$\frac{0.065}{0.27} \times 50 =$ $= 12.0$ A	50 A (rated)	$\frac{0.385}{0.27} \times 50 =$ $= 71.3$ A
$I_{FAV} = I_o/4$	3.0 A	12.5 A	17.8 A
$F_{F'(p/av)}$ from Fig. 10-10	5.75	3.9	3.5
F_{fF}' from Fig. 10-10	2.75	1.8	1.7
$I_{FWM} = I_{FAV} \times F_{F'(p/v)}$	17.3 A	48.8 A	62.3 A
$I_{F\,\text{rms}} = I_L = I_{FAV} \times F_{ff'}$	8.25 A	22.5 A	30.3 A

Step 2: Selection of diodes
Peak reverse voltage across diodes, from eq. (10-16), is

$$2V_{B\,\max} = 2 \times 50 \times 1.7 = 170 \text{ V}.$$

Diode type BYX13-800
Step 3: Transformer VA rating (nominal battery voltage):
Eq. (10-34): $VA_{2n} = 4 \times 76 \times 22.5 = 6840\ VA$.
Eq. (10-27): $V_{1h} = 1.35 \times 220 = 297$ V.
Eq. (10-31): Turns ratio $N = 297/76 = 3.91$.
Eq. (10-22): Primary current $I_{PL} = 1.07 \times 22.5\sqrt{2}/3.91 = 8.7$ A
Eq. (10-35): $VA_{1n} = 2.91 \times 220 \times 8.7 = 5570\ VA$
Eq. (10-36): $VA_n = (6840 + 5570)/2 = 6205\ VA$
Step 4: Choke VA rating (nominal battery voltage):
Eq. (10-32): $V_1' = 0.9 \times 0.59 \times 220\sqrt{2} = 165$ V.
Eq. (10-37): $V_{ch} = \sqrt{(220^2 - 165^2)} = 146$ V.
Eq. (10-38): $VA_{(ch)} = (3 \times 146 \times 8.7)/2 = 1900\ VA$.

The Scott circuit has been used many times in the past. We have given calculations here for completeness sake as one may have to re-equip an existing mercury vapour tube rectifier, and hence an existing Scott transformer, with silicon diodes. Therefore some background of Scott transformers is useful.

10.5 Simple 6 V/12 V Car Battery Chargers

10.5.1 General

Car battery chargers must be inexpensive yet reliable in performance. They should be foolproof, capable of withstanding shorts and preferably reverse connection of the battery. The circuit should therefore incorporate some means of limiting current, such as an incandescent lamp of sufficient wattage (alternatively, the leakage inductance of the supply transformer can be used for that purpose), and fuses must be inserted where necessary. The charger must exhibit a predetermined current-limiting impedance which, at rated charge current, will compensate for the difference between peak output voltage and minimum battery voltage level.

The battery chargers described in this section, which are equipped with type BYX21 diodes, all meet the above requirements.

10.5.2 4 A Battery Charger using Incandescent Lamps as Current limiters

The schematic diagram is shown in Fig. 10-18. The fuse will protect against reverse connection of the battery. The diodes are mounted on a common $8 \times 12 \times 0.2$ cm aluminium heatsink. The performance of the charger is given in Table 10-4.

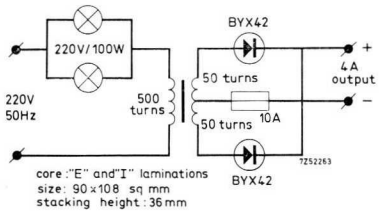


Fig. 10-18 Incandescent lamps as current limiter.

Table 10-4 Performance of 4 A battery charger employing incandescent lamps as current-limiting resistors (a.c. supply voltage 220 V nominal)

	voltage across transformer primary (V)	d.c. output current (A)
no output load	200	—
charging 12 V battery	140	3.8
charging 6 V battery	90	5.3
output shorted	30	7.0

10.5.3 4A Battery Charger with Leakage Transformer

The leakage transformer incorporated in this battery charger (Fig. 10-19) provides a very effective current-limiting action with low losses (Table

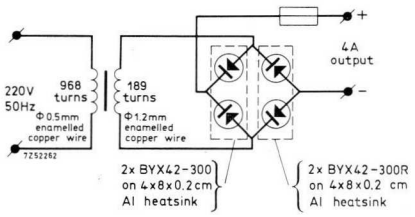


Fig. 10-19 Leakage transformer as current limiter (4 amp.).

10-5). The diodes are mounted on the heat-sinks in pairs. The transformer construction is shown in Figs 10-20 and 10-21. Two stacks of I-laminations provide a magnetic shunt. The height of these stacks must be adjusted to bring the performance of the charger into conformity with

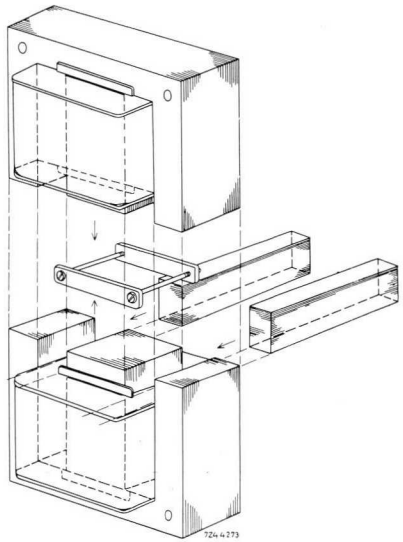


Fig. 10-20 Construction of battery charger leakage transformer.

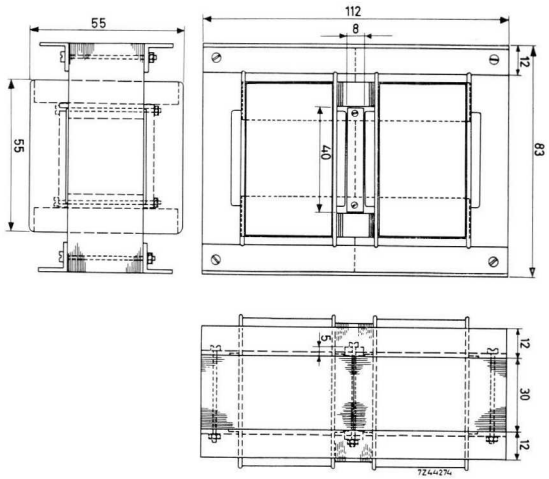


Fig. 10-21 4 Amp. battery charger leakage transformer-dimensions.

Table 10-5. The I-stacks must be shimmed with non-magnetic material to achieve constant leakage inductance.

Table 10-5 Performance of 4 A battery charger with leakage transformer (supply voltage 220 V a.v. nominal)

	primary current (A)	secondary voltage (V)	d.c. output current (A)
no output load	0.15	38	—
charging 12 V battery	0.95	16.5	3.8
charging 6 V battery	1.03	9	4.2
output shorted	1.05	—	4.4

10.5.4 20 A Battery Charger with Leakage Transformer

This type will provide rapid battery charging since it has a much higher output current rating (Fig. 10-22). The transformer construction is shown in Figs 10-20 and 10-23. Table 10-6 contains charger performance figures.

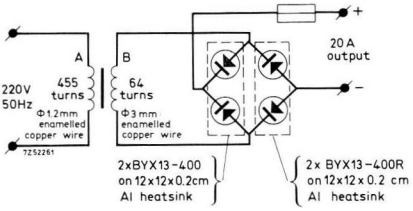


Fig. 10-22 Leakage transformer as current limiter (20 amp).

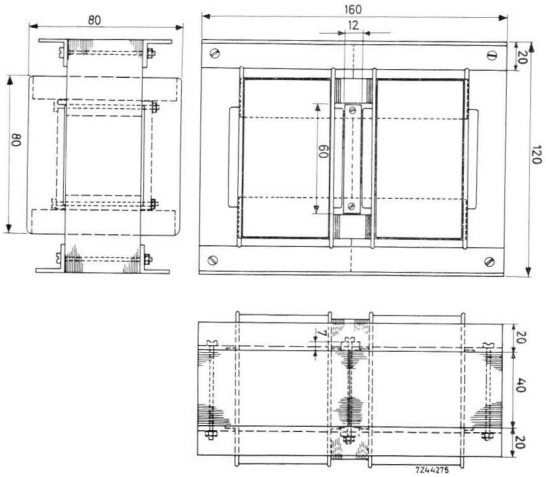


Fig. 10-23 20 Amp. battery charger leakage transformer-dimensions.

Table 10-6 Performance of 20 A battery charger with leakage transformer (a.c. supply voltage 220 V nominal)

	primary current (A)	secondary voltage (V)	d.c. output current (A)
no output load	0.7	28	—
charging 12 V battery	3.2	19.5	16.5
charging 6 V battery	3.8	9.5	22.0
output shorted	4.0	—	23.5

10.6 Battery Voltage Sensor

A traction battery voltage sensor to safeguard against excessive drain by the traction motor is illustrated in Fig. 10-24. It will cut out the traction motor at low battery voltage level or, trip a warning device. A timing circuit is incorporated to prevent the sensor responding to short duration battery voltage drops. Any drop in battery voltage will causes a change in the voltage level at the junction of R_1, R_2 which is applied to TR_1's base via zener diode D_1 without loss of sensitivity. TR_1's emitter receives approx. 0.8 V back-biasing voltage level from forward-biased diode D_2, which constitutes part of voltage divider D_2, R_7, D_3. At nominal battery voltage level (24 V), approx. 7 V drops across R_1, causing D_1 to break down.

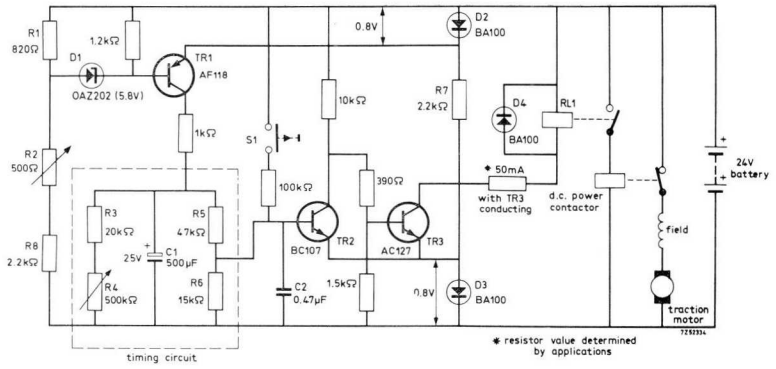


Fig. 10-24 Battery voltage sensor.

Sufficient voltage is applied to TR_1's base to overcome the emitter back-biasing voltage (over 0.3 V voltage drop between TR_1-base and emitter). Thus TR_1 will conduct, keeping timing capacitor C_1 charged to approx. 22 V. Sufficient current is delivered to TR_2's base to saturate this transistor despite the emitter reverse-biasing voltage originating from D_3. The accompanying low TR_2-collector saturation voltage drop maintains TR_3 in the OFF state. Thus, both relay RL_1 and the d.c. power contactor will remain de-energized.

When, owing to excessive battery drain, the sensor input voltage reduces to 22.8 V (1.9 V/cell), the voltage drop across R_1 is not large enough to maintain D_1 in its breakdown region. The base-emitter voltage of TR_1 drops below 0.2 V and it goes non-conducting. The voltage across C_1 collapses at a rate determined by the setting of R_4. When the voltage across C_1 drops below 7 V, TR_2 will switch OFF. TR_2's collector voltage rises, causing TR_3 to switch ON. The bottoming of TR_3 causes both RL_1 and the d.c. power to be energized, and the traction motor supply is interrupted. D_4 across relay RL_1 protects TR_3 against inductive voltage surges. TR_3 goes non-conducting at about one-third of the way down the discharge curve of C_1; in this region the decay in the capacitor voltage is fast enough to ensure reliable switching and at the same time minimize the variation in switching delay that may result from the spread in the gain characteristics of individual transistors.

If the battery voltage falls only momentarily below the controlled level, TR_1 too will pass only briefly into the OFF state and the decay in the voltage across C_1 will not go far enough for the contactor to come into

action. The delay in the sensor response can be adjusted between 15 and 40 seconds by means of R_4. Override button S_1 allows the van to be driven to the nearest charging station on a low battery. Its manipulation places a forward bias on TR_2, thereby de-energizing RL_1 and the d.c. power contactor and restoring the power supply to the motor. C_2 prevents interference from triggering the circuit.

R_2 adjusts the min. battery voltage level to which the sensor will respond, and caters for tolerances in D_1, D_2 and divider R_1, R_2, R_8. Input transistor TR_1 exhibits high gain and low leakage; there is a roughly 0.3 V difference between its switching levels. The sensor can easily be adapted to a higher battery voltage by connecting it up to the battery terminals via a resistive divider. The battery sensor can be improved by adding an expanded-scale 22-25 V voltmeter to monitor the battery voltage (Fig. 10-25). A 1 mA movement is connected across the output of a

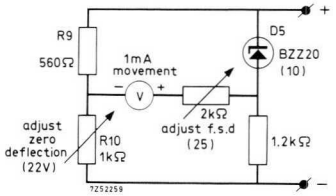


Fig. 10-25 Expanded scale voltmeter (22-25 V).

bridge whose input is fed by the battery voltage. Zener diode D_5 is incorporated to provide the expanded scale. Good scale linearity is accomplished by selecting low-ohmic resistors for R_9, R_{10}, leaving the voltage at the R_9, R_{10}-junction virtually unaffected by the current flowing through the meter. Trimmers are incorporated to adjust both zero and full-scale meter deflection.

11 Miscellaneous Applications

This chapter deals with applications in which power diodes play something other than a straight rectifying role. The "one-way" properties of these devices can be utilized to advantage in signalling systems such as traffic control or annunciating schemes, in two-position control of heating systems for switching between partial and full load or between zero and partial load, for protecting accumulators under charge against inadvertent reversal of leads, and so on. In cases where a controlled rectifier (thyristor) system powers an inductive load, a diode can be connected across the rectifier output in order to make the current in the load continuous over the major part of the output control range. Lastly, the diode forward threshold voltage may be turned to account in voltage-limiting circuitry for measuring instruments, or for protecting a secondary battery against overcharging.

11.1 Application in Control Systems

11.1.1 Traffic Control

In areas where roads are under repair one lane may be obstructed over a considerable length. A two-phase traffic control system will be adequate in most instances to maintain a regular flow of traffic from either side in turn, via the unobstructed lane. An all-red phase must be interlaced to clear the lane before admitting traffic from the opposite direction. The use of twin rather than triple-cored interconnecting cable will reduce the cost of such temporary installations. One possible scheme is shown in Fig. 11-1. The traffic lights are switched by reversing the polarity of the rectified a.c. supply. The circuit provides full-wave rectification and so the r.m.s. voltage level does not change, allowing normal lamp types to be employed. During a "red" phase the polarity is such that La_2 will be shorted by D_2 while La_1 is on. The opposite applies during a "green" phase. Fig. 11-2 shows an alternative wiring arrangement for the lamps.

11.1.2 Temperature Control

In two-position temperature control systems for ovens, temperature

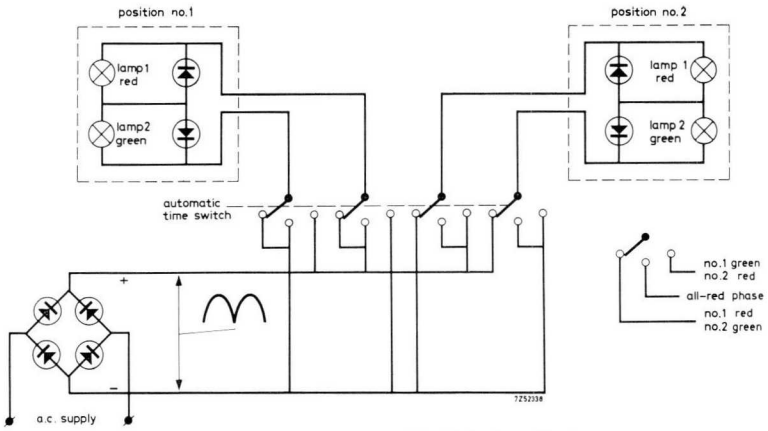


Fig. 11-1 Temporary traffic light installation.

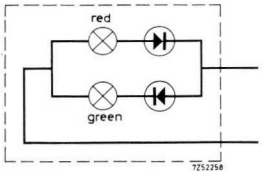


Fig. 11-2 Alternative diode arrangement for temporary traffic light installation.

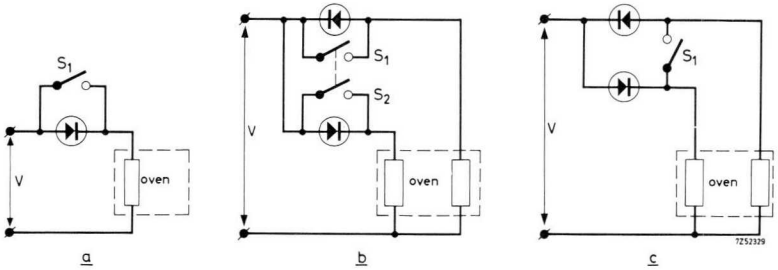


Fig. 11-3 Temperature control of ovens using diodes.

stabilization will be improved if the heating power is switched between narrower limits. Thus, oven temperature fluctuations are reduced when the input alternates between half and full power rather than switching between zero and full. Some arrangements that do away with the need for a tapped autotransformer may be found in Fig. 11-3; in each of these, changeover between half and full oven input power is effected by switching

diodes placed in series with the heating elements. The very simple circuit in diagram *a* passes only half-waves when switched to half power, and is suitable in cases where the mains supply is not transformed. Circuits *b* and *c* can be used in ovens equipped with an even number of heating elements intended for operation in parallel.

The diode ratings must be selected to withstand full power level P as given by one of the following formulae.

Fig. 11-3*a* and *c*: $$P = \pi I_{FAV\ \max} V_{PL}/\sqrt{2} \quad (11\text{-}1)$$

Fig. 11-3*b*: $$P = 2\pi I_{FAV\ \max} V_{PL}/\sqrt{2} \quad (11\text{-}2)$$

where:

$I_{FAV\ \max}$ = diode current rating (average)

V_{PL} = r.m.s. a.c. supply voltage

Thus, for 20 A diode rating and 220 V a.c. supply voltage we find 9.76 kW and 19.52 kW full output power for Fig. 11-3*a* and *c* and Fig. 11-3*b* respectively.

11.2 Application in Protection Circuits

11.2.1 Protection of Meters

A minimum forward voltage (threshold value) is needed to make a diode fully conductive. The diode current is relatively small for any forward voltage drop below the threshold value, but rises rapidly once the threshold is exceeded. This feature makes the diode useful as a voltage-limiting element. A conventional protective circuit for a measuring instrument is shown in Fig. 11-4. If the voltage (either polarity) across the meter terminals and the series resistor should start to exceed the diode

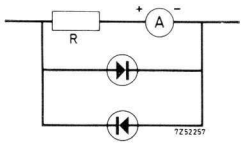


Fig. 11-4 Meter protection using diodes.

threshold voltage, the major part of the current will be diverted through the diodes, thus safe-guarding the meter against burn-out or mechanical damage. Depending on the overload sensitivity of the movement, the diode threshold voltage should not exceed two of five times the total

voltage drop occurring across the meter and series resistor R at full scale deflection. The correct value of series resistor is essential in the case of a sensitive movement. At a larger full-scale voltage drop, the resistor can be omitted; indeed, it may be necessary to place two or more seriesed diodes in parallel with the meter circuit. The diodes must be matched to the meter circuit to maintain scale linearity; at full-scale deflection the diode current should be low compared to the meter current.

11.2.2 Protection of Batteries

A method of protecting small secondary batteries against overcharging is illustrated in Fig. 11-5. The overall threshold voltage of the paralleled diodes will be exceeded as soon as the battery becomes fully charged, thus providing a "spillway" for excessive charge current. The diodes must be selected according to the voltage level of the battery in the fully charged state; the diode threshold voltage is approx. 0.7 V for silicon types, and approx. 0.4 V for germanium types, and will decrease as junction temperature increases.

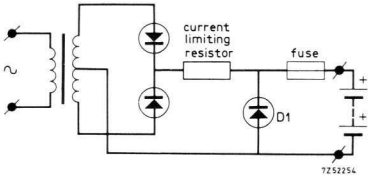


Fig. 11-5 Protection of batteries from overcharging by using diodes.

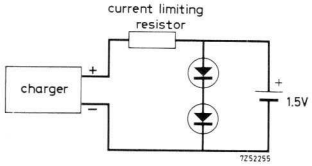


Fig. 11-6 Protection against reversing of battery leads.

The circuit depicted in Fig. 11-6 provides enhanced discrimination against reversal of charge current. When the battery terminals are reversed, the fuse will rapidly blow because protective diode D_1 becomes conductive. D_1 must be rated to withstand the short circuit current during the clearing time of the fuse.

11.3 Application as a Signalling Device

Fig. 11-7 shows the application of diodes in current indicating circuitry. The diodes will ensure that across the indicator lamp, an almost constant voltage appears (approx. 1.5 V) over a wide range of load current. This arrangement provides much more reliable evidence that current is being

taken by the load than does a pilot lamp placed across the load side of the switch which only indicates that voltage is applied. The diodes must be rated to withstand any inrush load current.

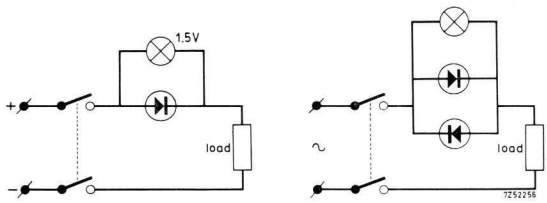


Fig. 11-7 Indicator lamps connected across rectifying diodes.

11.4 Application as a Load Current Smoothing Element

11.4.1 General

Smoothing of the output current from a controlled rectifier (thyristor) system is achieved by placing a reactor in series with the load. To ensure continuous current flow over the major part of the output control range, a very large and hence expensive reactor would be needed. A diode placed across the output, on the supply side of the reactor, gives continuous current flow even at large control angles, thus making better use of the reactor throughout the whole range of output control. In addition, an improved rectifier system power factor results, while less severe voltage jumps occur across the thyristors. Because the load current flows continuously, the load reactor produces no transients likely to damage the thyristors.

11.4.2 The Operation of the Free-wheeling Diode [18]

The operation of an inductively loaded two-phase half-wave rectifier circuit, not equipped with a smoothing diode, is shown in Fig. 11-8. Smoothing reactor L opposes any change in d.c. output current, and when time constant L/R_{load} is infinite a perfectly smoothed d.c. current results. When the secondary a.c. voltage starts to go negative, the voltage developed across the smoothing reactor by the somewhat decreasing current continues to force current through the load against the transformer secondary voltages; this prolongs Th_1's conduction until Th_2 starts conducting and vice versa. Neglecting rectifier circuit losses and transformer leakage inductance, the steady-state d.c. output voltage may be expressed as:

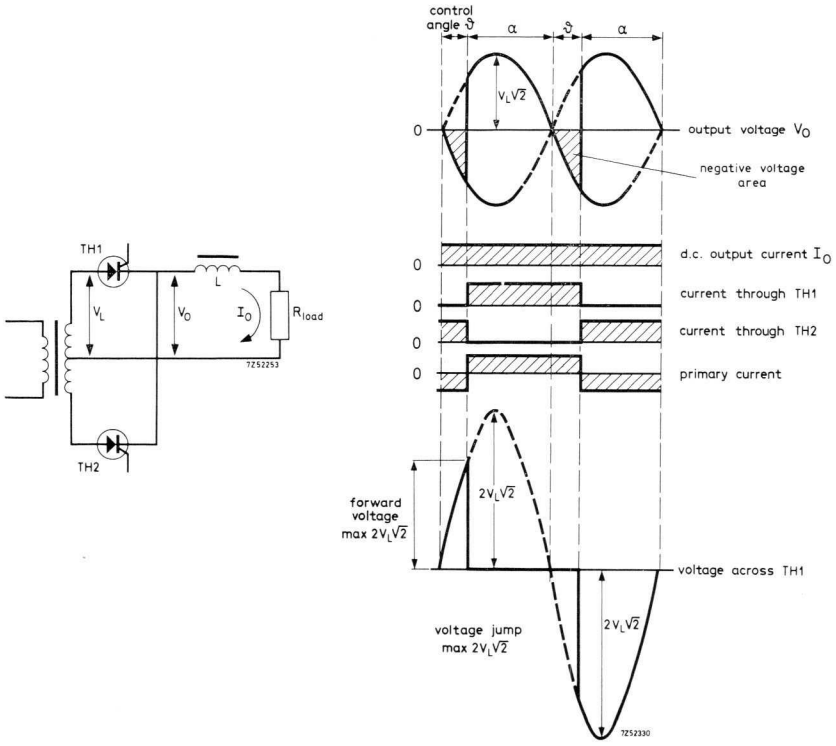


Fig. 11-8 Two-phase half-wave rectifier supply using SCRs and inductive smoothing.

$$V_o(\vartheta) = \frac{1}{\pi}\int_{\vartheta}^{\pi+\vartheta} V_L\sqrt{2}\sin\omega_s t\,\mathrm{d}\omega_s t = \frac{2}{\pi}V_L\sqrt{2}\cos\vartheta, \qquad (11\text{-}3)$$

where ϑ = control angle.
(See Fig. 11-10; curve *a*.)

In a practical circuit, load resistance R_{load} will not be zero so that time constant L/R_{load} will have a finite value. The output voltage will deviate from curve *a* at a certain control angle between 0 and $\pi/2$, and ultimately reduce to zero at $\vartheta = \pi$. This deviation, represented in Fig. 11-10 by curve *c*, is caused by the load current becoming intermittent. The point at which the discontinuity sets in depends on the time constant L/R_{load} of the output circuit.

The effect of adding a smoothing diode is illustrated in Fig. 11-9. As

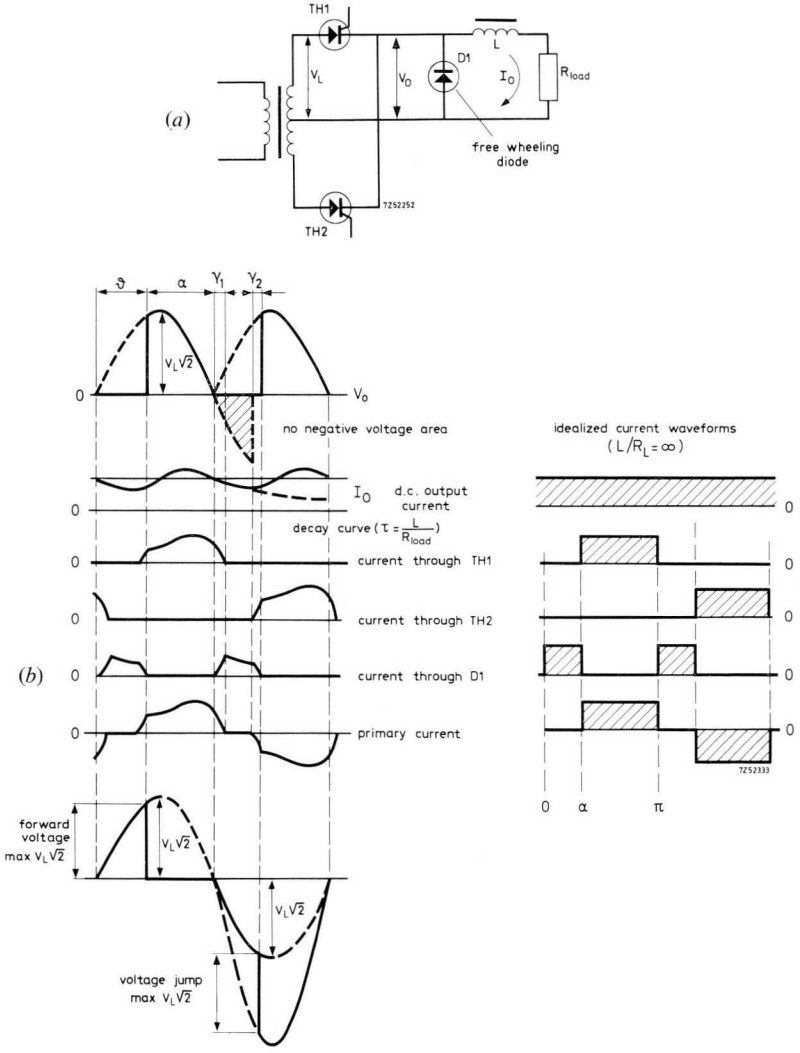


Fig. 11-9 Supply of Fig. 11-8 with free-wheeling diode added. (a) circuit; (b) idealized waveforms.

soon as the output voltage V_o starts to become negative, shunt diode D_1

(termed free-wheeling diode) will conduct and so allow the reactor to expend its stored energy through the load unhindered by an opposing voltage from the transformer. The purpose of the diode is to maintain the flow of load current during periods of zero output voltage as thyristors Th_1 and Th_2 cease to conduct as soon as their supply voltage drops below that required to supply their holding current. While D_1 is conducting, the load current decays exponentially depending on the time constant L/R_{load} (ref. dotted line in d.c. output current curve, Fig. 11-9) until thyristor turn-ON. Thus, the output current swings around an average value I_o, and its ripple depends both on L/R_{load} and control angle. Owing to the transformer leakage inductance there will be no immediate current take-over between thyristor and free-wheeling diode, and vice versa, so commutation will occur in any practical system; commutation angles γ_1, γ_2 (Fig. 11-9) are determined by reactor and transformer leakage inductance, supply voltage and load resistance.

When thyristor turn-ON is delayed, the d.c. current that would normally be carried by the transformer windings is diverted through the free-wheeling diode. Hence, at given d.c. output current, the r.m.s. value of the a.c. current is reduced, which results in an increased rectifier system power factor.

The output voltage waveshape depicted in Fig. 11-9 resembles that obtained with a pure resistive load. Neglecting circuit losses and transformer leakage, the d.c. output voltage is expressed as:

$$V_o(\vartheta) = \frac{1}{\pi}\int_{\vartheta}^{\pi} V_L\sqrt{2}\sin\omega_s t\,\mathrm{d}\omega_s = V_L\sqrt{2}(1+\cos\vartheta)/\pi. \qquad (11\text{-}4)$$

(See Fig. 11-10, curve *b*.)

Comparison of thyristor voltage waveshapes without and with free-wheeling diode added (Fig. 11-8, 11-9) shows that in the first instance a sudden voltage jump will occur during commutation. This voltage jump attains its maximum value $(2V_L\sqrt{2})$ (Fig. 11-8) for $\vartheta = \pi/2$ and heavy transients may occur due to hole storage recovery and transformer inductance. In the circuit shown in Fig. 11-9 however, the thyristor will have recovered long before a reverse voltage jump occurs (max. $V_L\sqrt{2}$ at $\vartheta = \pi/2$).

The benefits of including a free-wheeling diode in a rectifier installation may be summarized as follows:

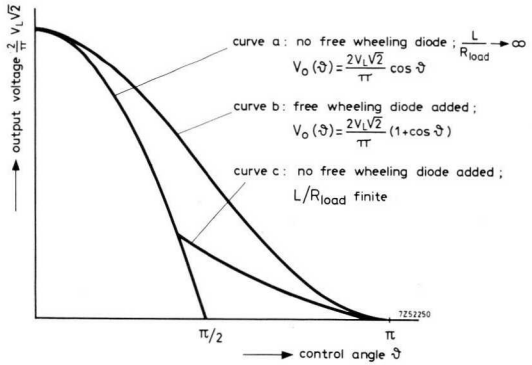


Fig. 11-10 Output voltage/control angle. ϑ for two-phase half-wave, and single-phase regenerative bridge rectifiers.

— it enhances the smoothing action of the reactor and so adds to its efficiency throughout the range of output control; even in simple, non-controlled half-wave rectifiers a considerable improvement may be effected in this way [19] [20]; in the case of two-phase half-wave rectification, a time constant (reactor inductance over load resistance) equal to one-half power period will suffice to provide a continuous flow of current for any control angle from 0 to nearly 180 deg [18];
— it increases the system power factor over the entire range of control angle;
— it reduces output voltage ripple at larger control angles since negative voltage areas do not occur;
— it reduces the voltage jumps and transients that accompany commutation and reverse recovery in thyristors, thereby making the output voltage less spiky and reducing the electrical stresses that thyristors must withstand.

11.4.3 Voltage Rating of Free-wheeling Diode

The diode must of course be able to block useful voltage level continuously, but the required reverse voltage rating cannot be fixed without knowledge of the transients occurring in the output voltage waveform. These, however, may stem from a variety of causes — the breaking of the primary circuit, the leakage inductance of the supply transformer, and reverse recovery in the thyristors and the free-wheeling diode itself.

The wisest course is to experiment on a breadboard version of the circuit and so determine the highest peak occurring.

The amplitude of spikes caused by reverse recovery in the thyristors can be reduced by a factor of two or more by using a diode whose own recovery time is very short.

During its recovery time the diode presents a short circuit to the rectified output. A heavy current flows momentarily, and in this way the diode itself becomes responsible for an inductive voltage transient of considerable magnitude.

Such voltage transients will be particularly severe at a low control angle, i.e. at almost full output current. Choosing a fast recovery free-wheeling diode will reduce the shunting time and hence the magnitude of the voltage transient. Another method of limiting the amplitude of this type of voltage surge is to connect a small capacitor with a damping resistor in series across both the reactor and the secondary of the supply transformer. When transient conditions are not known or if the design is still in the breadboard stage, a free-wheeling diode with a reverse rating of approx. 6 times peak output voltage is recommended. This rating may be reduced when the actual transients are known. A controlled avalanche diode is not necessarily the best answer in all circumstances, since the energy content of the transient may be considerable.

11.4.4 Current Rating of Free-wheeling Diode

In between the times at which the thyristors are conducting, the load current decays exponentially (Fig. 11-9) but for the purpose of fixing the diode rating it can safely be assumed to remain steady at the mean level I_o. This implies that the inductive load has a time constant of infinity and a power factor of zero; the leakage inductance of the transformer is ignored. It will further be assumed, in what follows, that the inductive load is passive; the argument does not therefore apply to motor control circuits. We now proceed to derive the average free-wheeling diode current I_{D1} as a function of control angle ϑ for two-phase, half-wave circuits (Fig. 11-11).

$$\text{Free-wheeling diode Duty Factor} = \vartheta/\pi. \tag{11-5}$$

From eq. (11-4):

$$I_o(\vartheta) = V_L/2(1 + \cos \vartheta)/\pi R_{load}. \tag{11-6}$$

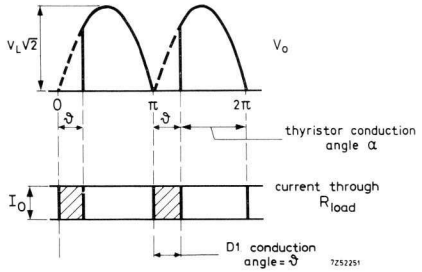


Fig. 11-11 Free-wheeling diode and thyristor conduction.

For zero control angle ($\vartheta = 0$), max. d.c. current:

$$I_o = 2\ V_L\sqrt{2}/\pi R_{load}. \tag{11-7}$$

where R_{load} = load resistance.

From the above equations:

$$I_{D1}/I_o = \vartheta(1 + \cos\vartheta)/2\pi. \tag{11-8}$$

I_{D1}/I_o has been plotted vs. ϑ in Fig. 11-12; it reaches its maximum value (0.262) around $\vartheta = 75$ degrees.

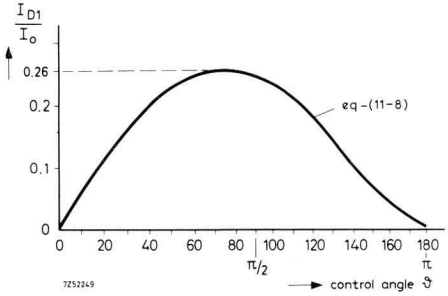


Fig. 11-12 Plot of $I_{D1}/I_o = f(v)$.

In practice I_{D1} values will be lower, actual load circuits having a finite time constant, and it will be safe to use a diode whose average current rating is one-quarter of the maximum average load current.

This rule is valid for two-phase, half-wave configurations. In the case of three-phase half-wave rectification, the free-wheeling diode will

conduct only for control angles ϑ exceeding 30 degrees (Fig. 11-13). From Fig. 11-14:

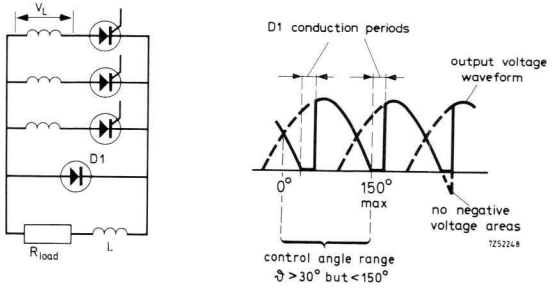


Fig. 11-13 Three-phase half-wave rectifier system with free-wheeling diode added.

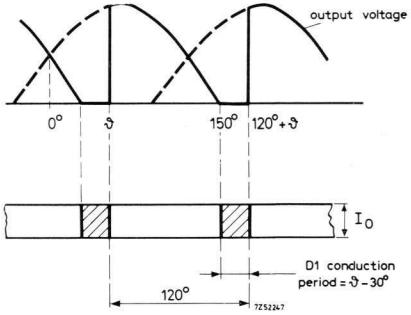


Fig. 11-14 Free-wheeling diode current.

$$\text{Free-wheeling diode Duty Factor} = (\vartheta - 30°)/120°. \tag{11-9}$$

For $\vartheta \geqslant 30°$:

$$I_o(\vartheta) = 3\ V_L/2\{1 + \cos(\vartheta + 30)\}/2\pi R_{load}. \tag{11-10}$$

For $\vartheta = 0$, max. load current:

$$I_o = 3\ V_L/6/2\pi R_{load}. \tag{11-11}$$

Thus:

$$\frac{I_{D1}}{I_o} = \frac{\vartheta - 30°}{120°} \times \frac{1 + \cos(\vartheta + 30°)}{\sqrt{3}} \tag{11-12}$$

for $\vartheta > 30°$ but $< 150°$.

Similarly, for *six-phase half-wave rectification*,

$$\frac{I_{D1}}{I_o} = \frac{\vartheta - 60^\circ}{60^\circ} \times [1 + \cos(\vartheta + 60^\circ)] \qquad (11\text{-}13)$$

for $\vartheta > 60^\circ$ but $< 120^\circ$.

where

I_{D1} = average current through free-wheeling diode = control angle.

I_{D1}/I_o vs. control angle ϑ has been plotted in Fig. 11-15 for both circuits. In a practical circuit where L/R_{load} is finite. take the following average currents:

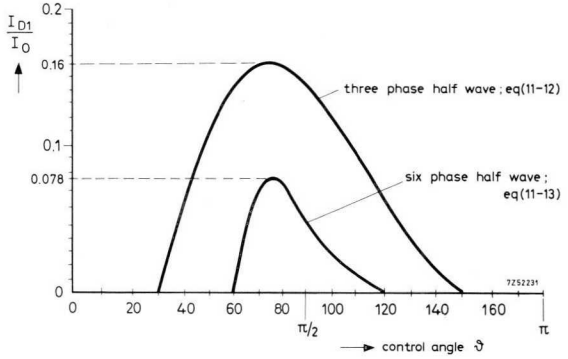


Fig. 11-15 Plot of I_{D1}/I_o vs ϑ for three-phase half-wave and six-phase half wave rectifier circuits.

Three-phase half-wave: 0.15 × max. average load current.
Six-phase half-wave: 0.075 × max. average load current.

When choosing a diode for free-wheeling purposes, its peak current rating has also to be considered. In the above analysis, a square wave free-wheeling diode current has been assumed whose duty factor depends upon the off-time of the supply current. The free-wheeling diode peak current will equal the average d.c. current flowing through the load. It will increase as the thyristor firing angle is reduced, and will become equal to the max. average load current at zero control angle due to the finite commutation period between successive thyristors. Thus, the free-wheeling diode peak rating must conform to *max. average load current.*

11.4.5 Regenerative and Non-regenerative Rectifier Bridges

A rectifier bridge is said to be regenerative when it feeds power back into the supply source during part of the a.c. cycle. Since for inverter action an e.m.f. must be generated in the load circuit, regeneration can only occur with inductive loading. In the case of a non-regenerative bridge, the rectifier system will operate as a true a.c./d.c. converter during the whole of the power cycle.

All-thyristor bridges are of the regenerative type since the load reactor keeps the thyristors conducting until commutation occurs, thus exerting regenerative action. Bridges equipped with both controlled and uncontrolled rectifier elements will exhibit no regenerative action because the uncontrolled rectifier elements provide a shunting path for the current delivered by the inductive load. Since free-wheeling action is already provided internally, the latter bridge types do not need an external free-wheeling diode.

Single-Phase Bridge. Fig. 11-16 illustrates the operation of a single-phase

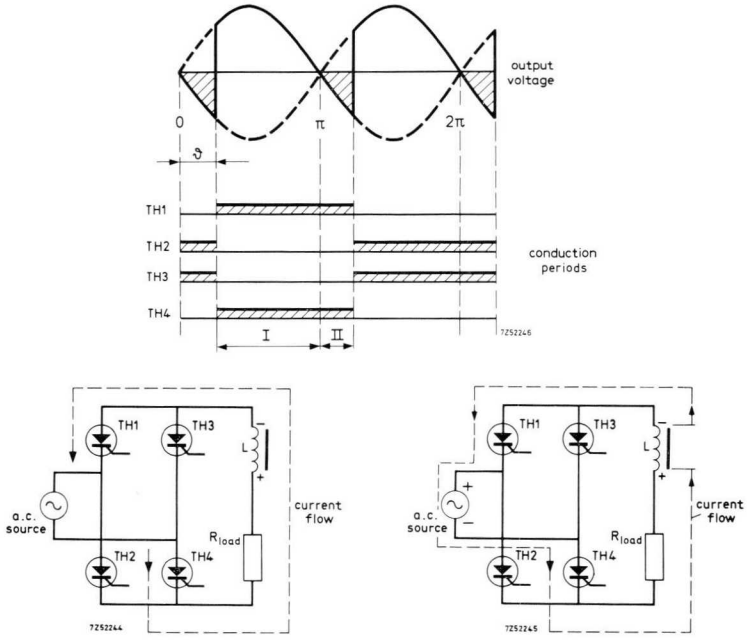


Fig. 11-16 Operation of a single-phase bridge rectifier system using thyristors.

regenerative bridge equipped with four thyristors. The bridge can be made non-regenerative by connecting a free-wheeling diode across its output.

Non-regenerative bridges may have thyristors in one single pair of seriesed or paralleled bridge arms (Fig. 11-17). When thyristors are incorporated in seriesed legs, as in Fig. 11-17a and b the diodes provide a shunt path for the current generated by the load reactor, and they continue to conduct during supply current off-periods. When thyristors are placed in paralleled legs (Fig. 11-17c and d), the reactor e.m.f. will extend the conduction period of each thyristor so that the thyristor provides a current path in conjunction with its series diode. Thus, during supply

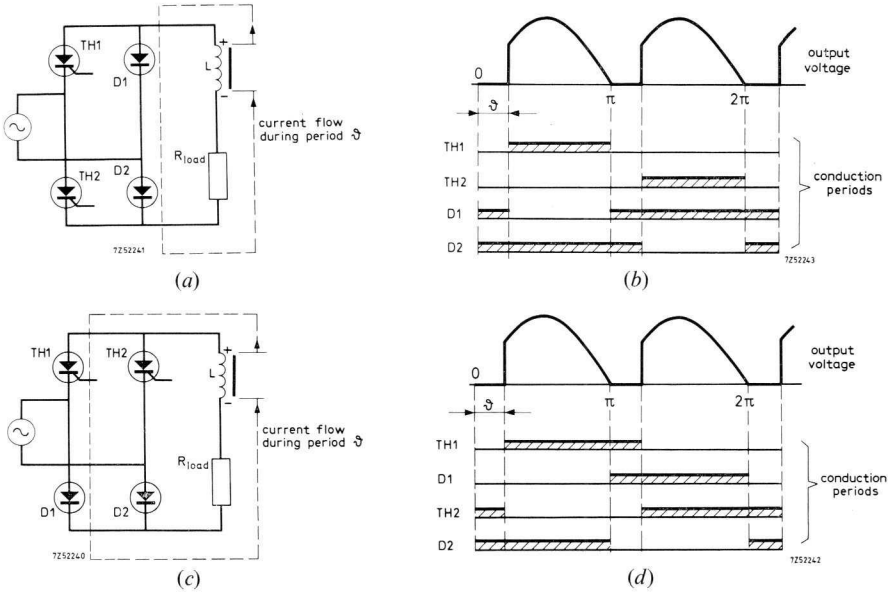


Fig. 11-17 Non-regenerative, full-wave rectifiers:
(a) thyristors in seriesed legs;
(b) conduction periods of elements shown in 11-17a;
(c) thyristors in parallel legs;
(d) conduction periods of elements shown in 11-17c.

current off-times, D_1, Th_1 and D_2, Th_2 conduct alternately. At any point in the output control range, all the rectifier elements in this circuit have conduction intervals of equal duration; they can therefore have the same current rating. This is not true of the bridge circuit in Fig. 11-17a. Because

diodes D_1 D_2 conduct over longer intervals, they must be of a slightly higher rating, as will be clear from the following analysis.

The duty factor of diodes D_1 and D_2 in Fig. 11-17a is

$$(\pi + \vartheta)/2\pi \tag{11-14}$$

from eq. (11-4) we have

$$\text{Load current } I_o(\vartheta) = V_L(1 + \cos \vartheta)\sqrt{2}/\pi R = I_o(1 + \cos \vartheta)/2 \tag{11-15}$$

where I_o = max. load current ($\vartheta = 0$)

V_L = r.m.s. a.c. input voltage.

Assuming infinite L/R_{Load} (pure d.c. load current) we derive from the above equations:

$$I_{FAV}(D_1,D_2)/I_o = (1 + \cos \vartheta)(\pi + \vartheta)/4\pi \tag{11-16}$$

where $I_{FAV}(D_1,D_2)$ is the average current through D_1 and D_2 (ϑ in radians).

Likewise we find:

$$I_{FAV}(Th_1,Th_2)/I_o = (1 + \cos \vartheta)(\pi - \vartheta)/4\pi \tag{11-17}$$

where $I_{FAV}(Th_1,Th_2)$ is the average current through Th_1 and Th_2.

Equations (11-16) and (11-17) are represented graphically in Fig. 11-18. from which it will be seen that the diodes must have an approx. 10% higher average current rating. However, where devices are amply rated, this 10% may be readily ignored.

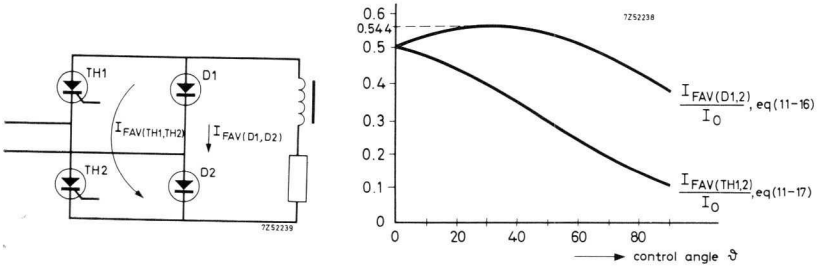


Fig. 11-18 Graph of equations (11-16) and (11-17).

The above considerations do not apply to motor drive circuitry.

Three-phase Bridge. In a non-regenerative three-phase bridge (Fig. 11-19), Th_1 and D_1, Th_2 and D_2, Th_3 and D_3 will conduct in turn during supply current off-periods, passing a current generated by the load reactor, exactly as in the single-phase bridge type illustrated in Fig. 11-17b. All cells have equal conduction periods and can thus have the same rating.

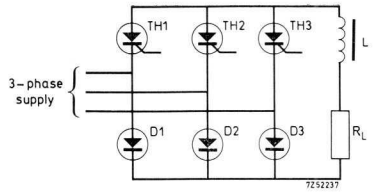


Fig. 11-19 Non-regenerative three-phase bridge system.

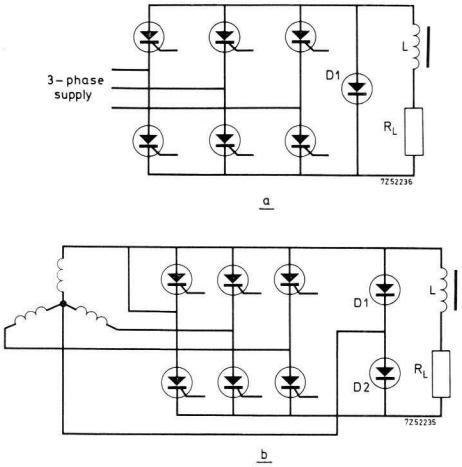


Fig. 11-20 (a) Three-phase bridge made non-regenerative free-wheeling diode; (b) as (a) but neutral line included to allow the use of two diodes.

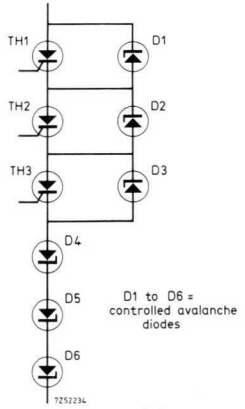
Three-phase bridges equipped with six thyristors can be made non-regenerative by adding one or two free-wheeling diodes (Fig. 11-20). Since zero output voltage periods occur for control angles exceeding 60°, the advantage obtained from a single free-wheeling diode (Fig. 11-20a) will be small, although the severity of reverse voltage jumps will be reduced for $\vartheta > 60°$. However, where a transformer neutral point is available, two free-wheeling diodes can be employed, as in Fig. 11-20b. The circuit may be regarded as a series combination of two three-phase half-wave rectifiers operating 30° out of phase, in which the free-wheeling diodes start to conduct as early as $\vartheta = 30°$ and are therefore more effective. The required free-wheeling diode rating is as derived in section 11.5.4 for three-phase half-wave rectifier systems.

11.5 Controlled Avalanche Devices as High-voltage Zener Diodes

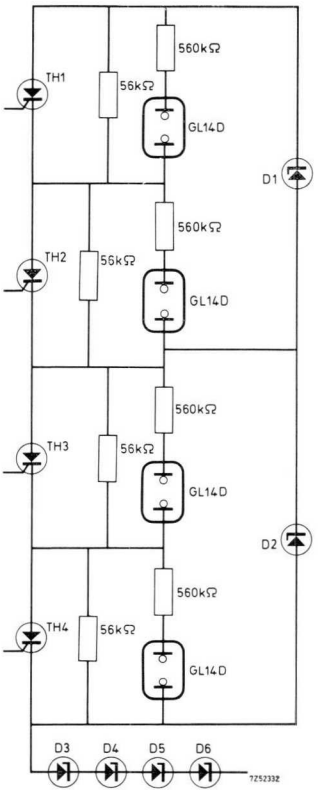
Because of their consistent reverse breakdown voltage controlled avalanche diodes may be used for overvoltage protection of the circuits dealt with below, these being only a few of the numerous applications.

11.5.1 Forced Voltage sharing in Series Legs

Forced voltage-sharing networks employing controlled avalanche diodes to protect thyristor in series chains against forward breakover caused by transients are shown in Fig. 11-21a and b. To afford this protection, the minimum breakover level of the thyristors in Fig. 11-21a must exceed the maximum reverse breakdown level of the diodes D_1, D_2 and D_3 placed in parallel with them.



(*a*)



(*b*)

Fig. 11-21 (a) Forced voltage sharing network using controlled avalanche diodes; (b) Forced voltage sharing network using redundancy to improve reliability.

Controlled avalanche devices D_4 to D_6 are added to enable the series chain to block reverse current. These diodes must be selected to withstand the peak voltage applied to the circuit in the reverse direction. If one of the thyristors in this circuit should fail to turn ON, the diode in parallel with it would risk destruction as a result of having to dissipate the full half-cycle power, $V_{R(BR)} \times I_{anode}$. The circuit in Fig. 11-21b is free from the drawback, for it is most unlikely that both the thyristors placed in parallel with a single reverse-biased diode would fail to turn ON. Diodes are selected which have a minimum avalanching voltage higher than the max. breakover voltage level per thyristor but a max. avalanching voltage lower than twice the min. breakover voltage of the thyristor. If now, Th_2, Th_3, Th_4 are triggered, Th_1 will be forced into conduction, thus protecting D_1 against excessive dissipation. This protection cannot be obtained from normal thyristors because their behaviour becomes highly unpredictable when the specified minimum breakover level is surpassed so it is advisable to use controlled-avalanche types. If in the case cited above Th_1 does not go into conduction, a situation will arise like that referred to in Fig. 11-21a. This may lead to the destruction of parallel diode D_1 and of thyristor Th_1, if its surge voltage rating is exceeded. Parallel resistors are incorporated to achieve adequate voltage sharing between thyristor pairs. Neon lamps have been added for monitoring purposes; all lamps should glow under OFF condition, and should go out when load current flows.

It will be noted that the voltage-sharing network is extremely simple. The circuit has been employed without modification in a practical rectifier system using twenty thyristors in series and rated to deliver 30 A at 11 kV.

11.5.2 Protection of Voltage-sensitive Loads

A system to protect a voltage-sensitive load is shown in Fig. 11-22. Any overvoltage will be clamped to D_1's breakdown level. If the surge voltage

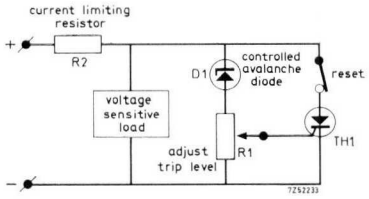


Fig. 11-22 Protection of voltage sensitive load.

should exceed D_1's avalanche voltage, the current through dropping resistor R_1 will be large enough to trigger overload-sensing thyristor Th_1, which protects the controlled-avalanche diode by shorting out the entire circuit. R_2 is placed in series, to limit the thyristor current.

11.5.3 Regenerative Voltage Protection

The circuit shown in Fig. 11-23 may be used to protect a rectifier system against regenerative voltages produced by a d.c. motor. A thyristor in series with a current-limiting (braking) resistor R is connected across each of the rectifier legs to one of the a.c. lines. Common point M will be positive whenever rectifier diode D_1 is conducting and negative when D_2 conducts 180° later, making V_M sinusoidal, as shown by the waveforms. When no regenerative action occurs, both thyristors are in their blocking state and the controlled avalanche diodes D_3, D_4 will operate below their breakdown level. Hence no energy is dissipated in braking resistors R.

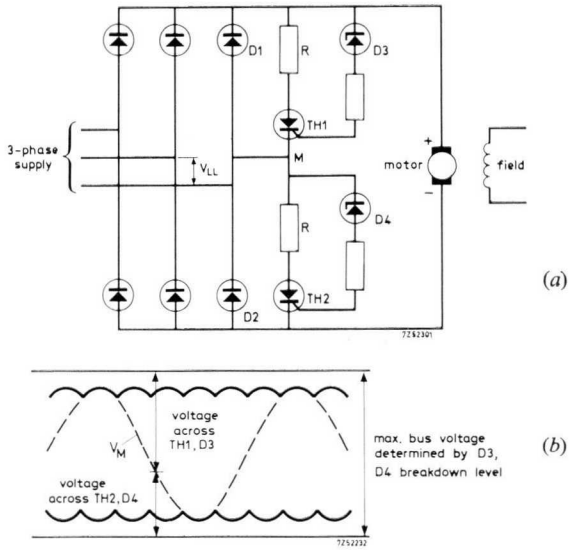
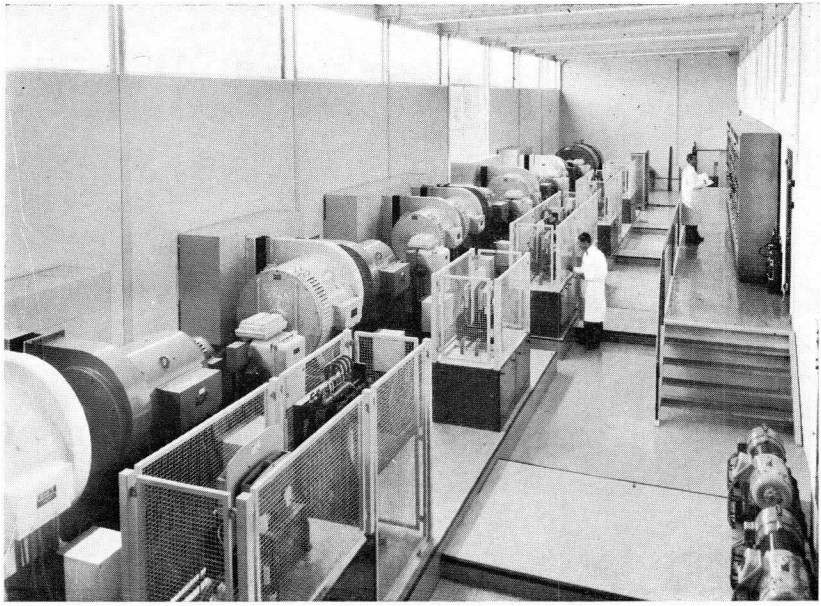


Fig. 11-23 Electronic braking system: (a) circuit; (b) waveforms.

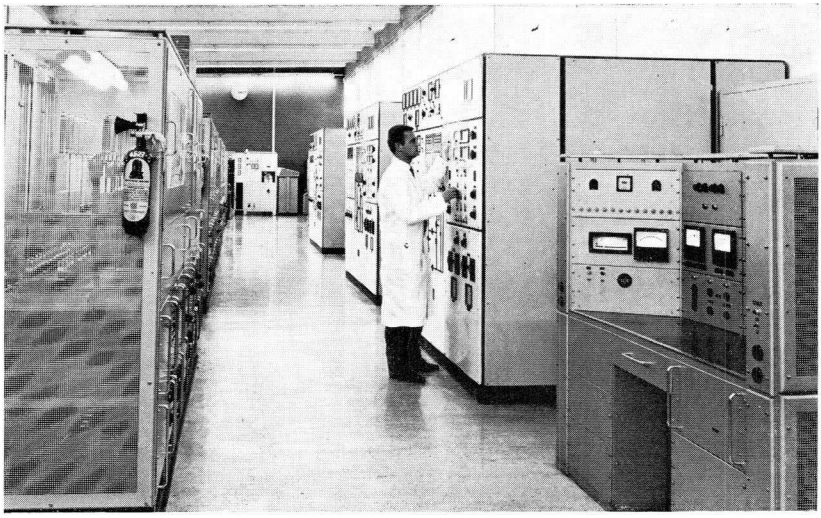
During regenerative action the motor, operating now as a generator, will try to feed back into the rectifier. The motor voltage supplied to the d.c. bus is higher than the voltage supplied by the rectifier. The diodes

block the reverse current flow, so a separate path for this current has to be arranged. Thyristors Th_1 and Th_2 together with braking resistors R act as such. When the bus voltage, generated by the motor, exceeds the avalanche voltage of D_3 or D_4, the thyristors are triggered and the resistors R cause the motor to brake.

When motoring action is resumed, D_1 and D_2 start to conduct again. This reverses the voltages on Th_1 and Th_2 and hence they regain their non-conducting state. If controlled-avalanche types are selected for Th_1, Th_2 diodes D_3, D_4 might be omitted, provided they avalanche at the desired bus voltage level. The circuit applies to single-phase bridge rectifier systems as well.



Machinery hall of Life Testing Laboratory.



Control room of Life Testing Laboratory.

12 Quality and Reliability

12.1 Introduction

Chapter 1 describes some of the features whereby a mechanically and electrically robust diode is made and the problems which have to be overcome to ensure that reliability is built in. This chapter discusses reliability qualitatively and gives an outline of the efforts taken to achieve it in power diodes.

12.2 Reliability

Reliability is the ability of an item to perform a required function under stated conditions for a stated period of time (IEC TC56). The ultimate reliability cannot be better than that of the weakest link in the whole chain of processes from design to dispatch of the finished product. Among their other duties inspection and quality control continually highlight these weak links so that corrective action can be taken, thereby increasing the yield.

12.2.1 Design Reliability

The designer in a diode development department has a target specification for a new diode, generally compiled from a survey of customer requirements, and his first approach is to study the specifications of available diodes to ascertain whether selection from an existing production line would give the desired new component. This is rarely the case and he must then resort to introducing changes to one or more of the manufacturing processes to meet the requirements of the specification. The designer considers introducing few changes at one time. As far as possible he avoids a completely new manufacturing technique as generally, until it has been mastered by the production staff, it causes trouble and lowers the reliability and hence the yield, so increasing the cost. Also, new tests have to be instituted to establish that the new technique is completely under control thus further increasing the cost.

Before proposing changes the designer studies the reports and control charts which inspection and quality control departments have laboriously compiled over the previous years; these show him which processes are

easily controllable and hence the simplest to change. The proposals are then discussed with representatives from manufacturing, commercial and inspection departments so that all forseeable difficulties can be solved.

Prototypes of the new device are made and tested under laboratory conditions and further development is conducted to completely understand and improve any new processes. Once the whole manufacturing process appears to be controllable and the device represents a sound commercial investment, pre-production or sample batches are ordered to be made under assembly line conditions and tentative data sheets drawn up.

12.2.2 Pre-production and Inspection

Once the approval has been given to make pre-production samples, the inspection and quality control departments play an increasingly greater part in the control of manufacture of the diode and the designer a lesser part.

Inspection is introduced at every process in the production line to assist the operators in mastering any new techniques. All variables (e.g. furnace temperature, diffusion time) are recorded to determine quantitively, the correlation between the variables and the process defect rate and the correlation between the variables and the overall defect rate after all environmental tests have been conducted. To establish this accurately means that either much of the inspection has to be 100% or that very large samples have to be taken. From the finished components samples are taken for environmental testing to examine the ability of a device to withstand the rougher treatment it will receive during its life. Also life tests are started to measure the parameter changes with respect to time. The results from all this testing enable inspection and quality control departments to:

— draw up their control charts putting in upper and lower warning limits;
— finalise the inspection sampling schemes to be employed when diodes are in full production;
— verify or modify the information in the tentative data sheets.

Finally when all processes are under statistical control the order is given for full production to start; data sheets and samples are then made available for customers.

12.2.3 Production and Inspection

Once manufacture is in full swing it is the skill and ability to assess their own efforts in the light of feedback from Inspection and Quality Control

which enables the production personnel to maintain or improve the quality attained in pre-production. This feedback takes the form of control charts drawn up from the results of sampling tests performed after each process or group of processes. These charts indicate whether processes are remaining under control or whether corrective action needs to be taken before the quality becomes unacceptable, i.e. before the number of defects is such that the batch is rejected. Inspection is also carried out on incoming parts and materials to establish that their quality is adequate.

The normal rules governing Reduced and Tightened inspection are employed so that unnecessary inspection, with its accompanying high cost, is eliminated. It seems a paradox that the most reliable process often involves the least inspection.

12.3 Final Tests

Once the diodes have been finished and before they are dispatched to the customer they must pass through the final inspection testing procedure. These tests are considered in three groups viz. 100%, Batch Release and Reliability Tests.

12.3.1 100% Tests

As the title suggests tests are conducted by the factory inspector on all diodes to check that the principal electrical and thermal quantities conform to the specification.

With diodes these tests include:

— forward voltage drop (V_F) at maximum repetitive forward current;
— leakage current at elevated temperatures at voltages V_{RWM} and V_{RSM};
— thermal resistance between junction and mounting base;
— reverse recovery charge and switching time, if applicable;
— reverse breakdown voltage $V_{(BR)R}$ (for controlled avalanche diodes);
— reverse power dissipation P_{RSM} (for controlled avalanche diodes).

12.3.2 Batch Release

Each batch (defined as one week's production which has passed the 100% factory tests) is submitted to a second control inspection department which takes samples according to MIL-STD-105. The samples are subjected to the tests listed in sect. 12.3.1. This forms a check that the factory tests have been performed satisfactorily. The diodes are then kept in what can be considered a bonded store.

12.3.3 Reliability Tests (Quality Control)

From the batch in the bonded store samples are taken by Quality Control to have their characteristics measured, then to be subjected to environmental testing and then to have their characteristics measured again. Any change in characteristics caused by the environmental tests is used as a measure of the quality of outgoing batches. Any batch, whose sample yields more defects than permitted by the sampling scheme, is examined to reject faulty devices.

Initial measurement

All devices from the sample are marked for identification and the following measurements made:

— forward voltage characteristic at two temperatures;
— reverse voltage characteristic up to V_{RSM} at room temperature and maximum junction temperature;
— thermal resistance between junction and mounting base;
— thermal resistance between mounting base and heat sink;
— reverse recovery charge and switching time (if applicable);
— reverse breakdown voltage characteristic at room temperature and maximum junction temperature;
— non-repetitive peak forward current I_{FSM} at maximum junction temperature.

In addition to these measurements, a proportion of the sample is checked for dimensions, and visually examined for quality of finished appearance and marking.

Environmental Tests (Quality Control)

Once the results from the above measurements have been recorded the sample is divided into groups and each group subjected to one or more of the following environmental tests: (not necessarily in the order quoted)
thermal shock;
thermal fatigue;
temperature cycling;
robustness of lead (or top electrode) and stud;
mechanical shock or bumping;
long term life under load;
storage.

End of Test Measurements

End-of-Test measurements are then made and, if the results after the first five tests listed prove satisfactory, permission is given for the release of the batch. The diodes can then be dispatched. The last two tests give us information on the long term behaviour of the diodes so that, with high confidence, we can forecast the reliability.

SYMBOLS AND DEFINITIONS

This manual follows the usual practice of appending the abbreviation "max" to a symbol subscript in order to represent device ratings; for example, $T_{j\,max}$ means max. allowable junction temperature. No attempt has been made to include all such maxima in the following list of symbols, and absence from the list does not imply that a given maximum rating symbol will not be used in the manual. All power diode ratings relate to a mounting base-to-ambient thermal resistance not exceeding a specified value under given operational conditions, as shown on the data sheets.

1. Diode Voltages

1.1 Forward

V_F — *Continuous forward voltage* — Value of forward d.c. voltage, at stated junction temperature, as represented in the typical forward characteristic.

V_{FAV} — *Average forward voltage* — Full-cycle average value of forward voltage.

1.2 Reverse

$V_{(BR)R}$ — *Reverse breakdown voltage* — Reverse voltage level, at specified junction temperature, at which a controlled avalanche device will break down due to reverse current avalanching. The device will suffer no damage if the reverse power is kept within its ratings.

V_R — *Continuous reverse voltage* — Vaue of reverse d.c. voltage, as represented in the typical reverse characteristic. A controlled avalanche device will not break down when subjected to max. permissible continuous reverse voltage $V_{R\,max}$.

V_{RWM} — *Crest working reverse voltage* — Crest value of

circuit voltage impressed across the device in reverse direction with the exclusion of repetitive voltage transients due to commutation etc., and non-repetitive voltage transients caused by switching etc. A controlled avalanche device will not break down when subjected to max. permissible crest reverse voltage $V_{RWM\ max}$.

V_{RRM} *Repetitive peak reverse voltage* — Peak value of reverse voltage including repetitive voltage transients but excluding all non-repetitive voltage transients.

V_{RSM} *Non-repetitive peak reverse voltage* — Peak value of reverse voltage including all non-repetitive voltage transients but excluding all repetitive voltage transients.

2 Diode Currents

2.1 Forward

I_F *Continuous forward current* — Value of forward d.c. current as represented in the typical forward characteristic.

i_F *Instantaneous forward current* — Instantaneous value of forward current.

I_{FAV} *Average forward current* — Full-cycle average value of forward current. Rated level $I_{FAV\ max}$ is valid for a specified rectifier configuration, and under specified conditions of frequency and current waveform.

I_{FWM} *Crest working forward current* — Crest value of forward current excluding all transients effects.

I_{FRM} *Repetitive peak forward current* — Peak value of forward current including recurrent transient effects due to commutation, capacitor discharge, etc.

$I_{F\ rms}$ *R.M.S. forward current* — Full-cycle r.m.s. value of forward current.

I_{FSAV} *Non-repetitive average forward current* — Full-cycle average value of forward current under fault conditions.

I_{FSM} *Non-repetitive peak forward current* — Peak value of non-repetitive current waveform. Diode rating $I_{FSM\ max}$ imposes an upper limit on the peak value of a non-repetitive 50 Hz (or 60 Hz) semi-sinusoidal forward current waveform of specified duration, consisting of equal-amplitude current pulses. Each 10 ms (8.33 ms) semi-sinusoidal current pulse occurring in the non-repetitive current waveform must be followed by a 10 ms (8.33 ms) off-period; the non-repetitive current waveform may be preceded and followed by max. rated voltage, current, and junction temperature valid for steady-state operation.

$I_{FS\ rms}$ *Non-repetitive r.m.s. forward current* — R.M.S. value of a single non-repetitive forward current pulse. Diode rating $I_{FS\ rms\ max}$ imposes an upper limit on the r.m.s. value of a single non-repetitive semi-sinusoidal forward current pulse of specified duration (10 ms or less); the non-repetitive current pulse may be preceded and followed by max. rated voltage, current and junction temperature valid for steady-state operation.

2.2 Reverse

I_R *Continuous reverse current* — Value of reverse d.c. current at stated junction temperature, as represented in the typical reverse characteristic.

I_{RM} *Peak continuous reverse current* — Specified maximum value of reverse d.c. current at crest reverse working voltage and specified mounting base or junction temperature.

3 A^2s

I^2t *I squared t* — A^2s content of a single non-repetitive forward current pulse. Diode rating I^2t_{max}

imposes an upper limit on the A^2s content of a single non-repetitive forward current pulse of specified duration (10 ms or less); the non-repetitive current pulse may be preceded and followed by max. rated voltage, current, and junction temperature for steady-state operation.

4 Power Dissipated in Diode

4.1 Forward

P_{tot} — *Average total power* — Sum of forward and reverse power dissipation (max. anticipated value) averaged over a.c. cycle.

4.2 Reverse

P_{RAV} — *Average reverse power* — Full-cycle average value of reverse power dissipated in a controlled avalanche device under recurrent operation in the breakdown region. Diode rating $P_{RAV\ max}$ imposes an upper limit on the average reverse power, at a specified junction temperature, dissipated in a controlled avalanche device under a.c. operation at a specified working frequency in the breakdown region.

P_{RRM} — *Repetitive peak reverse power* — Peak value of a repetitive square power pulse dissipated in a controlled avalanche device under recurrent operation in the breakdown region. Diode rating $P_{RRM\ max}$ imposes an upper limit, for a given junction temperature on the peak value of a repetitive square power pulse of specified duration dissipated in a device under a.c. operation in the breakdown region at a specified working frequency.

P_{RSM} — *Non-repetitive peak reverse power* — Peak value of a single non-repetitive square power pulse dissipated in a controlled avalanche device oper-

ating in the breakdown region. Diode rating $P_{RSM\ max}$ imposes an upper limit, for a given junction temperature on the peak value of a single non-repetitive square power pulse of specified duration dissipated in a device operating in the breakdown region.

5 Diode Resistance

r_{diff} — *Differential resistance* — The first derivative, taken at the rated average forward current level $I_{FAV\ max}$ of the $V_F I_F$-characteristic.

6 Recovery Time

t_{fr} — *Forward recovery time* — Time interval, under specified circuit and voltage waveform conditions, required by the device to attain its state of full forward conduction when switched from reverse to forward biased state.

t_{rr} — *Reverse recovery time* — Time interval, under specified circuit and voltage waveform conditions, required for the device to recover its full capability to withstand rated reverse voltage when switched from forward to reverse biased state.

7 Temperature

T_{amb} — *Ambient temperature* — Temperature of surroundings, commonly used as datum for thermal resistance or transient thermal impedance measurements.

T_j — *Junction temperature* — Instantaneous junction temperature under operating conditions. Diode rating $T_{j\ max}$ imposes an upper limit on average

junction temperature in a device operating in a rectifier configuration, and on peak junction temperature where a forward current flows for only a small proportion of the duty cycle.

T_{mb} *Mounting base temperature* — Temperature measured at the centre or bottom (heat sink side) of one of the hexagonal surfaces under operating conditions. In the case of a flat-base device, the mounting base temperature is the temperature measured at the bottom (heat sink side) of the envelope.

8 Thermal Resistance and Impedance

$R_{th\ j-a}$ *Junction-to-ambient thermal resistance* — Thermal resistance existing between junction and ambient deg C/W.

$R_{th\ j-mb}$ *Junction-to-mounting-base thermal resistance* — Device thermal resistance existing between junction and mounting base deg C/W.

$R_{th\ mb-h}$ *Mounting-base-to-heat sink thermal resistance* — Contact thermal resistance existing between mounting base and heatsink deg C/W.

$R_{th\ mb-a}$ *Mounting-base-to ambient thermal resistance* — Thermal resistance existing between mounting base and ambient (°C/W).

9 Junction Capacitance and Charge

$Z_{th(t)}$ *Junction-to-reference transient thermal impedance* — Temperature rise per unit power dissipation of junction above stated reference point for specified period of time after application of step increase of junction power dissipation with device case or ambient temperature held constant. It is expressed in deg C/W.

C_j Junction Capacitance (μF).

Q_{max}	Maximum stored charge at the device junction, on one diode of a group (μC).
Q_{min}	Minimum stored charge at the device junction, on one diode of a group (μC).
ΔQ	$Q_{max} - Q_{min}$.

10 Electrical Parameters

10.1 Voltages

V_B	Battery voltage.
V_{ch}	R.M.S. value of voltage across line choke.
V_{com}	Drop in rectifier d.c. output voltage due to commutation.
V_L	R.M.S. value of secondary voltage per phase.
$V_{LL} = V_L\sqrt{3}$	R.M.S. value of secondary voltage between phases (three-phase system).
V_{L1}	R.M.S. value of primary voltage per phase.
$V_{LL1} = V_{L1}\sqrt{3}$	R.M.S. value of primary voltage between phases (three-phase system).
V_{PL}	R.M.S. voltage per phase of a.c. supply source.
$V_{PLL} = V_{PL}\sqrt{3}$	R.M.S. voltage between phases of a polyphase supply.
V_O	Average value of rectifier output voltage.
V_{OM}	Peak value of rectifier output voltage.
V_{On}	Nominal rectifier output voltage (average value)
$V_{O\,rms}$	R.M.S. value of rectifier output voltage.
$V_{o\,rms}$	R.M.S. value of ripple components in rectifier output voltage.

10.2 Currents

I_L	R.M.S. value of secondary current per phase.
I_{LL}	R.M.S. value of secondary line current (three-phase system).
I_{LMsc}	Crest value of symmetrical (steady-state) fault current per phase available from transformer secondary.
I'_{LMsc}	Amplitude of first pulse of asymmetric fault current per phase, available at transformer secondary.

I''_{LMsc}	Permissible amplitude of first pulse of asymmetric fault current per phase, that will not damage the diodes.
I_{Lsc}	R.M.S. value of symmetric (steady-state) fault current per phase, available at transformer secondary.
I_{PL}	R.M.S. value of primary current per phase.
I_{PLL}	R.M.S. value of primary line current.
I_{PLsc}	R.M.S. value of symmetric (steady-state) primary fault current per phase.
I_O	Average value of rectifier output current.
I_{OM}	Peak value of rectifier output current.
I_{On}	Nominal rectifier output current (average value).
$I_{O\ \mathrm{rms}}$	R.M.S. value of rectifier output current.
$I_{C\ \mathrm{rms}}$	R.M.S. value of ripple components in rectifier output current.
I_{SM}	Peak inrush current of rectifier system.

10.3 Power

P_{AC}	Active a.c. input power.
P_{app}	Apparent a.c. input power.
$P_O = V_O I_O$	Pure d.c. output power of rectifier.
$P_{On} = V_{On} I_{On}$	Nominal d.c. output power of rectifier.
$P_{O\ \mathrm{rms}}$	R.M.S. output power of rectifier.
$P_{o\ \mathrm{rms}}$	Ripple component in rectifier output power.

10.4 Volt-ampere quantities

VA_{in}	Volt-ampere supplied by a.c. source.
VA_{1n}	Nominal value of transformer primary volt-amperes.
VA_{2n}	Nominal value of transformer secondary volt-amperes.
VA_n	Nominal transformer volt-amperes, $VA_n = (VA_{1n} + VA_{2n})/2$.
VA_{ch}	Nominal choke volt-amperes.
$VA_{n(\mathrm{phase})}$	Nominal value of transformer volt-amperes per phase.

VA_{sc}	Total short-circuit volt-amperes of transformer (all secondary phases shorted).
$VA_{sc(\text{phase})}$	Short-circuit volt-amperes of transformer per secondary phase.

10.5 Resistance and reactance

L_{load}	Inductance of load.
R_{load}	Resistance of load.
R_{Ls}	Overall source resistance per secondary phase (supply resistance + lumped series resistance + differential resistance of diodes).
R_s	Overall source resistance (supply resistance + lumped series resistance + differential resistance of diodes).
R_{sc}	Resistance of shorted circuit.
$X_L = \omega_s L_s$	Leakage reactance per phase as seen from transformer secondary.
$X_{Ladd} = \omega_s L_{add}$	Inductive reactance to be added per phase, to restrict fault current to proper value.
$X_{Lch(\text{sc})} = \omega_s L_{ch(\text{sc})}$	Inductive reactance of line choke under fault conditions.
$X_{LL} = \omega_s L'_s$	Half of leakage reactance between successive phases as seen from transformer secondary (primary terminals shorted).
$X_{sc} = \omega_s L_{sc}$	Inductive reactance of shorted circuit.
Z_{load}	Rectifier load impedance.

10.6 Frequency, phase angle, and time

f_s	Supply frequency.
$\omega_s = 2\pi f_s$	Angular supply frequency.
f_r	Fundamental frequency of rectifier output ripple.
t_{com}	Commutation time.
γ_{com}	Commutation angle (radians).
ϑ	Thyristor control angle (radians).
$\cos \Phi$	Power factor presented to a.c. supply source.
φ	Load phase angle at fundamental ripple frequency.
ζ	Phase angle of shorted circuit.

Ψ	Phase angle referred to preceding positive-going zero transition of a.c. supply voltage.

10.7 Non-dimensional quantities

$F_{F(f)}$	Form factor of diode forward current.
$F_{F(p/av)}$	Peak-to-average factor of diode forward current.
$F_{F(p/\mathrm{rms})}$	Peak-to-r.m.s. factor of diode forward current.
F_{fi}	Form factor of rectifier output current.
F_{fv}	Form factor of rectifier output voltage.
$F_{(p/av)i}$	Peak-to-average factor of rectifier output current.
$F_{(p/av)v}$	Peak-to-average factor of rectifier output voltage.
$F_{(p/\mathrm{rms})i}$	Peak-to-r.m.s. factor of rectifier output current.
$F_{(p/\mathrm{rms})v}$	Peak-to-r.m.s. factor of rectifier output voltage.
$F_{ri} = I_{o\ \mathrm{rms}}/I_O$	Ripple factor of rectifier output current.
$F_{rv} = V_{o\ \mathrm{rms}}/V_O$	Ripple factor of rectifier output voltage.
$F_{Pin} = P_O/VA_{in}$	Utility factor presented to a.c. supply source.
$F_{P1} = P_O/VA_{1n}$	Utility factor at transformer primary.
$F_{P2} = P_O/VA_{2n}$	Utility factor at transformer secondary.
I'_{LMsc}/I_{LMsc}	Offset factor of asymmetrical fault current.
m_1	Number of primary phases.
m_2	Number of secondary phases.
N	Primary-to-secondary turns ratio per phase.
%ripple	$100 \times$ Fundamental r.m.s. load ripple voltage$/V_0$.
x	Per unit transformer leakage reactance relative to d.c. load.
x_{add}	Per unit inductive reactance, relative to d.c. load, which must be added per phase in order to restrict fault current to a safe value.
$x_{ch(sc)}$	Per unit inductive reactance of line choke under fault condition, relative to d.c. load.
$x_{req} = x + x_{add}$	Total per unit inductive reactance per phase, relative to d.c. load, required to restrict fault current to safe value.
δ	Duty factor of square wave pulse waveform.
ε_{com}	Commutation voltage loss referred to average rectifier output voltage at zero load.
η_c	Conversion efficiency of rectifier system (pure d.c. output power over a.c. input power).

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