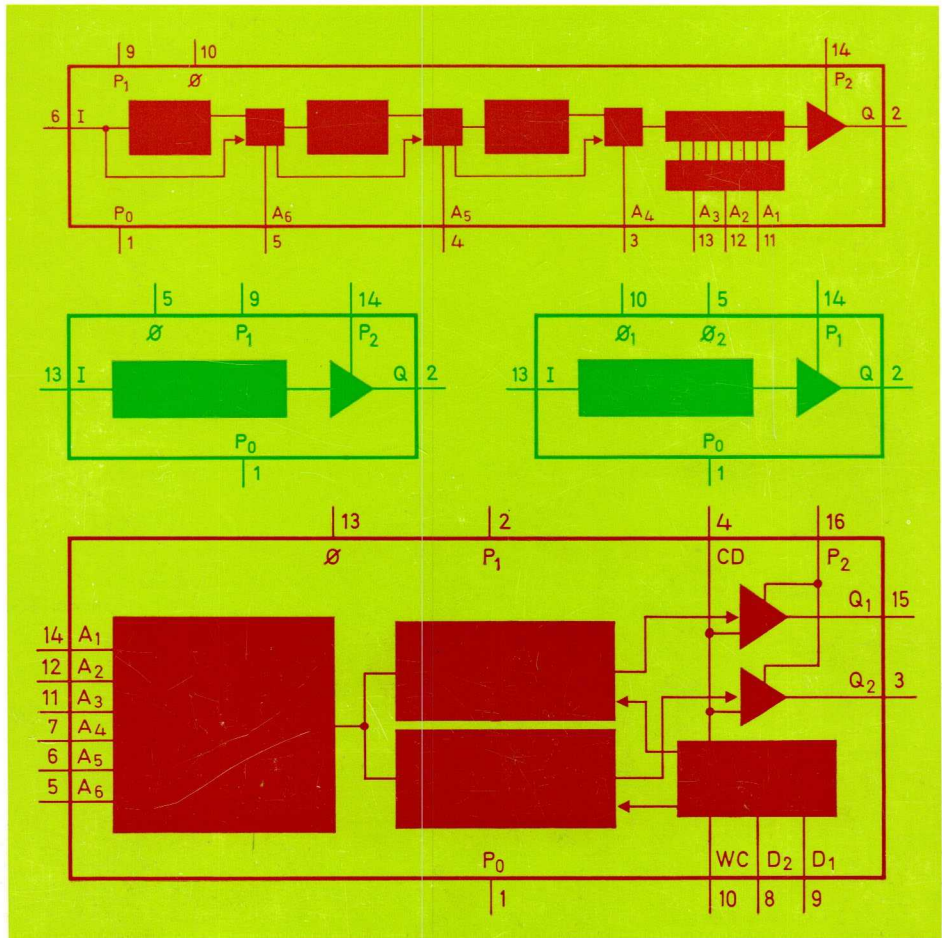


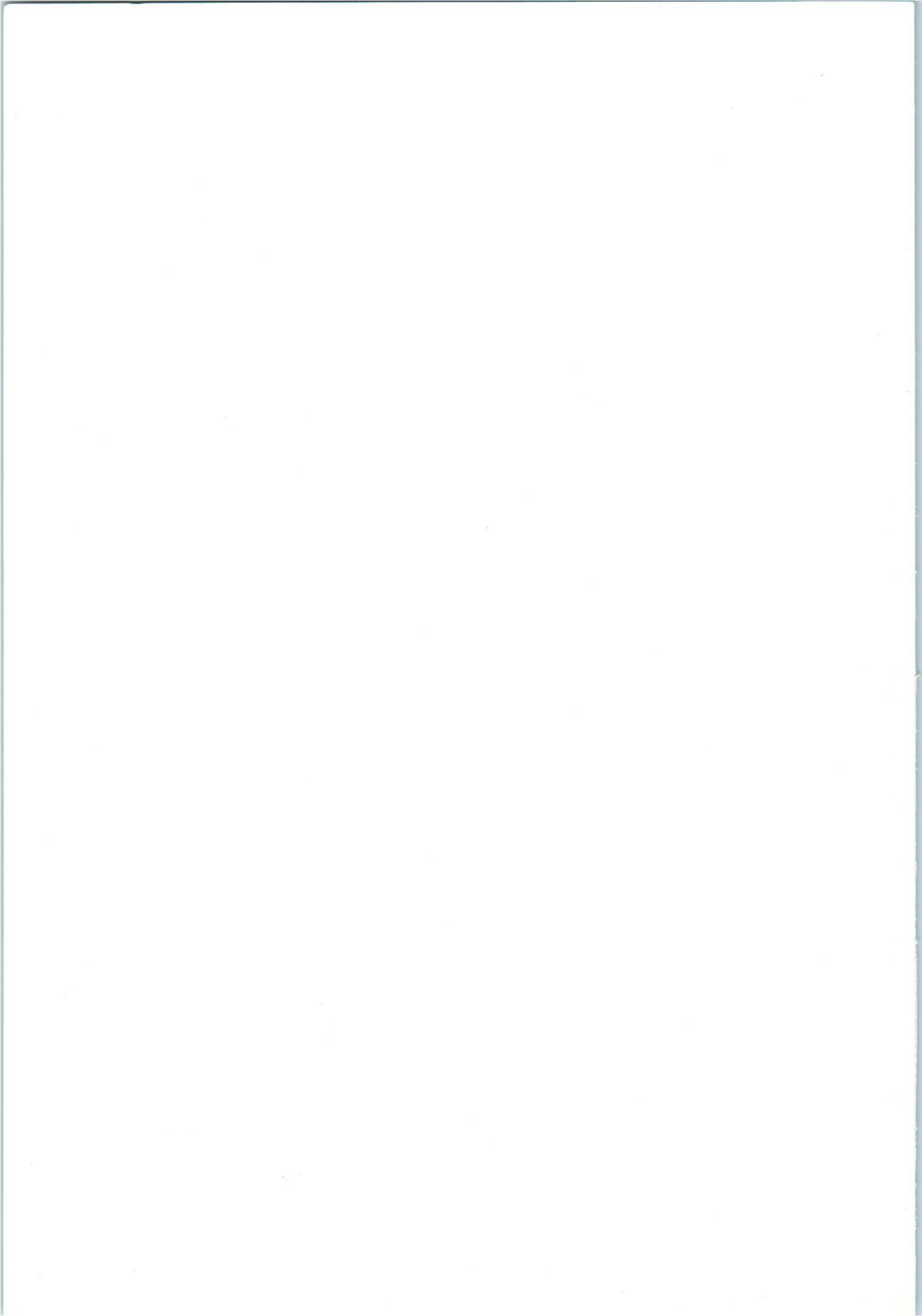
PHILIPS

APPLICATION BOOK

ELECTRONIC COMPONENTS
AND MATERIALS DIVISION

MOS INTEGRATED CIRCUITS AND THEIR APPLICATIONS





61

MOS INTEGRATED CIRCUITS

and their

APPLICATIONS

First published by Mullard Ltd., this book is based on material supplied by B. S. Cowle of the Mullard Industrial Electronics Division and R. J. Hatt, A. E. Jackets, and D. B. Jarvis of Associated Semiconductor Manufacturers Limited. It has been edited by I. N. Nathan of Central Technical Services, Mullard Limited.

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FOREWORD

This book gives users of MOS (metal-oxide silicon) integrated circuits an insight into their working. It is not intended to provide a detailed physical analysis of structure because, from the user's viewpoint, this is as unessential to success as is an understanding of cathode material work-functions to the user of thermionic valves. The description given is a qualitative one, and only factors which directly affect circuit design and use are treated in detail.

EINDHOVEN - The Netherlands

August 1970

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imply a licence under any patent*

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CHAPTER 1

MOS FUNDAMENTALS

INTRODUCTION

Since the introduction of the planar semiconductor manufacturing process, which allowed ICs (integrated circuits) to be made, there has been continual pressure to make devices more and more complex. The demand arises for several reasons, both technical and economic. The technical reasons are mainly as follows.

Size

Smaller units capable of more-complex functions allow the designer to make equipments of greater complexity and versatility, without them becoming cumbersome. Speeds comparable with bipolar circuits can be achieved.

Improved noise immunity

Noise immunity is improved because there is less interconnection wiring.

Easier stabilisation of circuits

Easier stabilisation of circuits is afforded, again because there is less external wiring and capacitance, for example in operational amplifier circuits.

Better system reliability

Better system reliability is achieved, because of the reduced number of potentially troublesome connections due to the higher degree of integration. This is, also, an economic advantage.

Most of the preceding considerations are economic as well as technical advantages to the equipment manufacturer because they result in a reduction of design time and of servicing costs. Other economic reasons

for aiming towards more-complex integrated circuits are as follows:

- easier handling and assembly
- easier testing of equipment
- lower price per function
- simpler fault-location and replacement
- fewer different item types resulting in easier stock handling.

Bipolar IC technology has advanced to a stage where small sub-systems such as counters, shift-registers and adders can be considered as the 'standard' forms of digital integrated circuit. This is so to the extent that devices such as normal gate-packs and JK flip-flops are beginning to be referred to as 'discrete integrated circuits' to distinguish them from the more complex devices. Only a year or two ago this term was unheard of, and the word 'discrete' was reserved for transistors, diodes and ordinary basic components. This gives some indication of the present rate of technical advancement in the IC field.*

The main limitation to increased complexity of bipolar ICs is chip size. As the necessary chip area is increased, cost also increases, and over a certain size, yield begins to fall. The desirable solution therefore is not necessarily to increase chip size, but to use an approach which allows a greater packing density of active devices on present chip sizes. By using the MOS technique this immediately is achieved, for three reasons. Firstly, and most important, the MOS circuits require no isolation diffusions. Secondly, because there are fewer steps in making MOS devices than there are in bipolar circuits (fewer masks and diffusions) the effects of cumulative tolerances are much less of a problem. Thirdly, the individual minimum-size MOS transistor on the chip can be made smaller than the equivalent bipolar device. The upper part of Fig. 1.1 shows an MOS store containing approximately 500 devices, and the lower part a bipolar counter of approximately 70 devices.

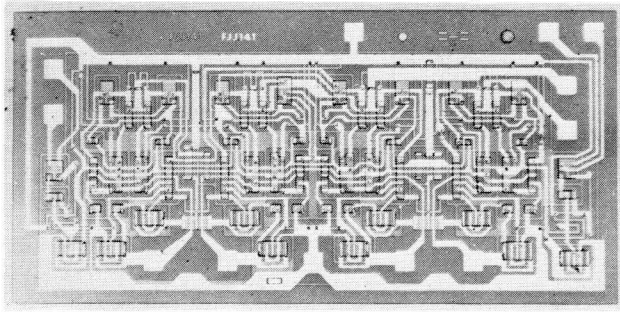
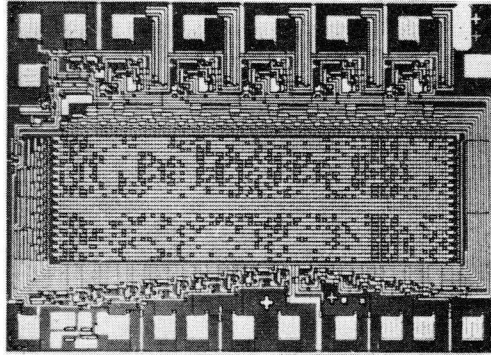
MOS INTEGRATED CIRCUITS

Although the capabilities of MOS devices in large-scale integration have made a great impact on the electronics industry, and will continue to do so, it does not follow that all future IC projects will, or even should, use MOS technology. There is a place both for MOS and bipolar devices, and the suitability of either technique for a particular project must be judged in relation to that project.

Detailed system comparisons show that in some cases MOS is the better choice, in others bipolar provides advantages. Some of the factors

*To avoid confusion, we recommend the use of the term 'simple integrated circuits' rather than 'discrete integrated circuits'.

Fig. 1.1—Comparative packing density of MOS and bipolar devices



affecting choice are system speed, system size (complexity), source of input signals and their voltage levels, required outputs, and the number of pin connections per pack.

The first of these may be a deciding factor on its own, since MOS logic speeds normally are limited to below 5MHz at present, although it is likely that this figure will double in the foreseeable future. However, for system speeds much in excess of 10MHz, bipolar technology must be used.

Small-scale integration is not likely to be economical in MOS form. The input and output requirements may also have a significant effect on the choice. For example, heavy current loads cannot be driven directly from MOS circuits, and if either input or output requirements, or both, are not directly compatible with the MOS circuits, special interface circuits are necessary; the overall cost of the system may favour a bipolar approach.

In cases where few inputs and outputs are needed, but there is a large

amount of logic to be done between input and output, the balance is likely to be in favour of MOS technology.

Standard MOS arrays

Because the individual MOS transistors on a chip are very much smaller than bipolar devices, the amount of logic which can be accommodated on a chip is much greater than can be fitted on a bipolar chip of the same size. Also, because MOS devices are unable to drive capacitive loads, since capacitances of a few picofarads are sufficient to cause significant speed reduction, it is undesirable to enter and exit from the logic chips more often than is absolutely necessary.

These considerations lead to two results. Firstly, individual MOS gate-packs as known in bipolar ICs will not be generally used in large quantities, although more-complex gate arrays may. Secondly, the standard or 'catalogue' items in MOS technology will in general be more complex than the present bipolar higher-order circuits. The most common standard circuits available at present are shift-registers of various types and lengths. The range of devices is also expanding to include multiple decade counters, multi-stage binary dividers, read-only stores or memories (r.o.s. or r.o.m., the latter also being known as n.d. (non-destructive) r.o.m.), and read-write stores.

Other functions which may be considered suitable for production as catalogue items are devices such as multiple binary adders, parallel multipliers, combined counters and stores, and reversible decade counters. Because of the complexity of this type of array the number of general applications is limited, therefore the number of different types of large-scale integrated circuits of this form also will be smaller than available in the less-complex bipolar range.

Custom-built MOS arrays

Where a customer has a large volume requirement for a special MOS circuit to provide a function not covered by items from the standard range, it is possible for this requirement to be satisfied by the semiconductor manufacturer undertaking a special 'customised' development. In this case the system requirements are specified by the user, and close co-operation with the semiconductor manufacturer leads to a final circuit design which is used as the basis for making the necessary layouts and masks for production. Early samples of devices are assessed, and any necessary changes are made before the device is produced at full volume. When considering custom-built arrays it is essential to design the logic in such a way that it uses only standard encapsulations and numbers of pins.

Gate arrays

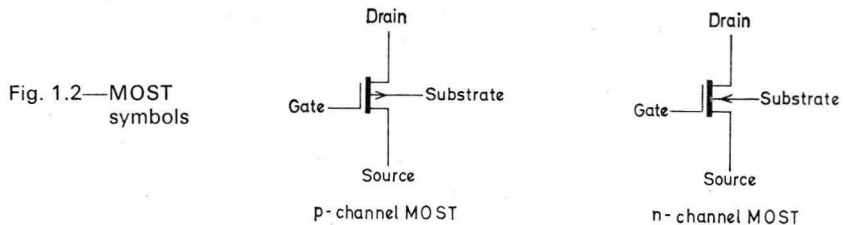
A possible approach to customised design for smaller units and smaller production volume is the use of gate arrays. Here, standard chips are made comprising a matrix of say 64 or 128, or more, gates and these are processed to the stage where the final aluminium interconnection pattern is to be applied. Slices are then held in store at this stage. When customer requirements for medium-scale integration logic functions arise, a suitable aluminium interconnection pattern is designed with the aid of a computer, and a final interconnection mask is made.

Although this approach is flexible enough to be used on relatively small runs, it cannot make optimum use of the available chip area and is not economic for large production runs.

OPERATION OF MOS TRANSISTORS

The MOST is a field-effect semiconductor device. Two basic types of field-effect device are in common use, the J-FET (junction field-effect transistor) and the IG-FET or MOST (insulated gate field-effect transistor or metal-oxide silicon transistor). For large-scale integration purposes it is the second type which is considered.

The MOST is basically a three-terminal device* shown symbolically in Fig. 1.2. The **source** and the **drain** are analogous to the emitter and collector of a bipolar transistor, and the **gate** is the control electrode which is



analogous to the base of a bipolar transistor, except that no input current is required. When a voltage is applied between source and drain, the current flow between these terminals is controlled by the gate voltage.

MOST devices can be operated with either electrons or holes acting as the carriers. It is possible to make devices which conduct when the gate is

*For the purpose of this description the substrate is not considered as an active terminal. The effect of substrate voltages is explained subsequently.

unbiased, and others which require a gate bias to cause conduction.

Devices using electrons as the carrier are known as 'n-channel' and those with positive carriers are 'p-channel'. Those which are normally cut off with zero gate bias are 'enhancement' types, and those which conduct with zero gate bias are 'depletion' types. The cut-off point is referred to as the pinch-off voltage V_P for depletion types and the threshold voltage V_T for enhancement types. Fig. 1.3 shows the regions in which the various types conduct.

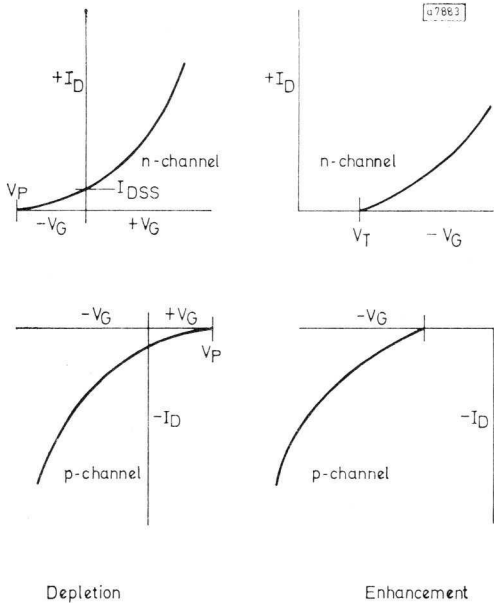
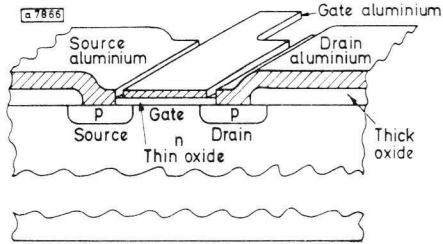


Fig. 1.3—Conduction characteristics of devices

For logic purposes it is necessary to have a device which is normally cut off with the gate at zero, so that the output voltage swing of a previous device can turn it on or off without extra voltage-shifting circuits; therefore, an enhancement type must be used. A p-channel enhancement device is easier to make than an n-channel type, and in general exhibits better stability of characteristics. There are special cases where it is desirable to have both p- and n-channel devices on the same chip but unless otherwise stated all the following applies to p-channel enhancement devices. The cut-off point, as already mentioned, is referred to as the threshold voltage V_T .

The sectional view in Fig. 1.4 shows the effective areas of the device.

Fig. 1.4—Effective areas of MOS device



The structure consists of a heavily-doped n-type substrate. Into this, p-type regions are diffused to form the source and drain areas. The area separating the source and drain areas is covered with a thin oxide, and aluminium is evaporated on top of this with a small overlap on the p-diffusions. This aluminium forms the gate electrode. Contacts are made to the source and drain regions, also by an aluminium deposition.

A more detailed description of the steps in manufacture is given in Chapter 2.

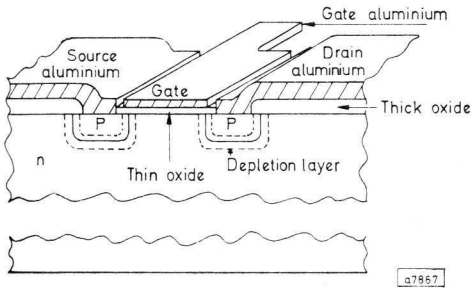


Fig. 1.5—Unbiased MOST

Conduction path in an MOS device

Fig. 1.5 shows the distribution of space-charge forming the depletion layers in an unbiased MOST. Care is taken in manufacture to ensure that there is no unneutralised charge in the gate oxide region, and in the unbiased condition the depletion layer is confined to the p-n junction areas as shown, with little or no distortion at the surface.

When a small negative bias is applied to the gate (with respect to source, and with substrate assumed connected to source and to the common or reference level) electrons are repelled from the surface immediately below the gate region and a depletion layer forms in this area, as shown in Fig. 1.6a. If the negative bias is increased further, the depletion layer deepens and positive carriers (holes) are attracted towards the surface, as shown

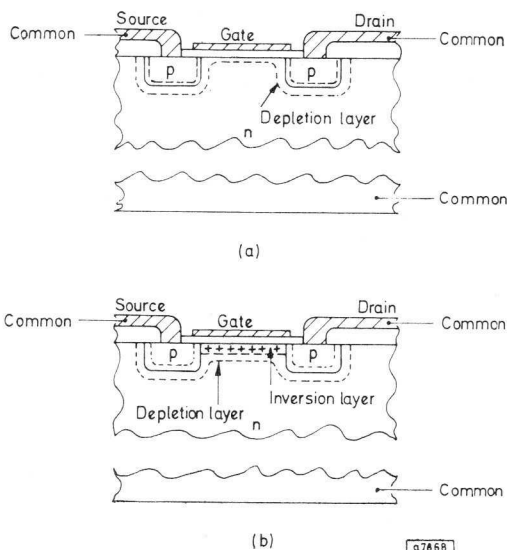


Fig. 1.6—Gate-only biased
 a) slightly negative
 b) further negative

in Fig. 1.6b. These form a p-conduction region or 'channel' below the gate, connecting the source and drain regions. The channel is effectively a p-layer but is formed in n-type material, and is referred to as the 'inversion layer'. The gate voltage at which an inversion layer is just formed is termed the 'threshold voltage'. A more precise definition of threshold voltage can be given in terms of the energy gaps, Fermi levels, and dimensions for the type of structure and doping levels involved but discussion in these terms is beyond the scope of this publication.

When a bias is applied between source and drain, as in Fig. 1.7a, in the presence of an inversion layer, conduction occurs along the channel and since there is a voltage drop along the channel the effective gate voltage falls as the distance from the source increases; thus the depth of the inversion layer also decreases. The depletion layer depth increases at the drain region because of the higher voltage field near the drain. Fig. 1.7a shows the condition at pinch-off or at the threshold level, where the gate and drain voltages are equal, and both greater than V_T . Fig. 1.7b shows the effect when the gate voltage is greater than the drain voltage. The channel now is deeper than in Fig. 1.7a. This condition is termed the 'unsaturated state', where channel current is a function both of gate and drain voltages.

In Fig. 1.7c, the drain voltage is greater than the gate voltage, and the voltage drop along the channel due to drain current gives rise to a condition where the channel is pinched-off before the drain is reached;

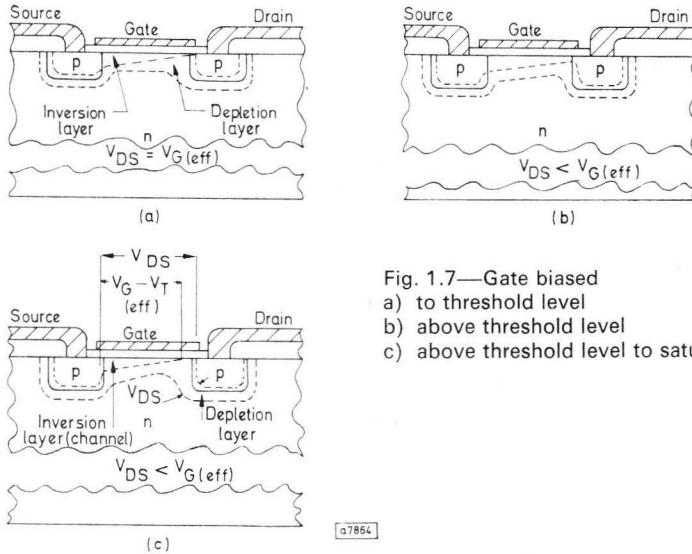


Fig. 1.7—Gate biased
 a) to threshold level
 b) above threshold level
 c) above threshold level to saturation

a current now flows across the depletion layer to the drain. This condition is the 'saturated state', and in this state the channel current is controlled by the gate voltage and is almost independent of drain voltage.

It is important to realise that this pinched-off distance is a very small fraction of the total source-to-drain distance.

As the drain voltage is further increased the channel becomes pinched-off slightly earlier, but because the pinched-off length is not directly proportional to drain voltage, there is a slight increase in drain current with increasing drain voltage.

Gain factor

For fixed drain-to-source voltage and fixed effective gate voltage ($V_{G(eff)} = V_G - V_T$), the main factors affecting the level of current flowing between source and drain, for a given material resistivity, are:

- 1) Drain-source current I_{DS} is inversely proportional to channel length L (shown in Fig. 1.8), that is, the distance between source and drain.
- 2) I_{DS} is also directly proportional to the channel width, that is, the width of the thin oxide region.
- 3) The threshold voltage is directly dependent on the number of surface charge states at the surface of the material. This is a function of the process used, and affects both the thin and thick oxide thresholds as shown in Fig. 1.9.

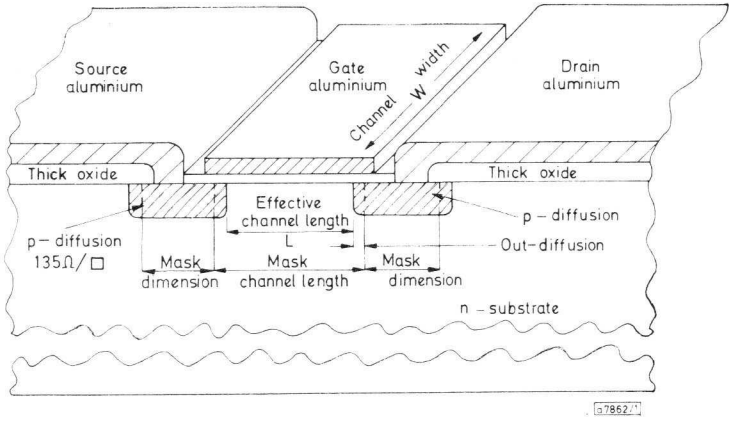


Fig. 1.8—Channel parameters

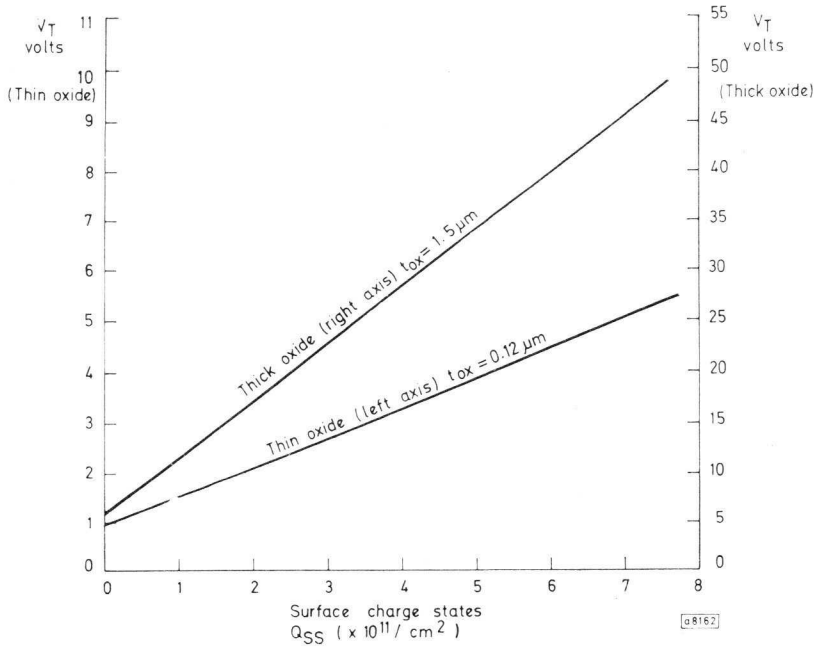


Fig. 1.9—Threshold voltage dependence on surface charge

- 4) As the thickness of the gate-insulating oxide layer is increased the effective field producing the inversion layer penetrates less deeply, and the thickness of the inversion layer is reduced, resulting in reduced drain current, due to higher channel resistance.
- 5) The field is more effective if the dielectric constant of the gate oxide is increased, and I_{DS} then increases proportionally.
- 6) Current and gain are proportional to carrier mobility.

The gain factor β_0 is associated with a particular manufacturing process, and the gain β of a particular device made within that process is $\beta = \beta_0 \cdot W/L$ where W is the channel width, L is the effective channel length, and β_0 is a function of carrier mobility surface states, dielectric constant, and dielectric thickness, and has the dimensions of $I_{DS}/(V_{G(\text{eff})})^2$.

Typical gain factors (β_0) lie between $5\mu\text{A}/\text{V}^2$ and $10\mu\text{A}/\text{V}^2$. The factor β is analogous to the large-signal common-emitter current gain h_{FE} of a transistor or, more accurately, the mutual conductance g_m of a thermionic valve.

Two operating states have been mentioned so far, these being the unsaturated state where drain voltage $V_{DS} < V_{G(\text{eff})}$ (sometimes referred to as the 'triode' region) and the saturated state where $V_{DS} > V_{G(\text{eff})}$. A detailed examination of the device characteristics in these two regions follows the section on device manufacture. At this stage it is sufficient to state that a good approximation to the value of drain current in the two regions is given by the following expressions:

Unsaturated (triode) state, $V_G > V_T > V_{DS}$

$$I_{DS} = \beta \left[V_{DS}(V_G - V_T) - \frac{V_{DS}^2}{2} \right]$$

or

$$I_{DS} = \beta \left[V_{DS}V_{G(\text{eff})} - \frac{V_{DS}^2}{2} \right].$$

Saturated state, $V_{DS} > V_{G(\text{eff})}$

$$I_{DS} \simeq \frac{\beta}{2} (V_G - V_T)^2$$

or

$$I_{DS} \simeq \frac{\beta}{2} V_{G(\text{eff})}^2.$$

CHAPTER 2

MANUFACTURE OF MOS INTEGRATED CIRCUITS

Several MOS manufacturing techniques have been developed, and variants and refinements are introduced from time to time to meet the requirements of particular devices. The present chapter describes a simplified deposition process; the dimensions and values quoted should therefore not be used for design.

The starting point for manufacturing an integrated circuit is a specification. This is converted into a circuit diagram which is subsequently converted into a large-scale layout of the final MOS chip surface. From this, a number of photographic masks for the various stages are produced, either by a combined computer mask-making process or by a two-stage photographic reduction to the final chip size, and these are used in the various manufacturing steps shown below. This sequence of events is shown diagrammatically in Fig. 2.1. The basic process from this stage

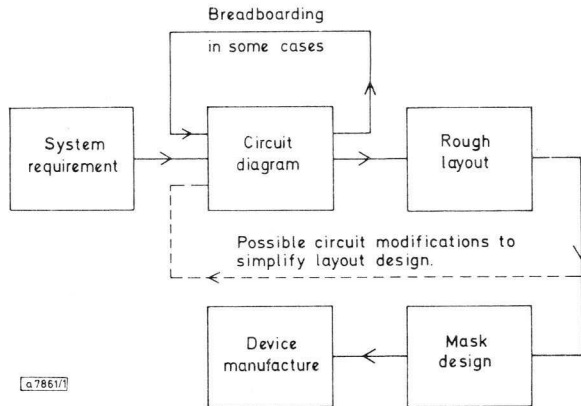


Fig. 2.1—Manufacture of MOS integrated circuits

on is described in Fig. 2.2, although not every detail is included. Variations to produce special features may be added to this basic process; the main steps are shown in Fig. 2.2.

The masks having been produced, the process begins with a slice of 111 oriented monocrystalline silicon, up to 2 inches in diameter, which is used to produce a large number of identical circuits. Instead, 100 oriented silicon may be used but is more difficult to handle and process. The steps given below refer to the 111 process. The slice is first covered with an oxide layer, after which it is covered with a photoresist; the first mask is used, in conjunction with ultraviolet, to define the areas where p-diffusions are required for source, drain and underpass regions. After exposure, the photoresist is removed from these areas and the oxide is etched away. Boron is then deposited, and during the deposition a further glass (oxide) layer grows. This is removed by an acid etch, and the boron is diffused or driven in at a high temperature. Drive-in produces a boron layer about $2\mu\text{m}$ deep. During drive-in there is also a small sideways diffusion resulting in an increase of some $1.5\mu\text{m}$ all round. The next stage is to grow a further oxide layer over the whole slice, giving a total thickness of $1.5\mu\text{m}$.

A second photoresist process is then used to define and etch away all the oxide over the gate areas and contact hole regions. A thin oxide of about $0.12\mu\text{m}$ is grown over these areas, and this is treated to remove undesirable effects such as charge centres.

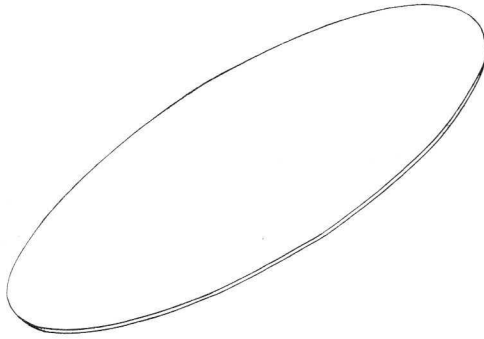
A third photoresist stage defines the contact holes, which are then opened by an acid etch.

An aluminium layer approximately 1 to $2\mu\text{m}$ thick is evaporated over the complete slice, and this is etched by means of a final photoresist stage to produce the gate electrodes, contacts, and interconnection pattern. A section of the resulting device might be as shown in Fig. 2.3.

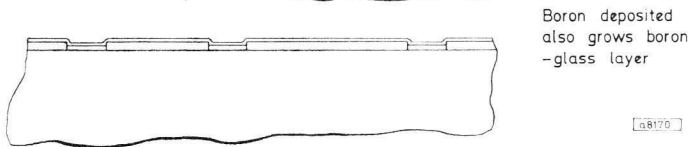
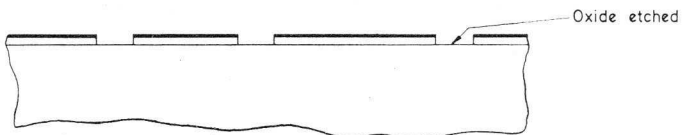
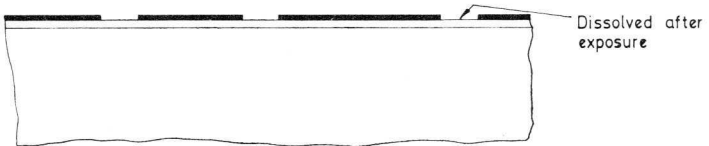
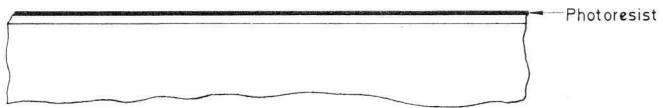
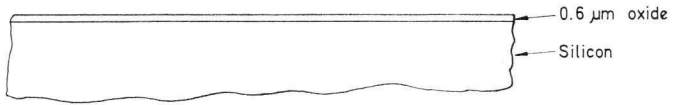
After testing, the slice is cut up into individual circuits, which are encapsulated. These devices undergo a full final test before delivery.

This process gives a thin oxide threshold voltage of between 2.5V and 4.5V. Areas between p-diffusion regions which are covered with thick oxide, over which there is an aluminium layer, could also act as MOS devices. These are known as parasitic MOS devices, and the purpose of thick oxide is to ensure that the threshold level of such parasitic structures is so high that they can never be turned on. The parasitic threshold voltage is over 40V and is in many cases in excess of 60V.

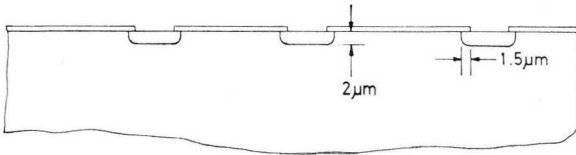
A major difference between the MOS and the bipolar IC process is that in MOS technology there are no isolation diffusions, resulting in a significant economy in chip area. Further, because there is only one diffusion as in bipolar circuits, where the emitter is diffused into the base which



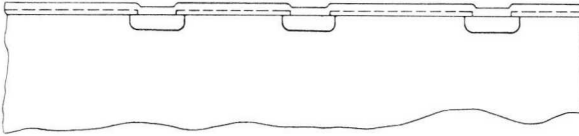
Monocrystalline
silicon, 111
orientation



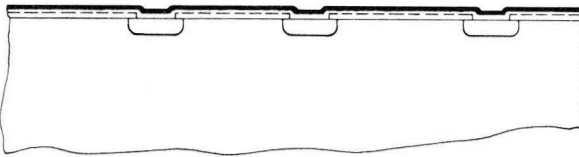
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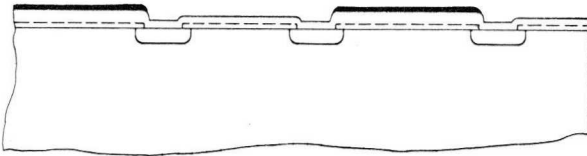
Boron drive-in
after boron-glass
removed



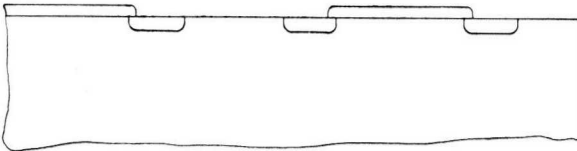
Second oxide layer
to total thickness
of 1.5µm.



Second photoresist

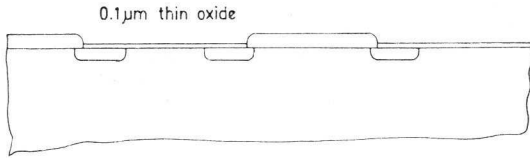


Second photoetch



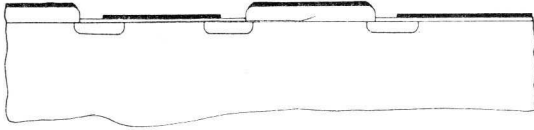
Gate and contact areas
exposed by acid etch

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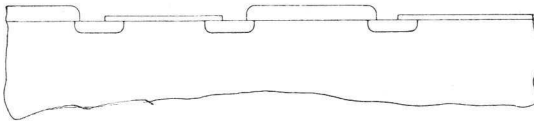


0.1 μ m thin oxide

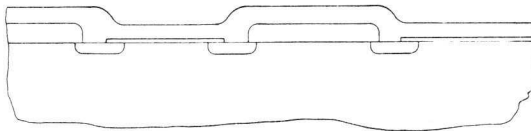
Thin oxide grown
0.1 μ m



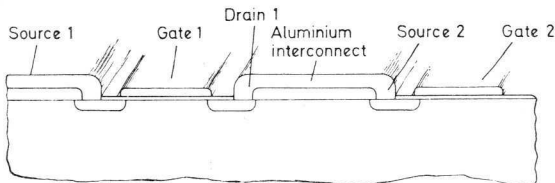
Photoresist process
in thin oxide to expose
contact holes



Photoresist
contact holes etched
and photoresist removed



Aluminium deposited



Aluminium contact
pattern etched after
fourth photoresist

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Fig. 2.2—Basic manufacturing process

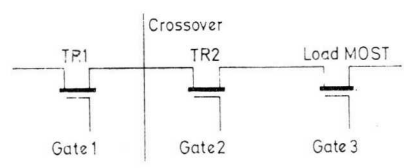
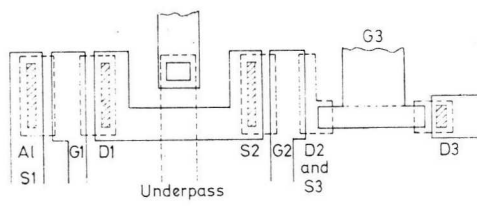
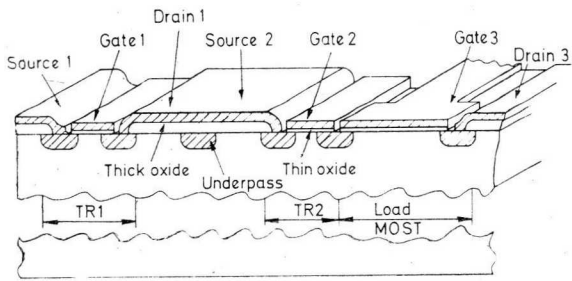


Fig. 2.3—Section of typical MOS device

has itself been diffused into the collector, the problems of cumulative mechanical tolerances are significantly reduced, giving further economy of area. In manufacture, advantage is taken of these factors and, where possible, minimum dimensions are adhered to. The smallest individual MOSTs in common use in integrated circuits have a $10\mu\text{m}$ -square gate region.

Typical packing densities for purpose-designed static logic circuits are some hundreds of devices per mm^2 . The exact figure depends on the ratio of active devices to interconnection aluminium.

CHAPTER 3

D.C. OR STATIC CHARACTERISTICS

As stated previously, two basic characteristic equations define the MOST drain current. While the gate-to-source voltage V_{GS} is below the threshold voltage V_T , no inversion layer exists and no drain current flows.

Unsaturated state (triode region)

When V_{GS} exceeds the threshold voltage, and while the effective gate voltage ($V_{G(\text{eff})} = V_{GS} - V_T$) is less than the drain-to-source voltage V_{DS} , the drain current is approximately:

$$I_{DS} \simeq \beta \left[V_{DS} \cdot V_{G(\text{eff})} - \frac{V_{DS}^2}{2} \right] \quad \dots(3.1)$$

where

$$\beta = \beta_0(W/L). \quad \dots(3.2)$$

Saturated state

When the drain-to-source voltage equals or exceeds the effective gate voltage the device is stated to be saturated. In this condition the voltage drop along the channel is less than the drain-to-source voltage, and the channel falls short of the drain p-region. Conduction very near the drain region occurs across a section of the depletion layer. In this condition the drain current is given by:

$$I_{DS} = \frac{\beta}{2} V_{G(\text{eff})}^2. \quad \dots(3.3)$$

The above equations do not take account of variations in effective channel length due to changes in V_{DS} , nor is the effect of substrate-to-source voltage V_{BS} included. These effects are considered in the more detailed discussion which follows.

Detailed discussion of MOST d.c. characteristics

Fig. 3.1 shows a plot of the drain-source characteristics calculated from the equations stated above, with β_0 assumed to be $7.5\mu\text{A}/\text{V}^2$ and W/L taken as $30/7\mu\text{m}$, giving a β value of $32\mu\text{A}/\text{V}^2$. This represents

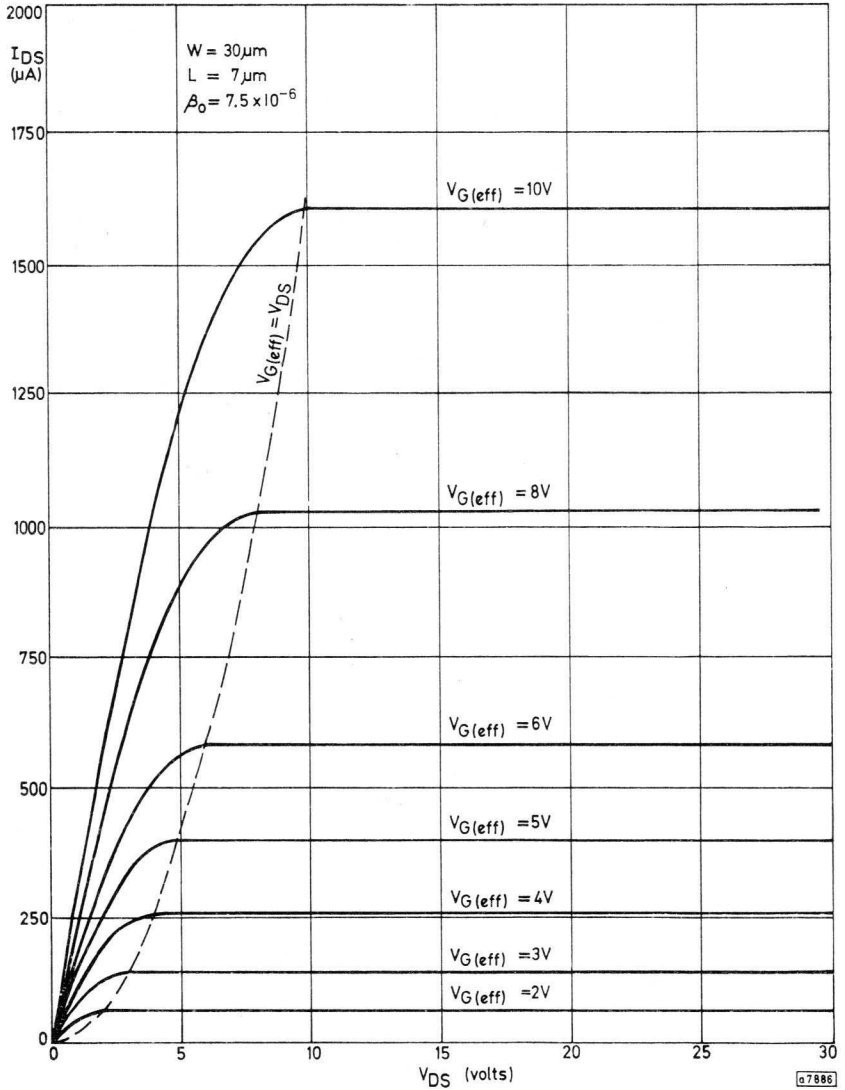


Fig. 3.1—Simplified calculated MOST characteristics

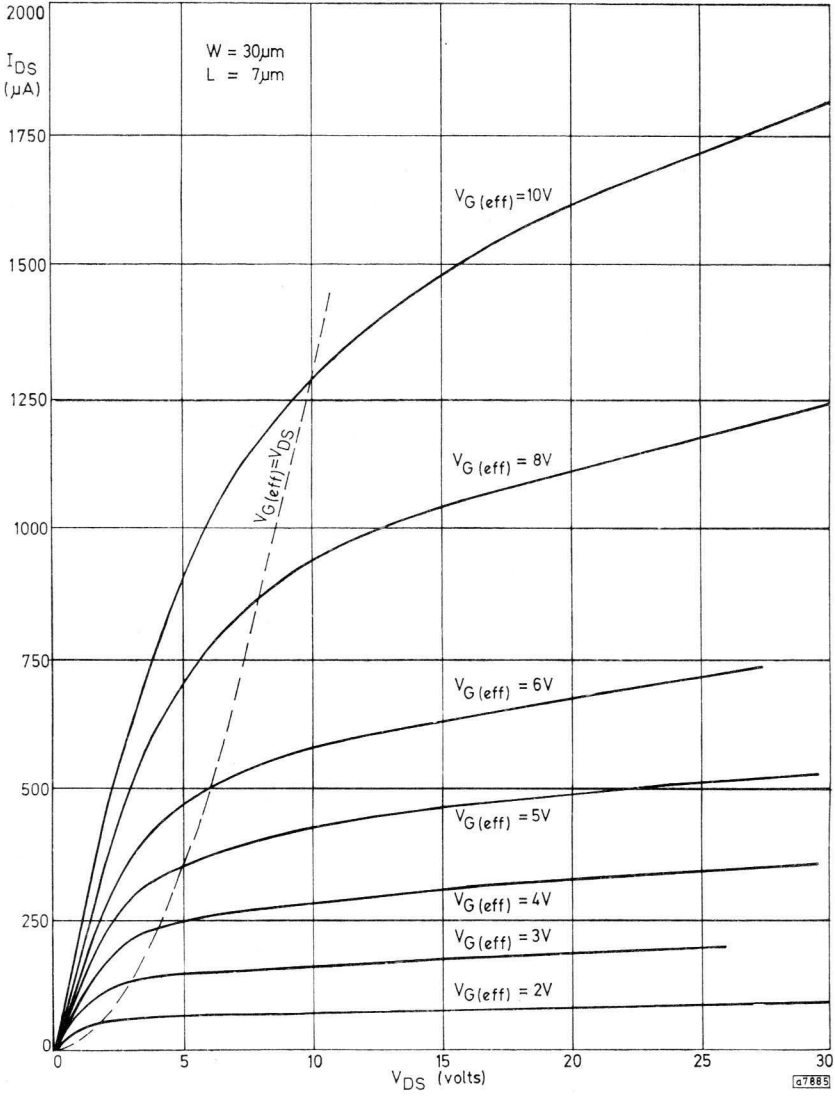


Fig. 3.2—Measured MOST characteristics

$30\mu\text{m} \times 10\mu\text{m}$ on the mask, with $1.5\mu\text{m}$ out-diffusions at source and drain. (A normalised plot of I_{DS}/β against V_{DS} is not valid for comparison purposes because variation in β due to changes in V_{DS} is a function of absolute channel length and not simply of the W/L ratio.) Above the $V_{\text{DS}} = V_{\text{G(eff)}}$ locus the slope of the characteristics calculated in this manner is seen to be zero, representing an infinite output impedance; that is, drain current appears to be independent of V_{DS} . This appears obvious from the equation used to calculate the characteristics because:

$$\frac{dI_{\text{DS}}}{dV_{\text{DS}}} = \frac{d(\beta/2 \cdot V_{\text{G(eff)}}^2)}{dV_{\text{DS}}} = 0. \quad \dots(3.4)$$

In practice this is not so, and other effects must be considered to account for the finite output impedance seen in the practical characteristics given in Fig. 3.2.

As stated earlier, the effective device β is modified by the drain voltage. It is also a function of the effective gate voltage.

For accurate performance calculation, the following equation replaces Eq. 3.2.

$$\beta = \frac{\beta_0}{1 + 0.03 V_{\text{G(eff)}}} \left(\frac{W}{L} \right). \quad \dots(3.5)$$

As the drain voltage is increased, the depletion layer deepens. The result of this deepening is to shorten the effective channel length as V_{DS} increases. In the saturated state, the depletion layer extends to such a distance that the inversion layer does not exist near the drain diffusion. This again results in a shortening of the channel length.

A reduction in channel length increases the W/L ratio thereby increasing β as the drain voltage rises, and this accounts for the finite output impedance in the saturated region. The effective channel length is given by:

$$L = L_0 - \frac{\sqrt{(V_{\text{DS}} - V_{\text{G(eff)}})}}{2} \quad \dots(3.6)$$

in the saturated state (lengths L and L_0 in micrometres) defined as $V_{\text{G(eff)}} < V_{\text{DS}}$, and

$$L = L_0 \quad \dots(3.7)$$

in the unsaturated state (lengths L and L_0 in micrometres) defined as $V_{\text{G(eff)}} > V_{\text{DS}}$, where L_0 is the actual channel length at zero bias (that is, actual separation of drain and source areas).

Modifying Eqs. 3.1 and 3.3 by Eqs. 3.5 and 3.6 gives an accurate representation of device characteristics. Characteristics calculated from these equations are shown in Fig. 3.3 for a device of the same size as

considered previously, that is $30\mu\text{m} \times 10\mu\text{m}$ on the mask ($30\mu\text{m} \times 7\mu\text{m}$ effective size because of $1.5\mu\text{m}$ out-diffusion at source and drain).

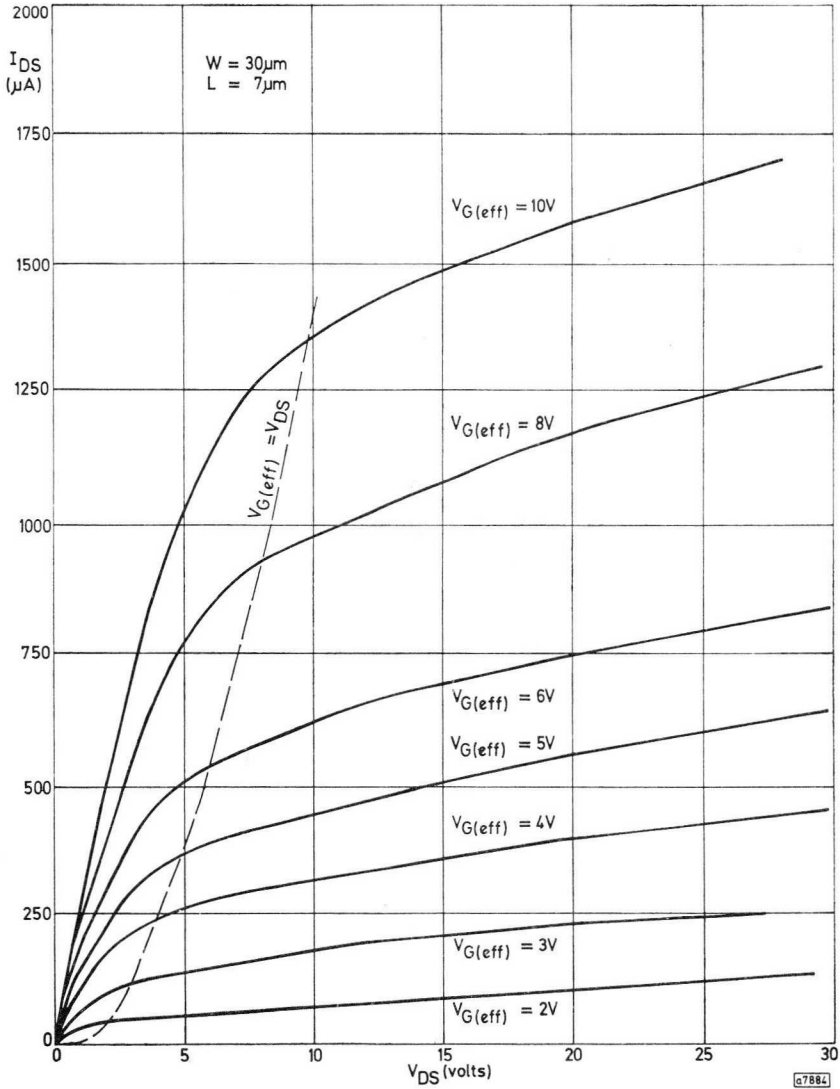


Fig. 3.3—Calculated MOST characteristics using corrected expressions

Output resistance, unsaturated state

Differentiating Eq. 3.1 with respect to V_{DS} gives an output conductance of:

$$G_{DS} = \beta(V_{G(\text{eff})} - V_{DS}), \quad \dots(3.8)$$

giving an output resistance of:

$$R_{DS(\text{sat})} = \frac{1}{\beta(V_{G(\text{eff})} - V_{DS})}. \quad \dots(3.9)$$

As shown in Figs. 3.1, 3.2 and 3.3 there is a difference between the practical output characteristics and those predicted by the simple expression 3.1. For most practical purposes the empirical value of output resistance given below gives sufficient accuracy.

$$R_{DS(\text{sat})} \simeq \frac{L_0 + 3}{\beta(V_{G(\text{eff})} - V_{DS})L_0}, \quad \dots(3.10)$$

where L_0 is in micrometres.

In some cases it may be necessary to add to the value a further contact resistance due to the source diffusion resistance of 100 to 150 Ω /square.

Output resistance, saturated state

Equation 3.3 indicates that I_{DS} in the saturated state is independent of V_{DS} and that therefore the output resistance is in fact as shown in Fig. 3.1.

The modified equation defining I_{DS} in the saturated state including channel length modulation, is:

$$I_{DS(\text{sat})} = \frac{0.5\beta_0 V_{G(\text{eff})}^2 W}{(1 + 0.03V_{G(\text{eff})})(L_0 - 0.5(V_{DS} - V_{G(\text{eff})} + 0.7))^{1/2}}. \quad \dots(3.11)$$

The output resistance derived from this equation is a cumbersome expression:

$$R_{DS(\text{sat})} = \frac{8(1 + 0.3V_{G(\text{eff})})(L_0 - 0.5\sqrt{(V_D - V_{G(\text{eff})} + 0.7)})^2 \sqrt{(V_D - V_{G(\text{eff})} + 0.7)}}{\beta_0 W V_{G(\text{eff})}^2}, \quad \dots(3.12)$$

and Fig. 3.4 shows values calculated from this expression for various sizes of MOS device.

The slope resistances determined above are of importance in designing charge-transfer MOSTs and output interface circuits. Both of these topics are discussed in later sections.

Effect of substrate voltage on threshold voltage

As seen in a previous section, all devices comprising an MOS IC are made on a common substrate. As a result the substrate voltage of all

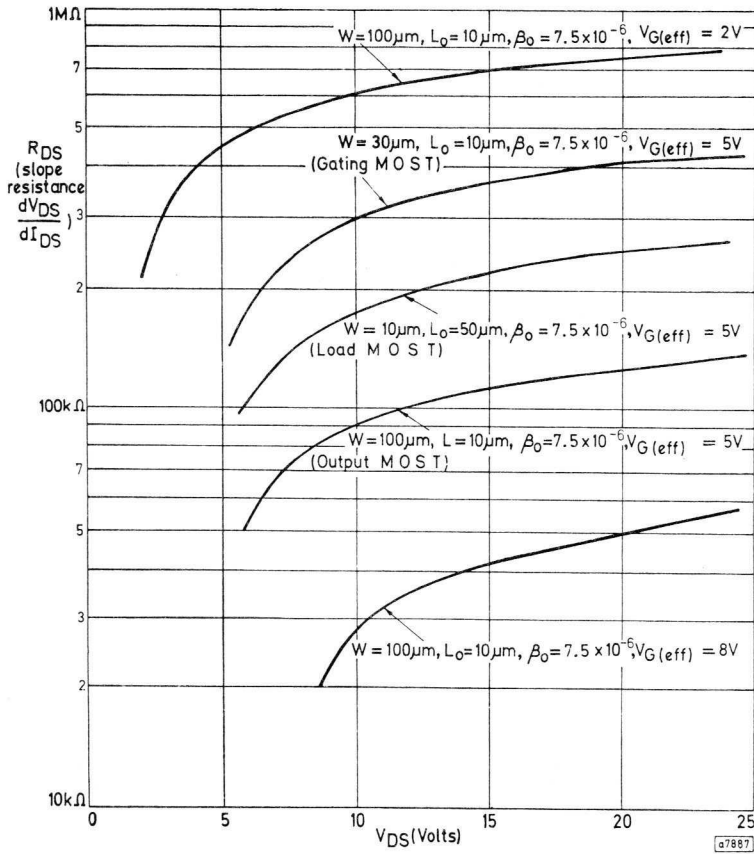


Fig. 3.4—Output drain slope-resistance, saturated state

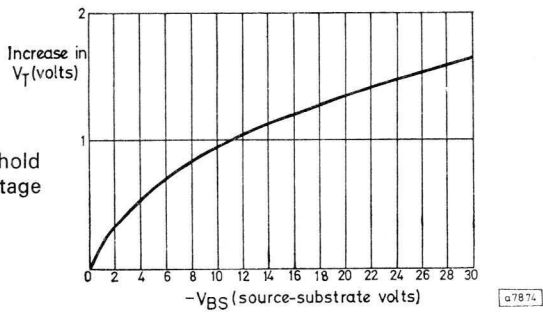


Fig. 3.5—Variation of threshold voltage with substrate voltage

devices is equal. In arranging the devices to form gating functions it is sometimes necessary to connect a number of individual MOSTs in series, resulting in an increase in source-to-substrate voltage in proceeding along the series chain. This has the effect of increasing the effective threshold voltage of devices whose source potential is higher (more negative) than the substrate potential, due to an increase in the depletion layer width. The change in effective threshold voltage is given by the following expression:

$$V_T = V_{T(0)} + 0.75[(V_{BS} + 0.8)^{\frac{1}{2}} - 0.93] \quad \dots(3.13)$$

where V_{BS} is the substrate-to-source voltage, and $V_{T(0)}$ is the threshold voltage with V_{BS} equal to zero. Fig. 3.5 shows the effect of this variation.

CHAPTER 4

THE MOS STATIC INVERTER

The basic circuit used in all logic gates is the simple inverter, shown in Fig. 4.1a. An idealised equivalent circuit of Fig. 4.1a is shown in Fig. 4.1b, where the switching MOST is replaced by a conventional switch.

In the practical case of Fig. 4.1a, a low- β MOST (high resistance) is used as a load resistor, and a high- β MOST (low resistance) is used as the switch. When TR_1 is on, the output voltage is given by:

$$V_{out(low)} = \frac{V_D(R_{DS(1)})}{R_{DS(1)} + R_{DS(2)}} \quad \dots(4.1)$$

where $R_{DS(1)}$ and $R_{DS(2)}$ are the drain resistances of TR_1 and TR_2 respectively. As shown previously, the values of $R_{DS(1)}$ and $R_{DS(2)}$ depend on the geometry and operating conditions of the two devices. Within a single chip the variation of β_0 from device to device is very small (less than 10%) and within a single slice the variation of V_T is less than 150mV.

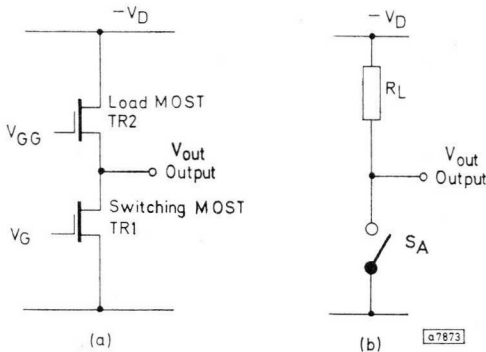


Fig. 4.1—Simple inverter
a) circuit
b) idealized equivalent circuit

As shown in Fig. 4.2a an inverter may be operated with the load MOST gate connected either to the common negative supply rail, in which case it remains saturated at all times, or to a more-negative potential than the normal supply so that the load MOST is kept unsaturated. The second condition, shown in Fig. 4.2b, provides greater operating speed as will be seen later, but also higher dissipation for a given output voltage.

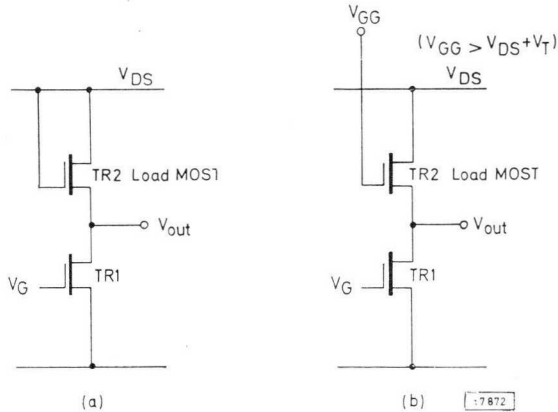


Fig. 4.2—Load MOST gate connected to
a) common negative rail (saturated)
b) more-negative potential (unsaturated)

Output voltage, low state

The low state output voltage of an inverter depends on the relative sizes of the two devices, the supply voltage, and the gate voltages. The output voltage can be calculated by equating the device currents but, even using the simple equations 3.1 and 3.3, the resulting quadratic equation is extremely cumbersome and highly inaccurate. Use of the complete modified equations leads to a solution which can only be usefully handled with a computer; for practical purposes a graphical method provides results which are far more meaningful than the rigorous treatment mentioned above.

In static inverters, the load MOST is a device having a high length-to-width ratio. When considering a long device, the effect of channel-length modulation by drain voltage may be safely neglected. The inverter output voltage is obtained by plotting the I_D/V_D characteristic of the load MOST as a load line on the output characteristics of the gating MOST.

For an inverter such as that shown in Fig. 4.2a, where the load is always saturated and V_S is the supply voltage,

$$\begin{aligned} V_{D(\text{load})} &= V_S - V_{\text{out}} \\ V_{G(\text{eff})\text{load}} &= V_S - V_T - V_{\text{out}} \\ I_{D(\text{load})} &= \frac{\beta_0 V_{G(\text{eff})}^2 W}{(1 + 0.03 V_{G(\text{eff})}) L} \quad \dots (4.2) \end{aligned}$$

$$= \frac{\beta_0 (V_S - V_T - V_{\text{out}})^2 W}{(1 + 0.03)(V_S - V_T - V_{\text{out}}) L} \quad \dots (4.3)$$

For an inverter of the type shown in Fig. 4.2b, V_{GG} is greater than the supply voltage, and the load MOST is unsaturated.

$$\begin{aligned} V_{D(\text{load})} &= V_S - V_{\text{out}} \\ V_{G(\text{eff})\text{load}} &= V_{GG} - V_T - V_{\text{out}} \end{aligned}$$

$$I_D = \frac{\beta_0 (V_D - V_{G(\text{eff})} - V_D^2/2) W}{(1 + 0.03 V_{G(\text{eff})})^4} \quad \dots (4.4)$$

$$= \frac{\beta_0 [(V_{GG} - V_T)(V_S - V_{\text{out}}) + V_{\text{out}}^2/2 - V_S^2/2] W}{(1 + 0.03)(V_{GG} - V_T - V_{\text{out}}) L} \quad \dots (4.5)$$

Load lines plotted from equations 4.3 and 4.5 are shown in Figs. 4.3 and 4.4.

Since in the Fig. 4.2b circuit the load MOST is in the unsaturated state and therefore has a lower channel resistance than the saturated load of Fig. 4.2a, the Fig. 2b circuit will have a higher dissipation than in Fig. 4.2a, for the same supply voltage.

However, by using a lower supply voltage in the circuit of Fig. 4.2b, speed can be increased considerably, compared to that of Fig. 4.2a, without increasing dissipation. This follows directly from the operating conditions. For an unsaturated load MOST the output resistance is low and the load capacitance, which is the major factor in determining speed, is charged rapidly. However, for the same output voltage and drain current the dissipation is proportional to the supply voltage.

Comparison of load line 'b' at 2V output in Figs. 4.3 and 4.4 shows that the dissipation with an unsaturated load circuit and a 15V supply (Fig. 4.4) is $15V \times 120\mu A = 1.8mW$. The dissipation with a saturated load circuit and a 25V supply (Fig. 4.3) is $25V \times 90\mu A = 2.25mW$. However, the output voltage swing of the Fig. 4.3 circuit is lower than that of the Fig. 4.4 circuit, resulting in a higher switching speed in spite of lower dissipation.

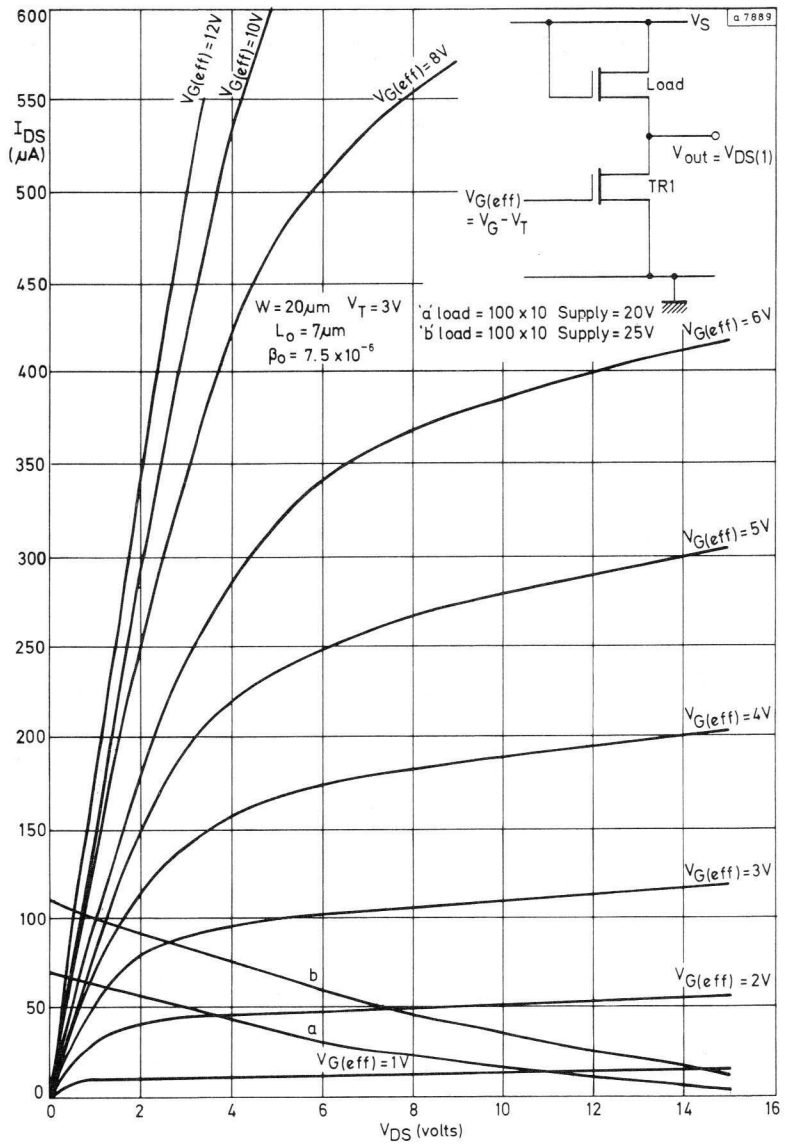


Fig. 4.3—Load lines of static inverter gating MOST, saturated load

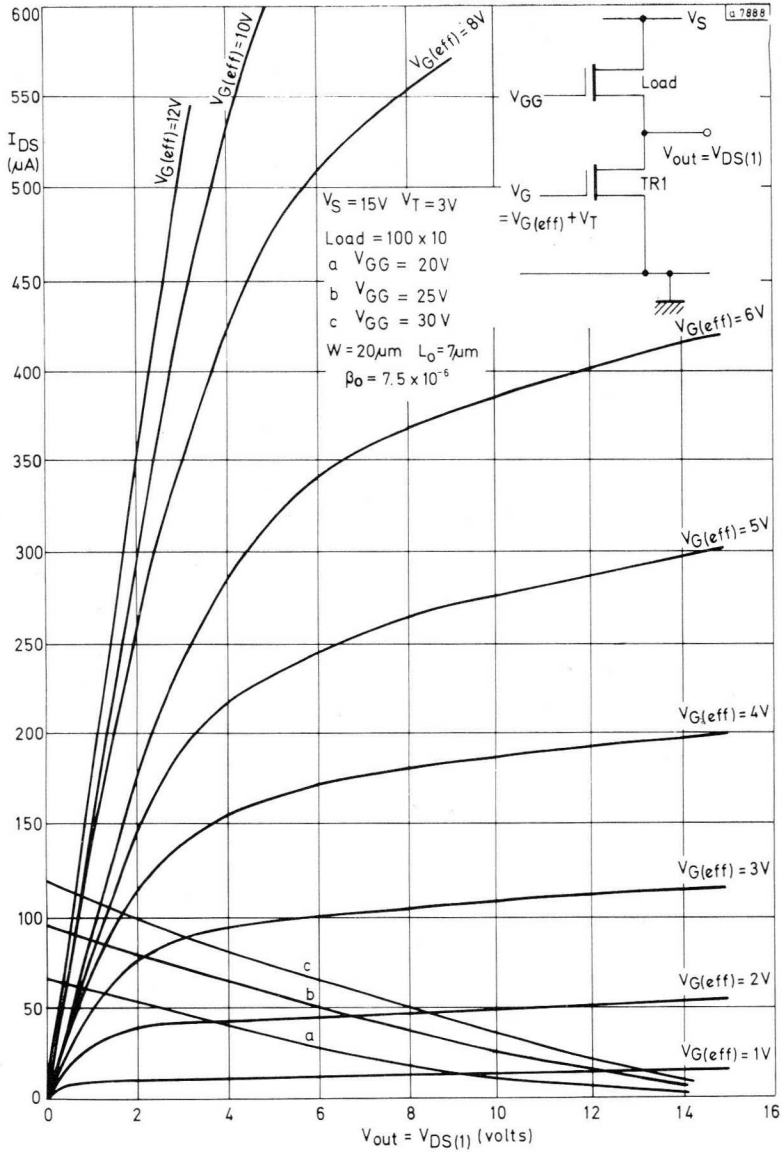


Fig. 4.4—Load lines of static inverter gating MOST, unsaturated load

It is interesting to note that the Fig. 4.3 circuit consists of $50\mu\text{m} \times 10\mu\text{m}$ devices for the load MOSTs plus $40\mu\text{m} \times 10\mu\text{m}$ devices for the driver MOSTs, requiring a total area of approximately $300\mu\text{m}^2$. For the Fig. 4.4 circuit there are $30\mu\text{m} \times 10\mu\text{m}$ devices for the load plus $40\mu\text{m} \times 10\mu\text{m}$ devices for the drive MOSTs requiring a total area of approximately $200\mu\text{m}^2$. The overall areas quoted allow space for source and drain contacts, and clearances.

In an optimised design and with unsaturated loads, the total area required for a device can be reduced by almost half but, as will be explained subsequently, the use of dynamic gating circuits allows a much greater reduction.

Replotting the output voltage of an inverter along the curved load line produces a transfer characteristic of the form shown in Fig. 4.5. To ensure that the output of the inverter is low enough to completely turn off a subsequent MOST, the inverter output must be below the minimum threshold voltage, say -2V , which for the inverter shown in Fig. 4.5 requires an effective gate voltage of at least 4V .

Because of the width of the indeterminate zone of the transfer characteristic it is obviously necessary to have fast rise and fall times of the driving waveforms to maintain good output speed. In bipolar circuits the width of the indeterminate zone is of the order of 100mV , indicating a much higher stage voltage gain which in turn makes it less difficult to maintain high operating speeds.

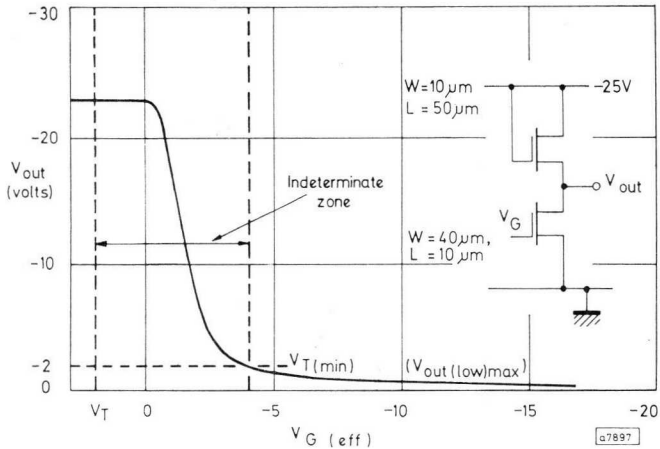


Fig. 4.5—Transfer characteristic of MOST inverter

CHAPTER 5

MOS SWITCHING CHARACTERISTICS

In bipolar circuits the switching characteristics are determined by the turn-on and desaturation times of the transistors, as well as the f_T (transition frequency) and load time-constants. The base drive and source resistance also have a significant effect.

In MOST circuits the intrinsic cut-off frequency is above 1GHz. The maximum operating frequency of large-scale integrated circuits is, however, several orders below this. The reason for this is that during each switching transient, gate and interconnection capacitances must be charged or discharged, and the charge or discharge path is of relatively high impedance.

In discrete MOST or J-FET amplifier circuits this limitation is not normally present because the design of source impedance can usually be tailored to take maximum advantage of the intrinsic device characteristics.

CIRCUIT CAPACITANCES

The most significant circuit capacitances are those associated with the gate electrode, which consists of aluminium over thin oxide, and the capacitance between the interconnection aluminium and the substrate. Although the dielectric of the interconnection capacitance is formed of the thick oxide, giving a much lower value of capacitance per unit area, the total area of interconnection associated with one gate output may be such that this capacitance assumes the greater importance. This condition may arise because of layout problems, and is a significant factor when designing MOS logic layouts. P-diffusions used as interconnection can also add significant circuit capacitances.

Gate capacitance

The gate is effectively a parallel plate capacitor as shown in Fig. 5.1 giving a capacitance value of $C_G = L.W\epsilon_{ox}/t_{ox}$... (5.1)

where ϵ_{ox} and t_{ox} are the dielectric constant and thickness of the thin

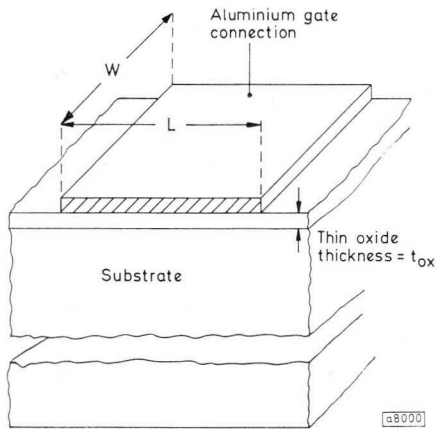


Fig. 5.1—Gate capacitance

oxide layer respectively. With a thin oxide layer $0.1\mu\text{m}$ to $0.12\mu\text{m}$ thick, this expression yields a gate capacitance of:

$$C_G = 3.4 \times 10^{-4} \text{ pF}/\mu\text{m}^2. \quad \dots(5.2)$$

(In calculating the gate capacitance, allowance must be made for the sideways diffusion of the p-regions.)

Interconnection capacitance

The aluminium interconnection also forms a parallel plate capacitance to the substrate, and this has a value of:

$$C_I = 3 \times 10^{-5} \text{ pF}/\mu\text{m}^2. \quad \dots(5.3)$$

Source and drain capacitance

The p-diffusions forming the source and drain electrodes have a capacitance to substrate which depends on the bias voltage between the p-region and the substrate, as well as on the area of the diffusion. This is the normal p-n junction capacitance:

$$C_{pn} = A \sqrt{\frac{q\epsilon_0\epsilon_r N_b}{2V_D}} \cdot \sqrt{\frac{V_D}{V_D + V}} \quad \dots(5.4)$$

where N_b is the background impurity concentration, $V_D = 0.76$, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity. For the process described in Chapter 3 Eq. 5.4 may be expressed as follows:

$$C_{pb} = C_{10} (A + 2.5 P) \sqrt{\frac{10.7}{0.7 + V}} \quad \dots(5.5)$$

where C_{pb} = capacitance between p-diffusion and substrate
 C_{10} = capacitance at 10V bias = 3×10^{-5} pF/ μm^2
 V = reverse bias between p-area and substrate
 A = area of p-diffusion
 P = perimeter of p-diffusion (on mask).

Fig. 5.2 shows a plot of this capacitance against bias voltage for various device sizes.

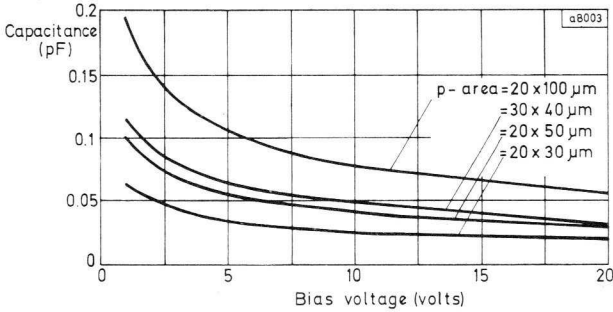


Fig. 5.2—Capacitance between p-diffusion and substrate

SWITCHING TIMES

Rise-time—Case 1, saturated load MOST

Fig. 5.3a shows the circuit of a MOST inverter. The equivalent circuit for the case where TR_1 is turned off is shown in Fig. 5.3b. The total output, gate, and interconnection capacitance is represented by C , and since for a step input function the channel current of TR_1 is turned off immediately the gate voltage V_G is made positive, this is equivalent to

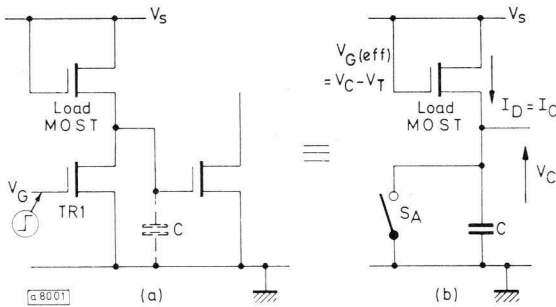


Fig. 5.3—Equivalent circuit of MOST inverter for rise-time calculation (saturated load)

opening switch S_A in Fig. 5.3b.

The effective gate voltage of the load MOST is

$$V_{G(\text{eff})} = V_S - V_T - V_C \quad \dots (5.6)$$

where V_S is the supply voltage, V_T is the threshold voltage, V_C is the voltage across the capacitance, giving a drain current level (using the simple expression) of:

$$I_{DS} = \frac{\beta}{2} V_{G(\text{eff})}^2$$

$$I_C = \frac{dV_C}{dt} \quad (\text{where } I_C \text{ is the current through the capacitance})$$

$$I_{DS} = I_C = C \frac{dV_C}{dt}.$$

Therefore,

$$\frac{dV_C}{dt} = \frac{\beta}{2C} (V_S - V_T - V_C). \quad \dots (5.7)$$

From this,

$$V_{C(t)} = \frac{(\beta t / 2C) (V_S - V_T)^2}{1 + (\beta t / 2C) (V_S - V_T)}. \quad \dots (5.8)$$

Since $V_S - V_T$ is the final value at $t = \infty$, Eq. 5.7 may be written in the normalised form:

$$\frac{V_{C(t)}}{V_{\text{fin.}}} = \frac{(\beta t / C) V_{\text{fin.}}}{2 + (\beta t / C) V_{\text{fin.}}}. \quad \dots (5.9)$$

Fig. 5.4 shows a comparison between the voltage/time curve for a capacitor charged by a saturated load MOST and the same capacitor charged through a fixed resistor of value $1/g_m$, to the same final voltage. The value of g_m is $\beta V_{G(\text{eff})}$. The $V_{G(\text{eff})}$ is in fact a varying quantity, but in Fig. 5.4 fixed values of $0.5V_{\text{fin.}}$, $0.4V_{\text{fin.}}$, and $0.25V_{\text{fin.}}$ are shown. The exponential curves show different rates of rise from those of the saturated load MOST case, but give a reasonable approximation with $R = 1/g_m = \beta V_{\text{fin.}}$.

In load MOST calculations the effects of channel length modulation with varying drain-to-source voltage need not be considered because the variation is insignificant in comparison to the length of devices used as loads.

Rise-time—Case 2, unsaturated load MOST

An inverter circuit using an unsaturated load MOST is shown in Fig. 5.5a. The equivalent circuit for analysis is shown in Fig. 5.5b.

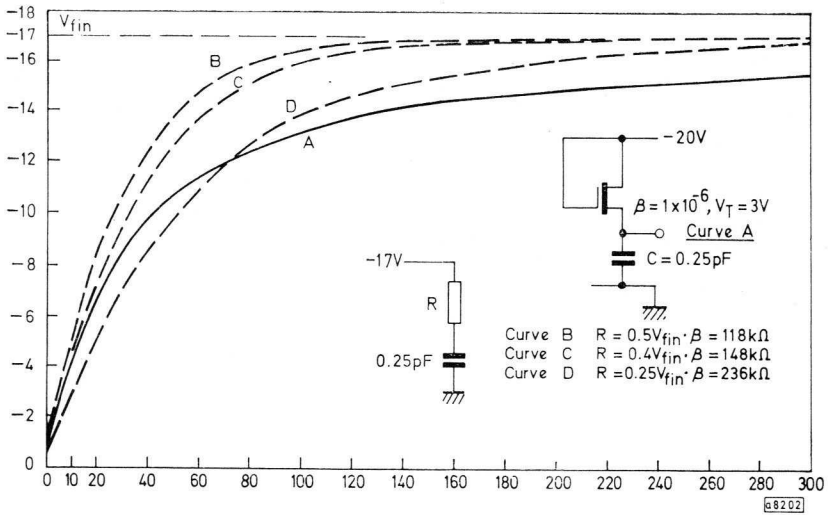


Fig. 5.4—Rise-time (in nanoseconds) for saturated load MOST

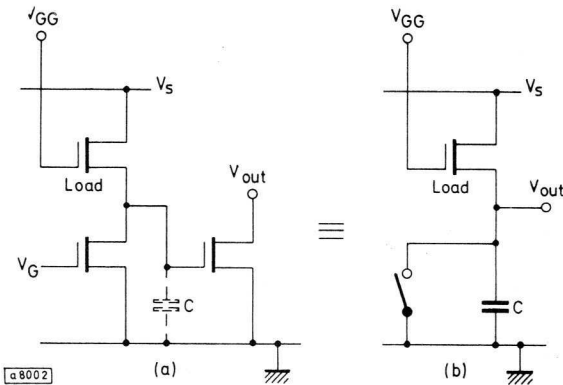


Fig. 5.5—Equivalent circuit of MOST inverter for rise-time calculation (unsaturated load)

The drain current of the load MOST in the unsaturated state is given by:

$$I_{DS} = \beta[V_{G(\text{eff})} \cdot V_{DS} - (V_{DS}^2/2)]$$

where

$$V_{G(\text{eff})} = V_{GG} - V_T - V_C$$

and

$$V_{DS} = V_S - V_C.$$

As before, equating the capacitor current to the drain current gives:

$$dV_C = I_{DS}/Cdt$$

or

$$\int_0^{V_C} dV_C = \int_0^{V_C} I_{DS}/Cdt.$$

From this,

$$\int_0^t \frac{\beta}{C} = \frac{\beta t}{C} = \int_0^{V_C} \frac{dV_C}{(V_{GG} - V_T - V_C)(V_S - V_C) - \frac{1}{2}(V_S - V_C)^2} \dots (5.10)$$

which results in

$$\frac{V_C(t)}{V_S} = \frac{\{1 - \exp[-(\beta t/C)(V_{GG} - V_T - V_S)]\}}{1 + \frac{V_S \exp[-(\beta t/C)(V_{GG} - V_T - V_S)]}{V_S - 2V_T - 2V_{GG}}} \dots (5.11)$$

Note that V_S is the final value in this case.

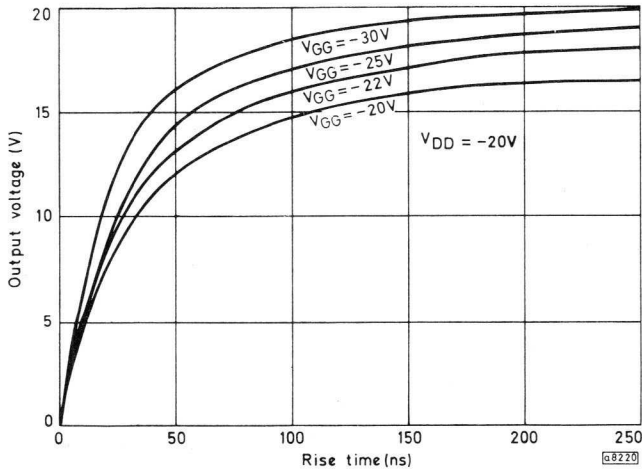


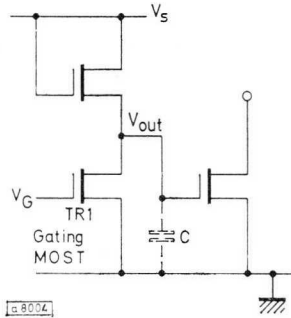
Fig. 5.6—Effects of varying V_{GG}

A family of curves is shown in Fig. 5.6 illustrating the effects of varying V_{GG} , and comparing the unsaturated load case with the saturated load case. Switching speeds calculated from Eq.5.11 are of particular relevance when considering the operation of the dynamic logic circuits described in later sections.

TURN-ON SWITCHING TIMES

The turn-on characteristic of a MOST consists of two distinct parts. As the gating MOST of an inverter (Fig. 5.7) begins to turn on, it is, normally, initially in the saturated state. Capacitor C is initially charged to a voltage V_{CO} , the OFF state voltage of the inverter. Transistor TR_1 is then turned on and the capacitor is discharged. Eventually a point is reached when $V_{DS} = V_{G(\text{eff})}$. From this point on, the device is in the unsaturated state.

Fig. 5.7—Inverter



For a simple analysis the equivalent circuit considered is as shown in Fig. 5.8.

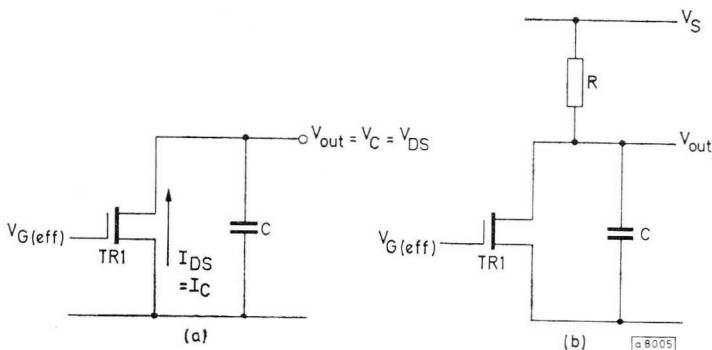


Fig. 5.8—Simple equivalent circuit for turn-on analysis

For the Fig. 5.8a circuit, in the saturated region:

$$V_{\text{out}} = V_{\text{CO}} - \frac{1}{C} \int_0^t I_{\text{d}} dt \quad \dots(5.12)$$

$$= V_{\text{CO}} - \frac{\beta V_{\text{G}(\text{eff})}^2 t}{2C} \quad \dots(5.13)$$

Thus, from the starting voltage V_{CO} to the limit of saturation, the time in the saturated state is given by:

$$t_{\text{sat}} = \frac{2C(V_{\text{CO}} - V_{\text{G}(\text{eff})}) - V_{\text{T}}}{\beta V_{\text{G}(\text{eff})}^2} \quad \dots(5.14)$$

Equation 5.14 predicts a linear fall in output voltage while the device is in the saturated state. In practice, since the gating device has a finite output resistance, the output voltage fall will not be linear and will be more rapid than Eq. 5.14 predicts. This simple analysis ignores the effects of the load MOST on the switching time, and since this increases the switching time, Eq. 5.14 may be regarded as being sufficiently accurate for most purposes.

In Fig. 5.8b the time in the saturated state is given by:

$$t_{\text{sat}} = \frac{CR \log_e(1 + 2V_{\text{G}(\text{eff})} - V_{\text{S}})}{\beta R V_{\text{G}(\text{eff})}^2} \quad \dots(5.15)$$

Turn-on time, unsaturated state

In the unsaturated state,

$$-dV_{\text{C}} = (I_{\text{DS}}/C)dt$$

$$= \frac{\beta}{C} \left[V_{\text{G}(\text{eff})} \cdot V_{\text{DS}} - (V_{\text{DS}}^2/2) \right] dt \quad \dots(5.15)$$

$$= \frac{\beta}{C} \left[V_{\text{G}(\text{eff})} \cdot V_{\text{C}} - (V_{\text{C}}^2/2) \right] dt \quad \dots(5.16)$$

from which it can be shown that the fall time in the unsaturated region is given by

$$t_{\text{unsat}} = - \frac{C}{\beta V_{\text{G}(\text{eff})}} \log_e \frac{V_{\text{C}}}{2V_{\text{G}(\text{eff})} - V_{\text{C}}} \quad \dots(5.17)$$

For a fall from V_{D} to $0.1V_{\text{D}}$, the time taken is

$$t_{100\% \text{ to } 10\%} \simeq \frac{2.95C}{\beta V_{\text{G}(\text{eff})}} \quad \dots(5.18)$$

Full turn-on time

The full turn-on time is the sum of t_{sat} and t_{unsat} , and from Eqs. 5.14 and 5.18 is given by:

$$t_{\text{ON(tot)}} = \frac{C}{\beta V_{\text{G(eff)}}} \left(\frac{2V_{\text{G(eff)}} - V_{\text{CO}}}{V_{\text{G(eff)}}} - 2.95 \right) \quad \dots (5.19)$$

for a fall time from V_{CO} (saturated state) to $10\% V_{\text{G(eff)}} + V_{\text{T}}$.

The transition from the saturated to the unsaturated state during turn-on is shown in Fig. 5.9a, and the path of the turn-on characteristic for a step input is shown in Fig. 5.9b.

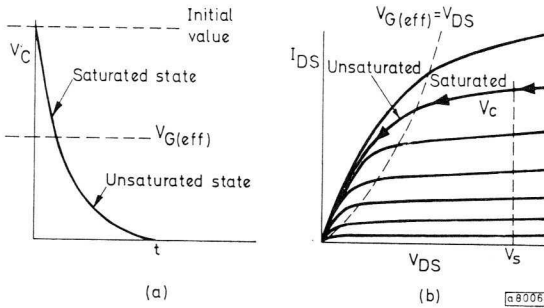


Fig. 5.9—Turn-on

- a) transition from saturated to unsaturated state
- b) path of characteristic for step input

CHAPTER 6

MOS GATE CIRCUITS, STATIC LOGIC

The term 'static' as applied here refers to logic circuits capable of operating at switching speeds down to d.c.

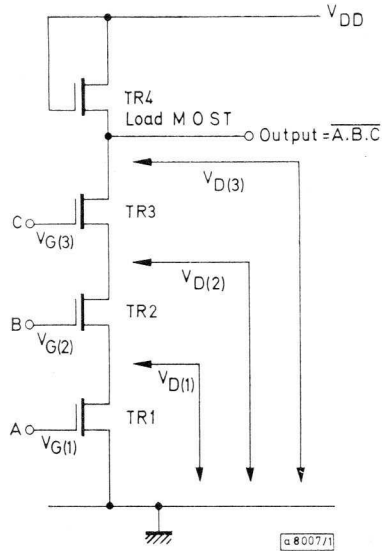
In logic circuits the MOST is used either as a switch or as a resistor. The basic gating element is the static inverter discussed previously in Chapter 4. A modification of the basic inverter to form a NAND gate is shown in Fig. 6.1. The devices TR_1 , TR_2 and TR_3 form the gating elements, and TR_4 is a load device. In Chapter 4 the output voltage of an inverter was shown to be dependent on the gate drive voltage and the device geometry. The ratio of W/L (gating MOST) to W/L (load MOST) is the most important factor in determining the performance of an inverter. Normally, for a simple inverter, this 'ratio of ratios' lies between 20 and 50; for example, a $40\mu\text{m} \times 10\mu\text{m}$ gating device with a $10\mu\text{m} \times 50\mu\text{m}$ load gives a ratio of 20:1.

For a circuit such as Fig. 6.1 to achieve the same low-state d.c. output voltage as the inverter described above, the combined effect of TR_1 , TR_2 and TR_3 must be equivalent to a single device with a W/L ratio of 4 (assuming the load MOST remains unchanged). To achieve this, since the three devices are series-connected, each device must have a W/L ratio of 12. Thus these three devices must each be $120\mu\text{m} \times 10\mu\text{m}$, and such a device could be laid out on the chip as shown in Fig. 6.2a.

When the NAND gate is in the ON state the three devices conduct in series, and there is therefore a build-up of voltage across the gate due to the series resistance of the devices. The effective gate voltage of TR_3 in Fig. 6.1 is therefore slightly reduced as a result of $V_{D(3)}$. This can be compensated by a further increase in the device sizes.

A 3-input NOR gate, such as Fig. 6.3, could be laid out on the chip as shown in Fig. 6.2b. This gate provides the same low-state output voltage as the NAND gate (Fig. 6.2a) but occupies only about half the surface area. Further, each gate oxide area of the input devices is one third of the area of the NAND gate devices, and therefore each device has one third of the gate capacitance of the NAND gate devices. If the two gates were driven

Fig. 6.1—Static MOST NAND gate



from the same type of inverter stage, the NOR gate would respond in one third of the time of the NAND gate response time. Alternatively, for the same operating speed, the driver for the NAND gate would need to provide three times more output current than the NOR gate driver, which would cause increased dissipation.

From the above it is clear that NOR logic has considerable advantages in economics due to reduced chip area, and gives a much better speed/power ratio than the NAND version. The use of MOST elements to generate other gating functions is shown in Figs. 6.4 to 6.9. A NAND-NOR combination is shown in Fig. 6.4. Transistors TR₁ and TR₂ would have twice the width of TR₃ (assuming minimum channel length in all cases) for the same operating speed. A NOR gate followed by an inverter is used in Fig. 6.5 to form the OR function.

If F is held at a logical '1' in Fig. 6.6 the circuit can be used as a NAND gate. Transistors TR₁ and TR₂ form a series AND gate to the gate of TR₅. The inclusion of TR₃ and TR₄ is necessary to remove the accumulated charge when the gate is turned off. In Fig. 6.7 a combined AND-OR input is used, and the function F is applied to TR₄ conditionally, depending on the state of the input gating. Transistor TR₅ is a long (load) device which provides a discharge path for the gate charge of TR₄. Different forms of the exclusive-OR function are shown in Figs. 6.8 and 6.9.

Series gates such as Figs. 6.6 and 6.7 are not generally used in static logic circuits but can be used in the dynamic circuits discussed later.

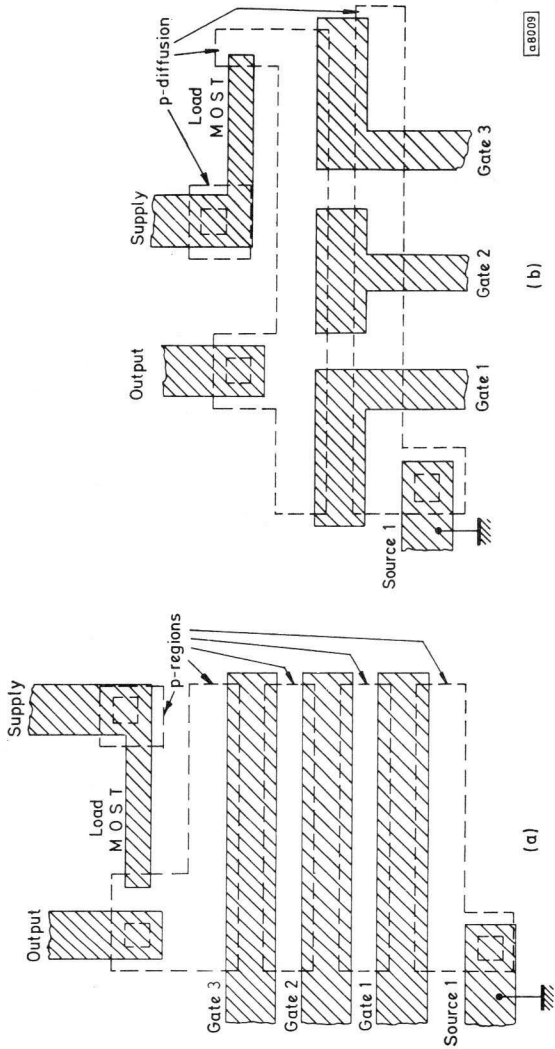


Fig. 6.2—Possible static gate layouts
 a) 3-input NAND gate layout
 b) 3-input NOR gate layout

Fig. 6.3—Static MOST NOR gate

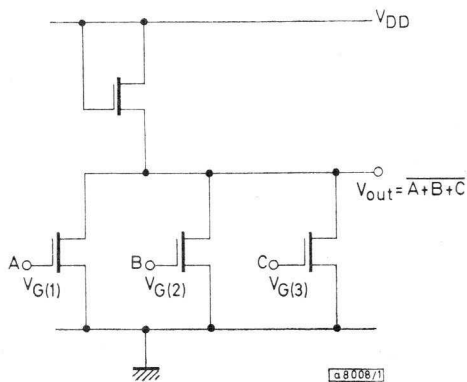


Fig. 6.4—Combined gates

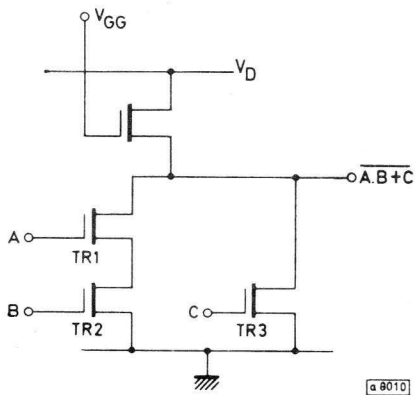
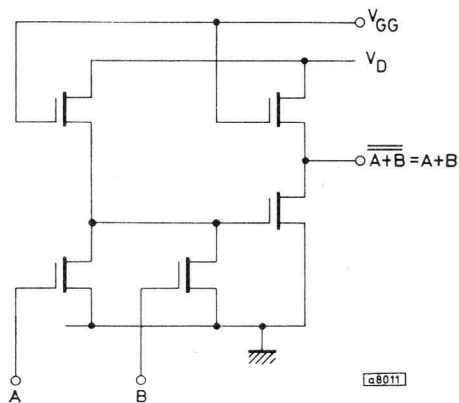


Fig. 6.5—OR gate



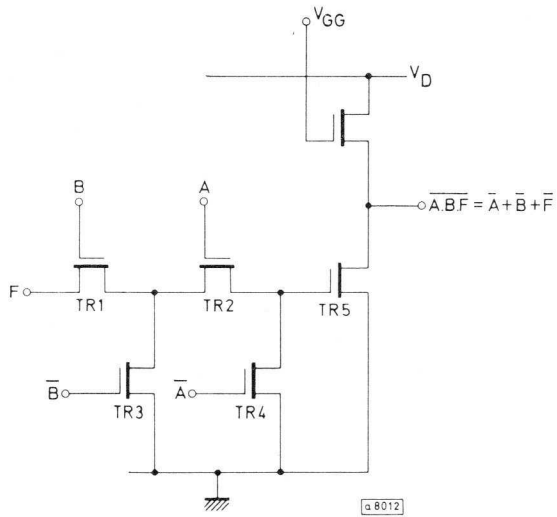


Fig. 6.6—Alternative NAND gate

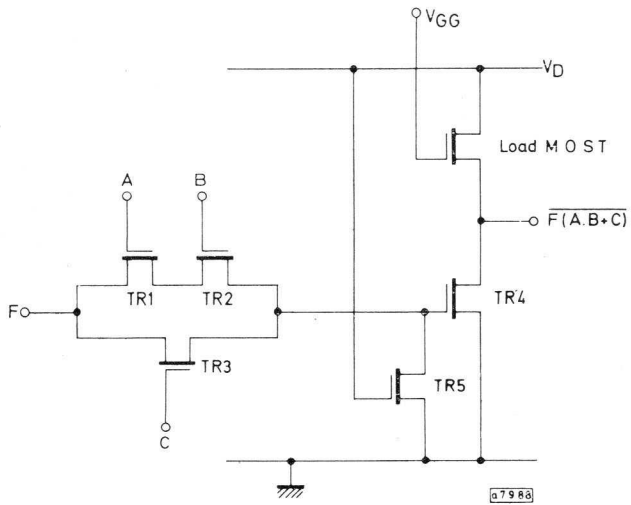


Fig. 6.7—Combined conditional gate

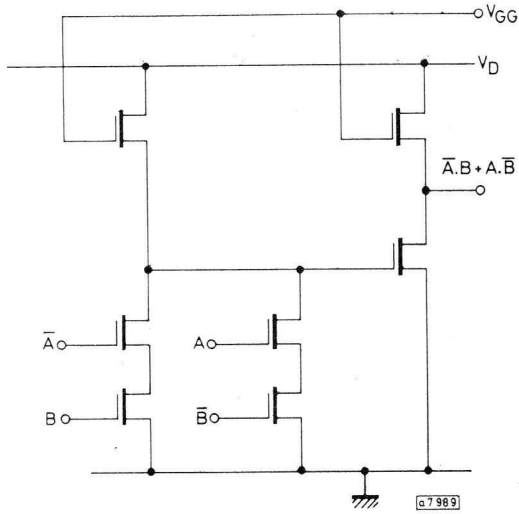


Fig. 6.8—Exclusive-OR gate

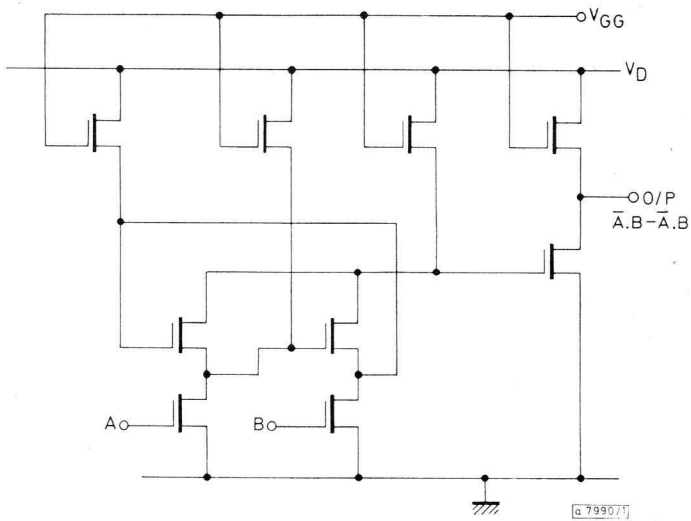
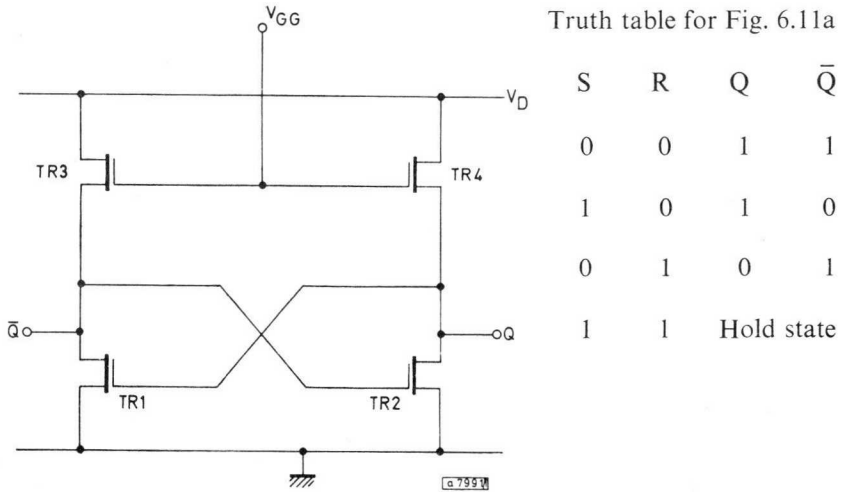


Fig. 6.9—Alternative exclusive-OR gate

STATIC BISTABLES

By cross-coupling inverter circuits as in Fig. 6.10, TR_1 and TR_2 form the driving sections of the inverter. Transistors TR_3 and TR_4 are load devices. Two methods of applying control inputs to the simple bistable circuit by means of TR_5 and TR_6 are shown in Fig. 6.11. These two extra devices would be smaller in the Fig. 6.11a circuit than those in Fig. 6.11b for the same performance. The speed of these bistables is limited by the same factors that set limits to the operating speeds of static logic gates.



Truth table for Fig. 6.11a

S	R	Q	\bar{Q}
0	0	1	1
1	0	1	0
0	1	0	1
1	1	Hold state	

Fig. 6.10—Basic static MOS bistable

STATIC SHIFT-REGISTER, CHARGE STORAGE

The simple bistable element of Fig. 6.10 can, with minor modifications, act as a shift-register stage. Two stages of a long shift-register using this circuit are shown in Fig. 6.12. Transistors TR_3 , TR_4 , TR_8 and TR_9 are cross-coupling devices which can be turned on and off by the clock 1 and clock 2 signals. In stage 1, TR_2 and TR_5 form a bistable with cross-coupling via TR_3 and TR_4 . In the static state the clock signal is absent, and therefore clock 1 and clock 2 are both high (negative) and the cross-coupling transistors are on. To shift information from one stage to the next, the clock line is made high, and data is passed via the coupling transistors TR_1 and TR_6 from one stage to the next. Inputs clock 1 and clock 2 are now low, and the cross-coupling is inoperative so that data can only affect the stage to which it is directly applied.

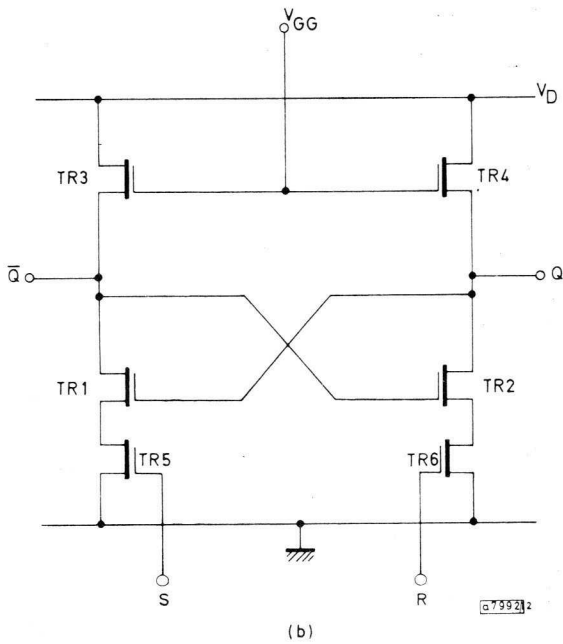
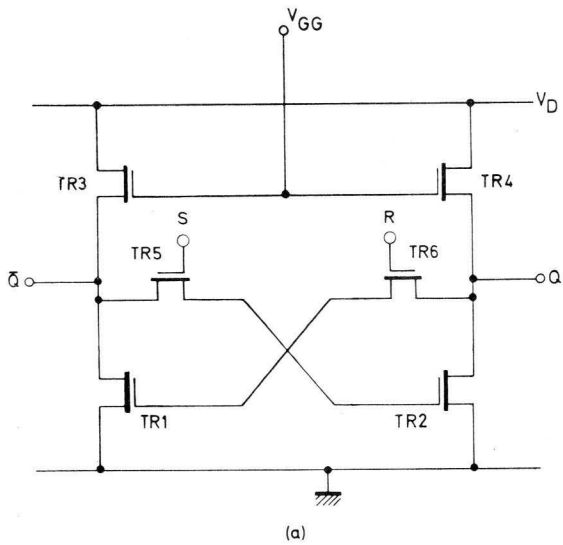
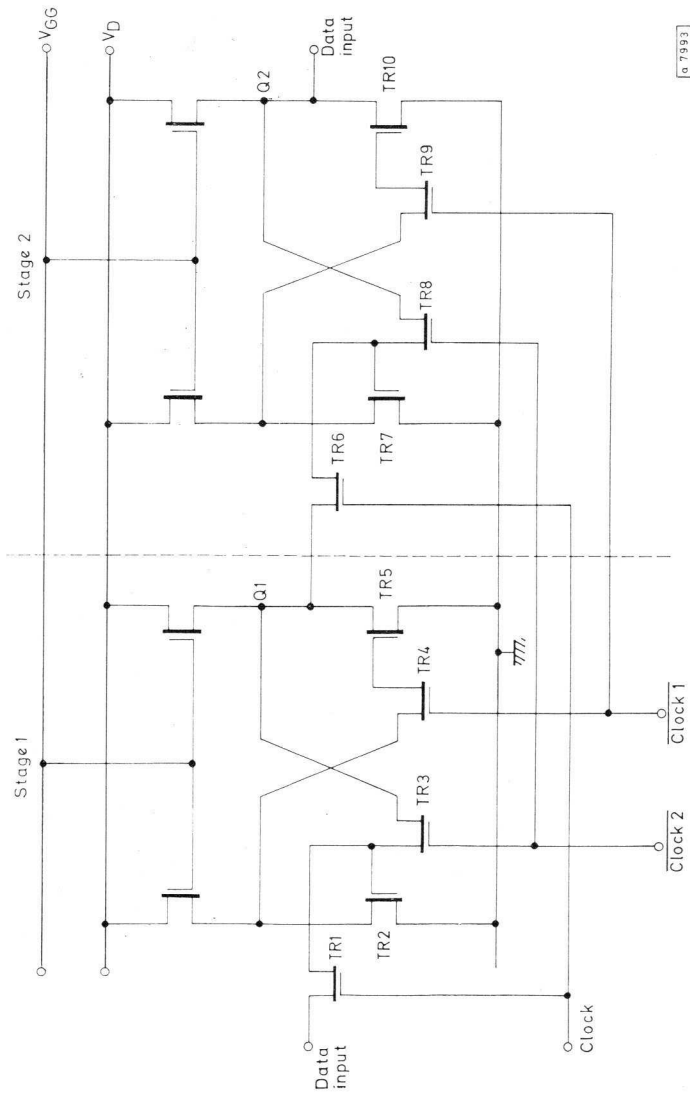


Fig. 6.11—Two methods of applying set and reset inputs to simple RS flip-flop



6 7993

Fig. 6.12—Static CMOS shift-register (2 bits)

While the clock pulse is present the information is held in the bistables in the form of gate charges on TR₅, TR₁₀, etc., and a shift operation must be completed before the charge can leak appreciably, otherwise the information will be lost. When the clock signal is removed, the data input devices are cut off and the transferred data is stored in the gate capacitance of TR₂, TR₇ etc. Data is entered when the clock signal goes negative ('1' state) and appears at the output when the clock signal returns to '0'. To ensure that this data is not reduced in amplitude when clock 1 and clock 2 are taken negative, clock 1 slightly precedes clock 2. The same effect can be achieved by reducing the amplitude of clock 2. A simple method of deriving the required driving waveforms is shown in Fig. 6.13. This generator would normally be incorporated in the MOST shift-register chip. Shift-registers of the type shown in Fig. 6.12 operate at clock rates of up to 1MHz.

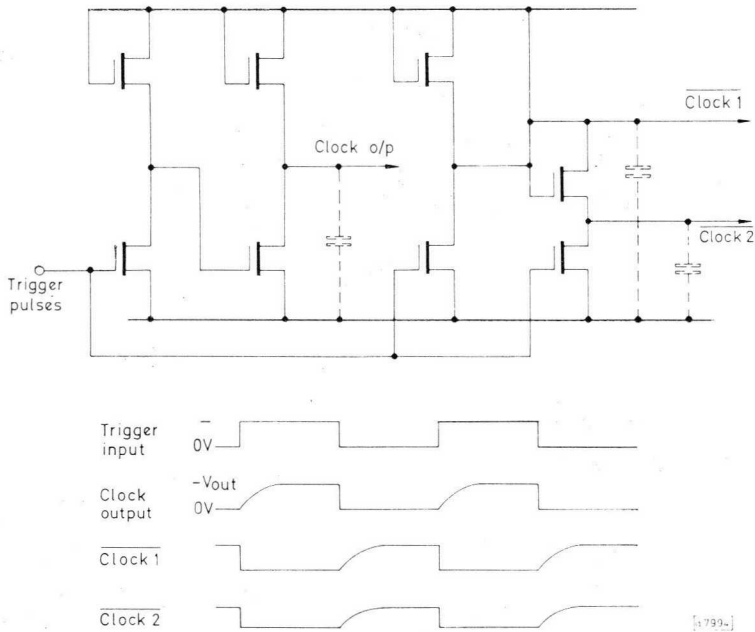


Fig. 6.13—Shift-register clock waveform generator

COUNTING BISTABLE

For use in counting circuits a particular type of bistable element is required. This element changes state at each clock input. Several methods of achieving this function are possible and one well-known circuit is that shown in Fig. 6.14. Transistors TR₁, TR₂, TR₃ and TR₄ form a basic bistable element.

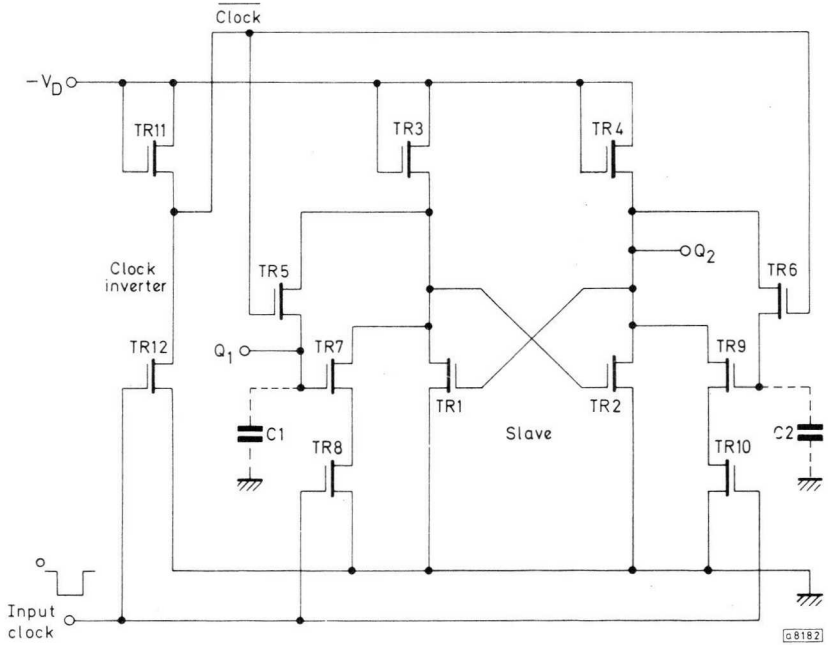


Fig. 6.14—Counting bistable

Transistors TR_{11} and TR_{12} form an inverter for the clock signal. In the normal state, the clock line is at zero and TR_8 and TR_{10} are cut off. Transistors TR_5 and TR_6 are turned on, and the bistable output voltage states are fed to the gates of TR_7 and TR_9 where they charge the gate capacitances of these devices. When the clock line is taken negative, these charge levels are isolated because TR_5 and TR_6 are turned off by the clock inverter. Transistors TR_8 and TR_{10} are turned on.

If Q_1 was negative (1) and Q_2 was at zero (0) before the clock pulse, there will now be a negative charge on C_1 , and C_2 will be discharged. Transistor TR_7 will therefore turn on, and TR_7 and TR_8 in series will pull Q_1 to the zero state. The cross-coupling connection will make Q_2 negative or high. The bistable has therefore changed state. When the clock pulse ends, TR_8 and TR_{10} are once again turned off, and C_1 and C_2 are charged to hold the new state of the bistable in preparation for the next clock pulse.

READ-ONLY STORES

In many systems such as sequential control or small calculators it is necessary to have fixed logic arrays to control data routing, to perform decoding or code conversion, or to store fixed data tables. These functions can be accomplished by the use of r.o.s. (read-only stores) which sometimes are termed r.o.m. (read-only memories). An r.o.s. consists of an array x by y , and at each crossing or address $(x,y)_n$ there is the possibility that there is or is not a transistor depending on whether the particular location contains a '0' or a '1'. In addition it is necessary to provide circuits which can select any desired location in the matrix. This circuitry is an address decoder which is similar to that used with true read-write stores or r.a.m. (random-access memories); the latter are discussed under that heading.

A section of a possible 64-word 1-bit r.o.s. matrix is shown in Fig. 6.15 but the decoding circuits are not shown. When no address signal is present, output lines $o/p_{(1)}$, $o/p_{(2)}$, etc., are all high. Transistors TR_0 , TR_1 , TR_2 , etc. are therefore in the ON state and the output bit line is low. When a row and column location is addressed by the input lines, if it contains a device that device will be turned on and the associated output line will become low, making the output bit line high (a '1' output). If the location contains no device then the output bit line remains low, indicating a '0' output. Stores such as this can be assembled to form longer words. For example, eight such stores addressed in parallel would provide a 64-word 8-bit memory.

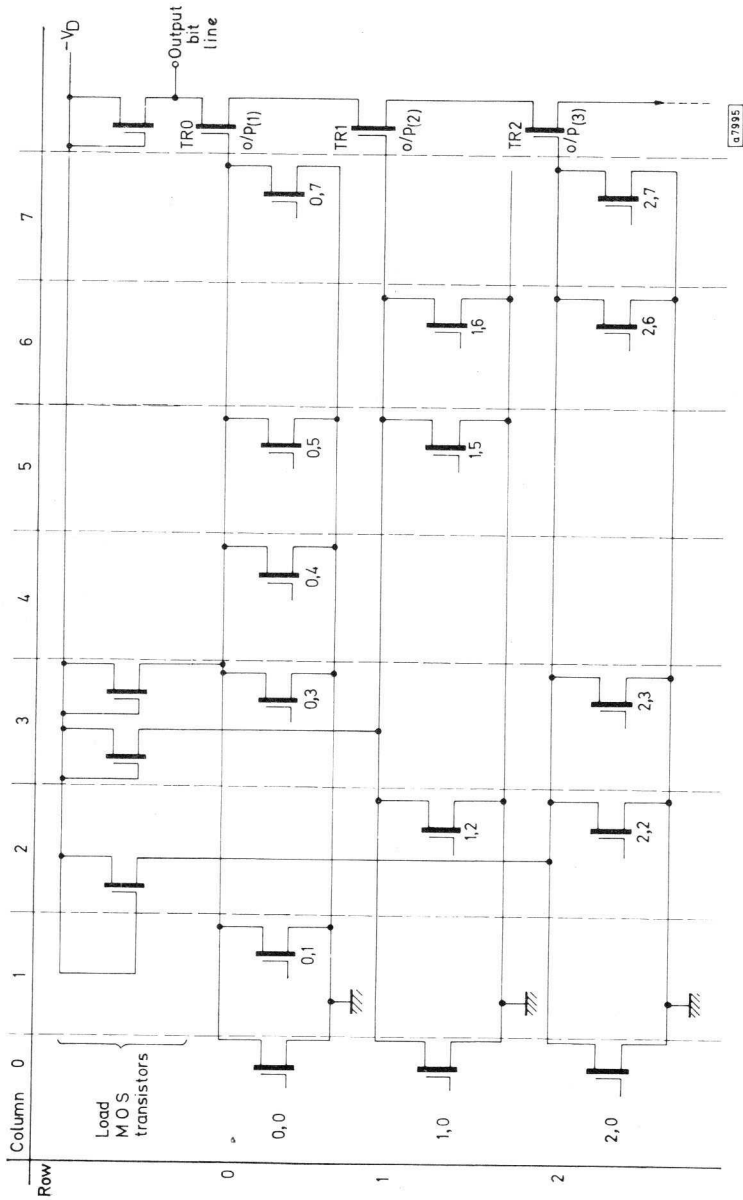


Fig. 6.15—Section of 64-bit read-only store matrix

RANDOM-ACCESS MEMORIES

The r.a.m. (random-access memory) or read-write store is a device consisting of a matrix of memory cells (bistables) arranged in x rows and y columns. Each location $(x,y)_n$ can be separately addressed and its contents read out, that is, transferred to an output line; alternatively, the location can be written into under the control of a 'write' line.

The basic memory cell is shown in Fig. 6.16. This is a simple bistable with common input-output connection. To write into the bistable the read-write terminal is made high (1) or low (0) according to the input information, and under the control of a 'write' control input. When the 'write' control is not active, the contents of the location may be read by sensing the logical state of the read-write terminal. Each memory cell has associated with it a read-write gate and output buffer, as shown in Fig. 6.17; the output buffer TR_6 is necessary to prevent the contents of the location being destroyed during a read pulse.

To read the contents of a particular location, that location is addressed on its read line. Transistor TR_7 is turned on and if the bistable contains a 0, then \bar{Q} is high and TR_6 is also in the ON state, making the output bit line low. If the location contains a 1, then \bar{Q} is low, TR_6 remains off and the bit line is held high by the common load MOST (not shown) which serves that particular bit line. The line may be common to say 16 bits in a store matrix.

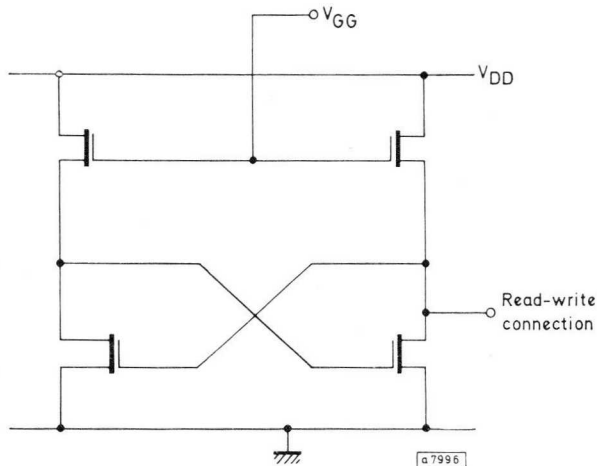


Fig. 6.16—Basic memory bistable

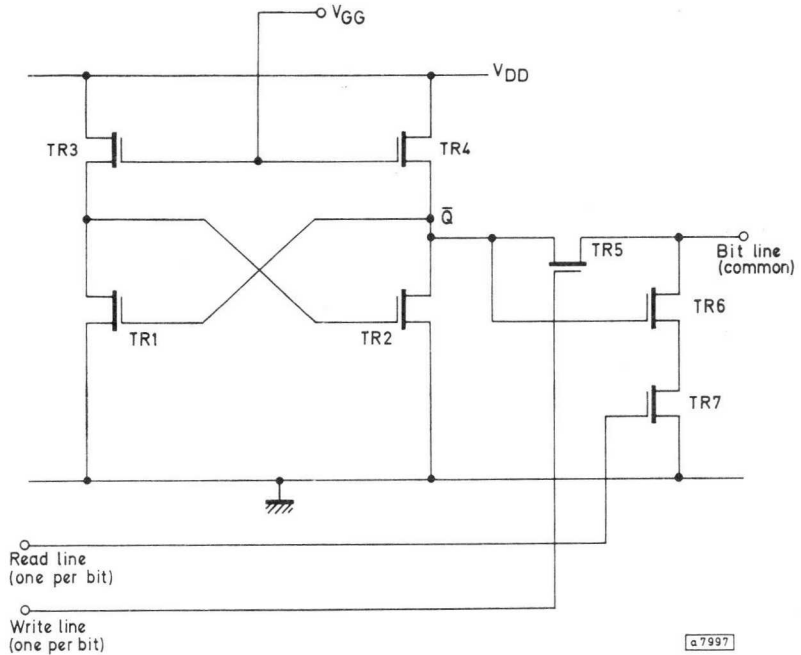


Fig. 6.17—One bit of random-access memory, including control gate and output buffer

To write into a location, the location is addressed on the write line, TR₅ is turned on, and the information level on the bit line at that time is entered directly to the bistable. Other bits common to this bit line are not affected because they are not addressed. As with the r.o.s., several r.a.m. units may be stacked to build up stores of multi-bit words, such as our experimental 16-word 4-bit single chip memory.

STORE DECODING ARRAY

The function of a decoding array is to allow any location within a store array to be individually addressed. Decoding arrays are often referred to as 'selection trees', and a number of different configurations are possible.

Fig. 6.18 shows part of a 16-address decoder using binary coding. Four inputs A, B, C and D are necessary to provide 16 possible input combinations. Each address using this system requires eight MOST devices, plus a share of the input buffers. A better arrangement is based

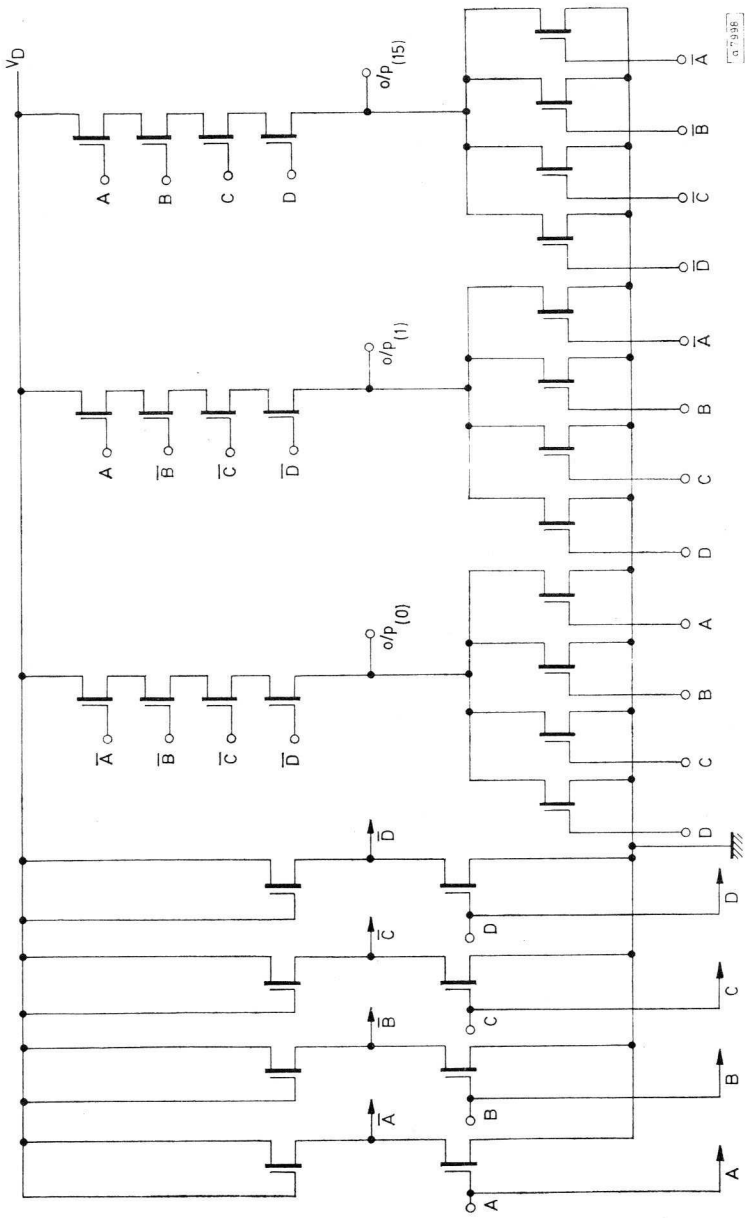
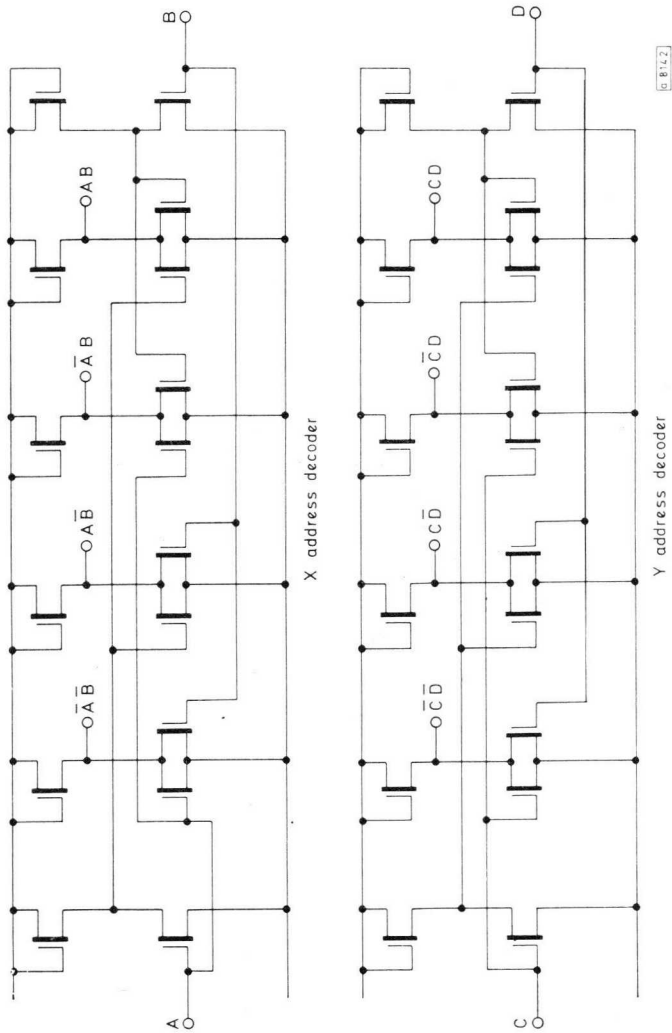
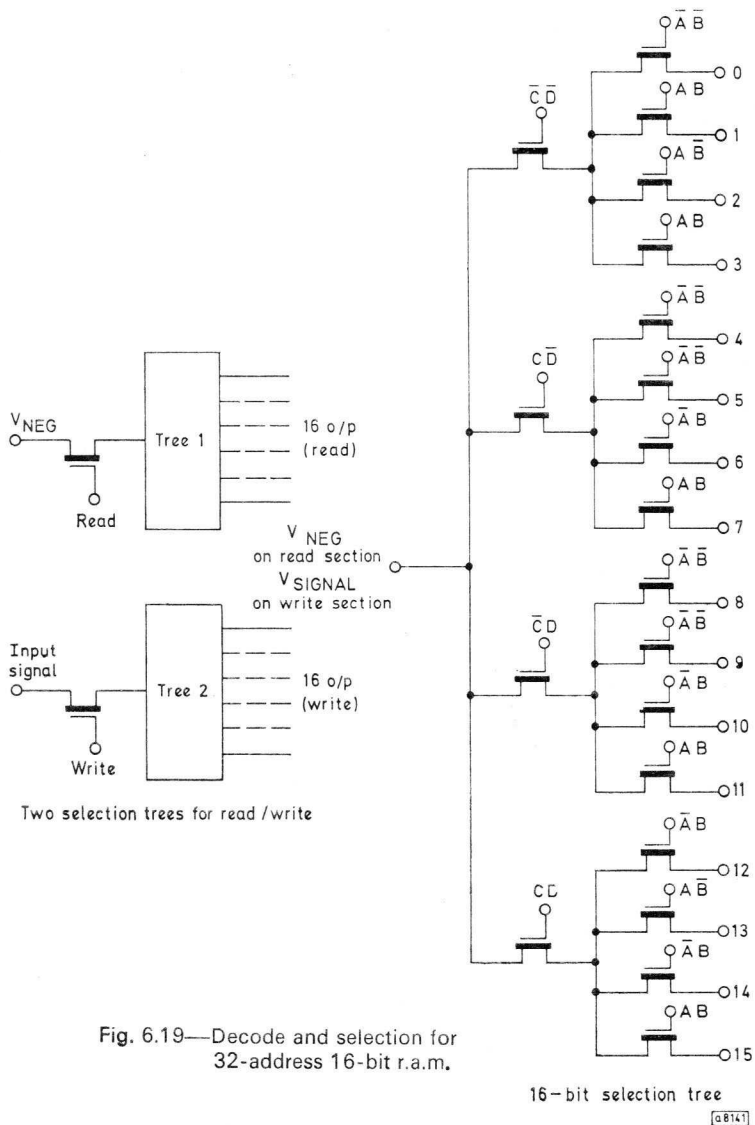


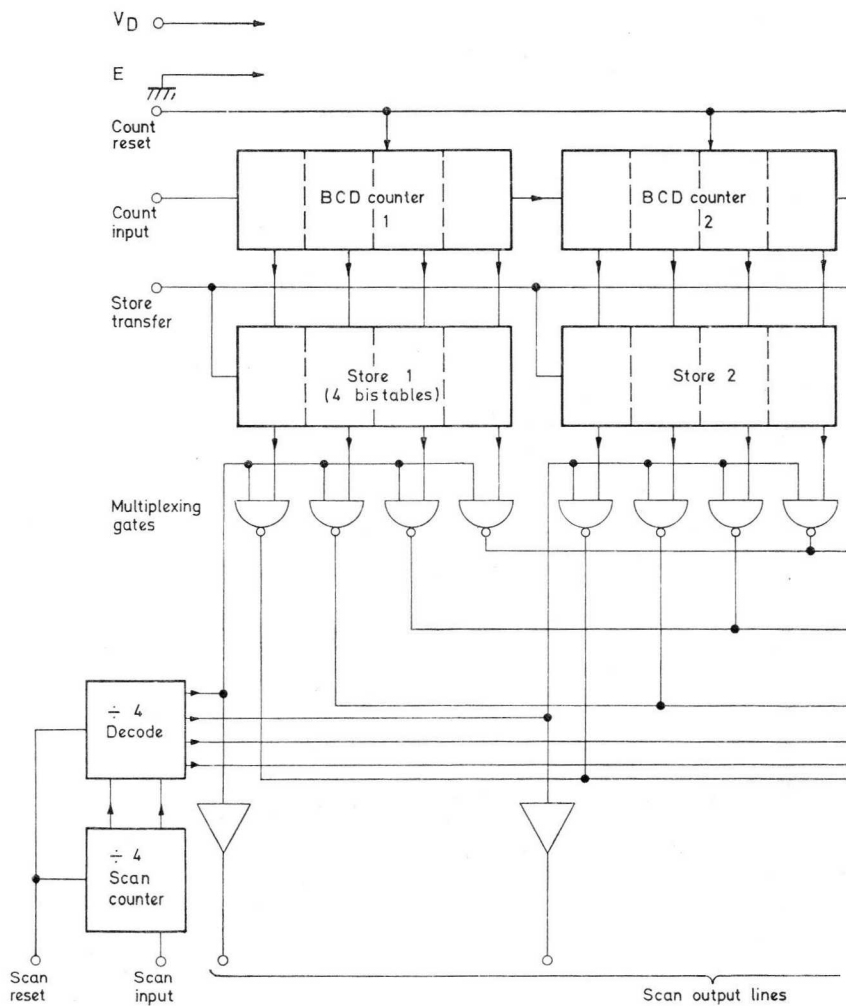
Fig. 6.18—Possible arrangement for 16-address decoder for r.o.s. (136 MOST devices)

on branching circuits as shown in Fig. 6.19, although care must be exercised in the design of this type of circuit if maximum speed is to be achieved, because of the series CR circuits.



7.17.2





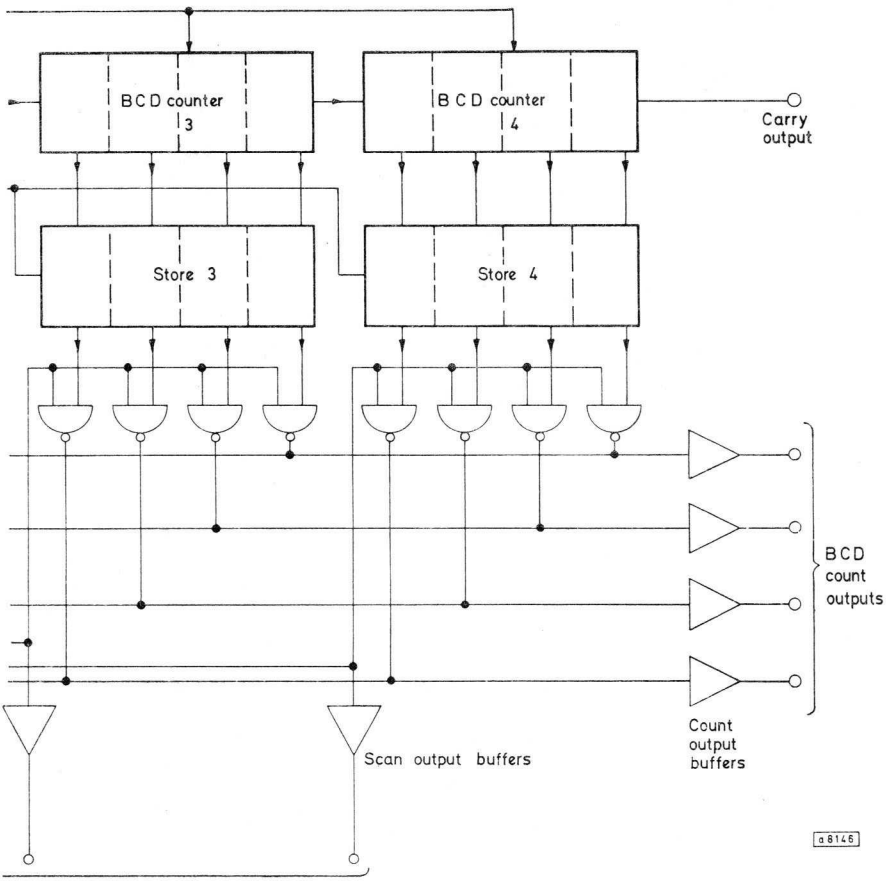


Fig. 6.20—Block diagram of 4-decade counter with multiplexed outputs

DYNAMIC SCANNING WITH STATIC LOGIC CIRCUITS

A major consideration in designing MOST logic circuits is the achievement of greatest economy; the complete system should be contained on as small a number of chips as possible, and the ratio of logic-to-pins should be as high as possible. One method of achieving a high ratio is to multiplex input or output signals to and from a MOST circuit.

The multiplexing concept is described by reference to a particular counting circuit. Multiple decade counters are frequently necessary for use in instruments and in control systems. An example of such a device might be the 4-decade counter shown in block diagram form in Fig. 6.20. This counter is a 4-decade unit operating in BCD code. Each decade is followed by a storage or staticisor stage, and the outputs of the 4-decade store stages are multiplexed to four BCD output lines.

Conventional circuitry would require the following connections:

two supply lines	carry output
common rail	reset zero
count input	store transfer
16 output lines (four for each decade),	

making a total of 23 leads. With multiplexing techniques the complete function can be accommodated in a 16-lead pack. The operation of the system is as follows. The counter stages can be reset to zero, in parallel, by means of the reset input. The 4-decade counters operate normally from the count input. When the count is complete, or a predetermined time has elapsed, the counter contents are transferred to the store section by means of a pulse applied to the store transfer line. The count information is then held static in the stores, and the counter section may be reset to zero and may proceed with another counting sequence.

The outputs from the stores (16 lines) must then be processed and fed out on the four output lines. This is achieved by means of the multiplexing gates. These 16 gates have their outputs OR-ed together in four groups of four. A second counter, the scan counter, generates sequential pulses on each one of four lines. The first pulse enables the multiplexing gates for Store-1 to pass the Store-1 contents to the output lines. This pulse then disappears, and Store-2 gates are enabled to proceed, and so on. The scan generator therefore causes the contents of each decade to be presented at the four count output terminals in sequence. The scan signals are also fed out from the counter chip and may be used externally for routing the sequential count output information.

Fig. 6.21 is a block diagram of part of a larger system incorporating a counter of the type described above. Here, a common BCD to decimal decoder supplies four display tubes. The anodes of these tubes are switched by the scan signals to ensure that each tube is on only during the period

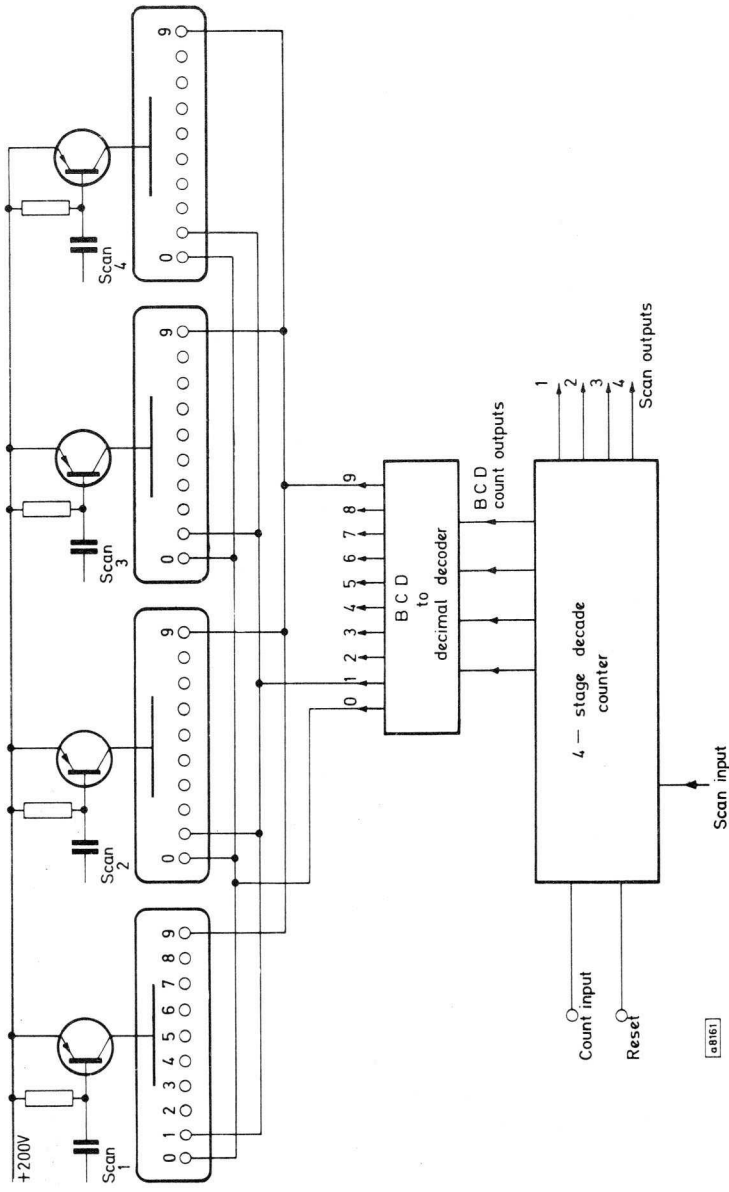


Fig. 6.21—Block diagram of 4-stage decade counter using display tubes

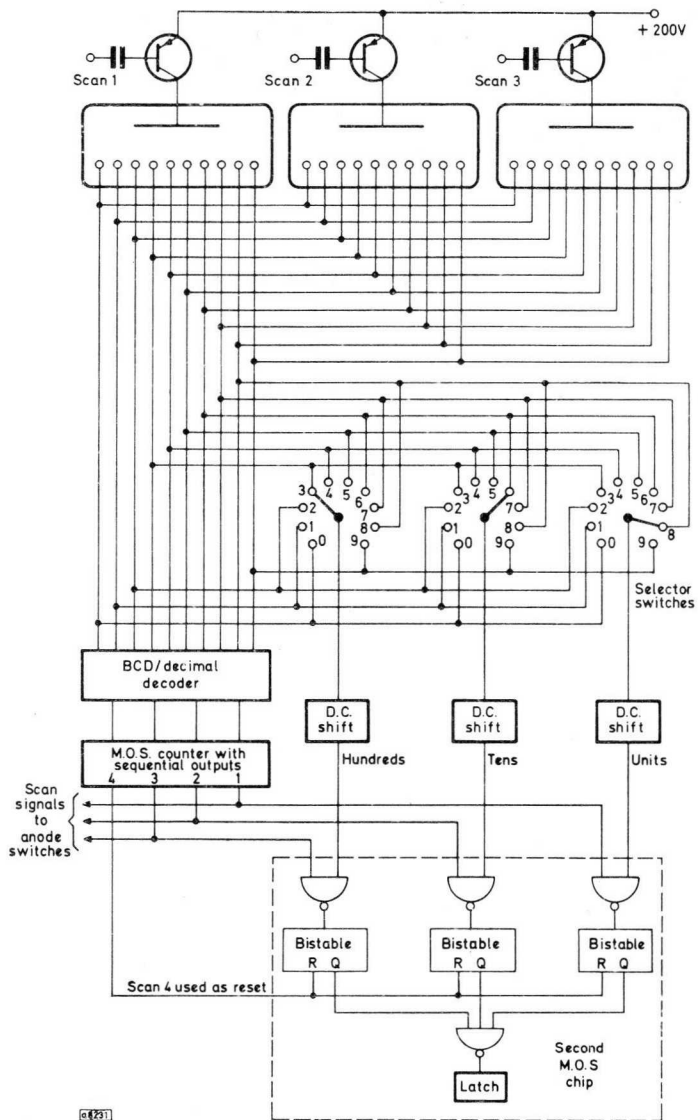


Fig. 6.22—Sequential input system

when the decoder output is intended for that particular tube.

The multiplexing technique can be used in a wide variety of systems. For example, read-only memories organised for 8-bit words could provide, say, 32-bit words by sequentially 'outputting' four words. The full word could then be built up in a 32-bit shift-register, the shift pulses being synchronised with the word-scanning pulses.

Input scanning is also used in some cases, not necessarily for pin economy, but for dealing with sequential input signals. In Fig. 6.22, a 3-decade display is operated by a sequential counter as described above. It is necessary to operate logic in a second MOS chip when a predetermined count has been reached, this number being set on the decade switches. Three of the scan signals route the switch outputs through gates to sensing bistables in this second chip. When the required count is reached, all three of these bistables will be set during a single scan cycle and the latch bistable will then be set. At the end of each scan cycle, the sensing bistables must be cleared; the fourth scan signal is used for this purpose.

The systems described above introduce the idea of dynamic scanning in logic systems, though in these systems the logic itself is static. Later chapters extend this idea to systems in which the logic is also operating under dynamic conditions.

CHAPTER 7

DYNAMIC LOGIC CIRCUITS

The elementary logic circuits discussed previously are analogous to bipolar logic elements, in that their logical state is defined by d.c. input levels, and the outputs are also d.c. levels. These elements absorb supply current via the load MOSTs all the time they are in the ON state, thereby giving rise to a certain average level of power dissipation for a given logic function. The power dissipation in static logic circuits can be reduced by increasing load MOST lengths, but the reduction in dissipation is achieved only at the cost of lower operating speed and increased device surface area.

Gating circuits of similar configurations to those discussed under static logic circuits (Chapter 6) can be designed to operate in the 2-phase mode by incorporating transfer and load switching. The d.c. design of the gates is similar in that the ratio of W/L of load and drive MOSTs must ensure correct d.c. logic levels, but higher currents may be used to gain higher speed because the dissipation is reduced in the ratio of clock OFF to ON time. The transfer MOSTs must be designed so that their ON resistance is sufficiently low to charge the storage gate capacitances within the minimum clock duration.

With special two-phase circuit techniques, the surface area can be reduced without loss of speed and with reduced dissipation. Four-phase logic, which will be described in detail subsequently, provides increased speed, reduced dissipation, and reduced area per function.

TWO-PHASE LOGIC CIRCUITS

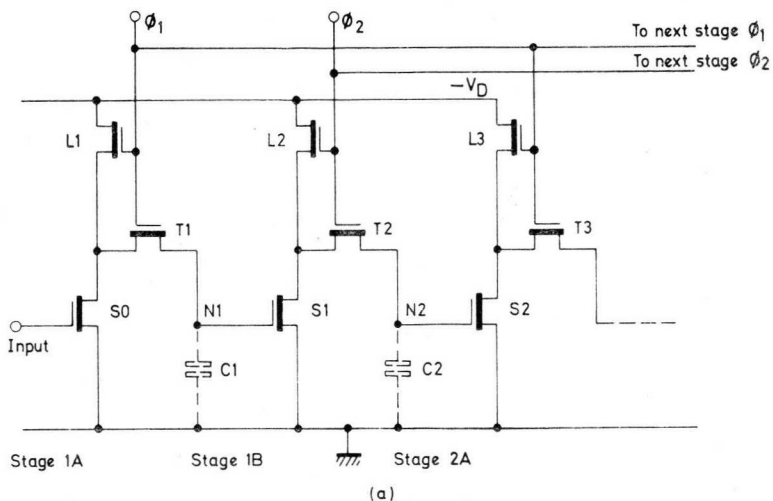
The main feature which distinguishes dynamic from static logic is that in static logic, d.c. supply power is consumed continuously, while in dynamic logic the load devices are only turned on during the presence of a clock pulse. Between clock pulses, information is stored in the form of a charge on the device gate capacitances (nodes).

Fig. 7.1 shows the basic circuit arrangement of a 2-phase logic element. Defining the devices in this circuit as 'S' for switching, 'T' for transfer and 'L' for load, transistors S_0, S_2 , etc. are the gating transistors and would normally consist of a number of devices connected in say a NOR function. Transistors S_1, S_3 , etc., the transient store devices, use gate capacitance to store charge, although with careful design these too could be used to provide gating functions. Transistors L_1, L_2, L_3 , etc., are load devices, and T_1, T_2 , etc., are transfer switches, which charge and discharge the storage gate capacitances, and make use of the bi-directional current-carrying capability of MOS devices.

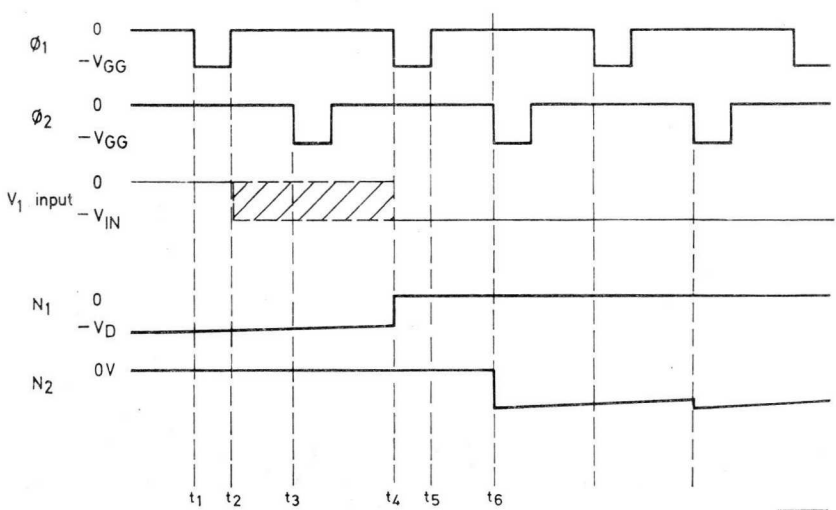
The operation of the circuit is as follows. An input logic level V_1 is applied to the gate of S_0 . Since ϕ_1 and ϕ_2 are initially both at zero, no supply current flows at this time. When ϕ_1 goes negative (time t_1), L_1 and T_1 are turned on and \bar{V}_1 is applied to the gate of S_1 . At the end of clock pulse ϕ_1 (time t_2) \bar{V}_1 is stored on the node capacitance C_1 , and L_1 and T_1 are turned off again. Input information is now locked out until the next ϕ_1 pulse. The supply current through L_1 and S_0 , and the charging current for C_1 , only flows during the presence of ϕ_1 . The circuit now remains quiescent until the ϕ_2 signal is applied (t_3). Transistors L_2 and T_2 are now turned on, and the \bar{V}_1 level stored on C_1 is applied after inversion to node capacitance C_2 , being the gate of S_2 . Thus, after a complete cycle of ϕ_1 and ϕ_2 (t_1 to t_4), the input logic voltage V_1 is stored on C_2 . The transfer MOSTs T_1, T_2 , etc., ensure that the charge stored on the gate capacitances remains while both clock signals are absent.

During the interval between clock pulses there will be some discharge from the gate capacitances, and it is this leakage time-constant which determines the maximum delay between clock pulses and hence the minimum operating frequency of the circuit. The maximum operating frequency is determined by the time taken to charge or discharge the gate storage capacitances with a given ϕ_1, ϕ_2 voltage level, which in turn sets a minimum safe clock pulse duration. Increasing the clock pulse levels produces an increase in speed, but too great a clock voltage (assuming ratings are not exceeded first) will cause the load MOSTs to turn on so hard that the logical '0' level may become too high and therefore give incorrect operation.

Input information is only entered during the ϕ_1 pulse and need only be correct during this time. Output information is true after the ϕ_2 pulse, and changes (if necessary) at the leading edge of the ϕ_2 pulse. Information is therefore delayed by one clock cycle time in a gating circuit. The circuit shown in Fig. 7.1a has no logic gating devices, and simply transfers input information from stage to stage at each clock cycle. It therefore provides a shift-register function.



(a)



Note. ϕ_1 and ϕ_2 must never overlap
 ϕ_1 and ϕ_2 levels are 0 and $-V_{GG}$ $V_{GG} > V_{DD}$
 (b)

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Fig. 7.1—Basic 2-phase logic circuit
 a) circuit
 b) waveforms

The information in a 2-phase circuit may be fed to a static inverting output stage such as that shown in Fig. 7.2, or may be fed out as a dynamic signal from a normal clocked stage. Static bistables may be included in 2-phase circuits as staticisers at the end of a logic chain, ensuring that information is not lost even if the clock signals are removed.

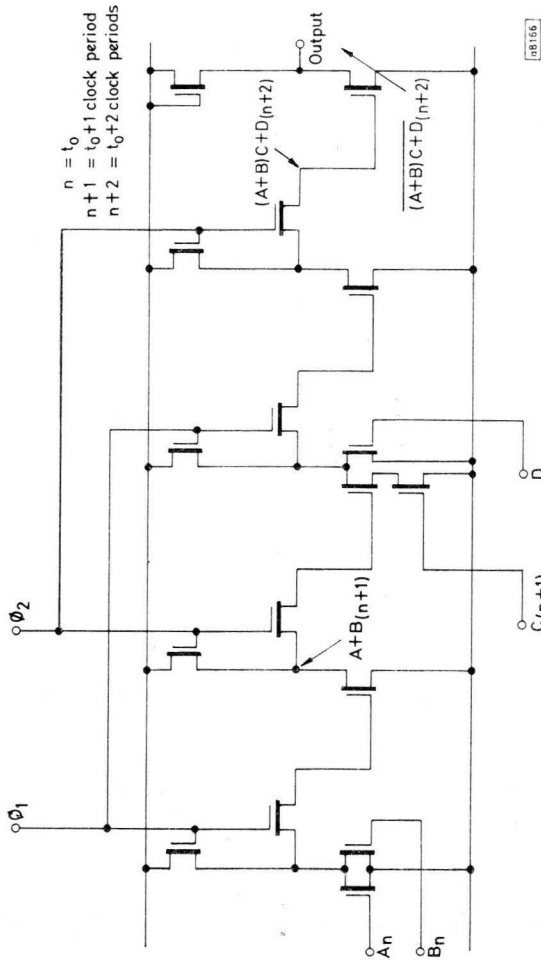


Fig. 7.2—Two-phase logic circuit (static output)

Operating frequencies with 2-phase circuits range from about 10kHz to 3MHz at present. The minimum operating frequency increases at high temperatures because of increased leakage in the circuit. Power consumption varies with operating frequency and clock pulse duration. Typically, shift-register stages operate at about 1 to 2mW per bit at 1MHz.

TWO-PHASE LOGIC VARIANT

Two-phase circuits can be designed so that their operation depends on their ratio of sizes of one device to another as in d.c. logic circuits. It is also possible to design 'ratio-less' circuits where all devices are substantially the same size. One of the major advantages of dynamic logic comes from this approach in that no load MOSTs are required. Thus it is possible to achieve higher operating speed and, at the same time, a reduction in area.

Fig. 7.3 shows a variant of the 2-phase logic theme. Here, each half stage consists of an inverter and a transfer MOST. Devices TR₄, TR₈, TR₁₂, etc., are the gating MOSTs and TR₃, TR₇, TR₁₁, etc., are transfer devices. An additional device, TR₁, is added to the system described previously. The system functions as follows. Data is entered at the input terminal. When ϕ_1 is applied (negative), TR₁ turns on and C₁ is charged to a negative voltage. Pulse ϕ_1 is now removed and after a short interval,

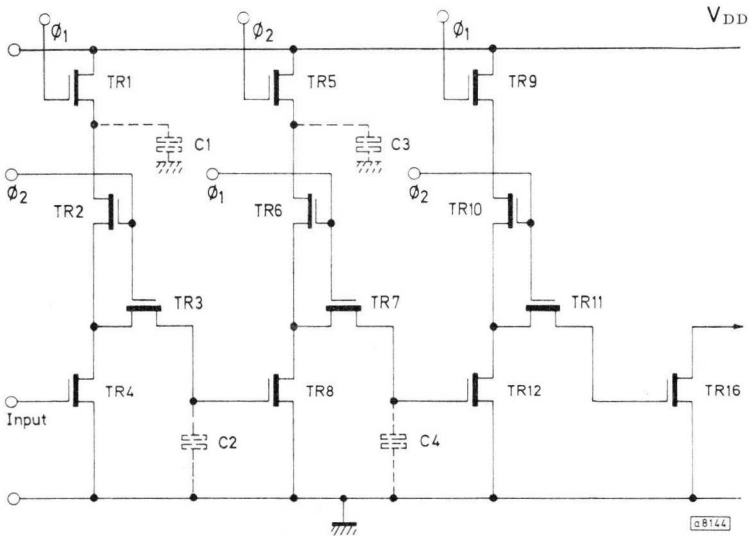


Fig. 7.3—Two-phase dynamic shift-register

ϕ_2 is applied; this turns on TR₂ and TR₃. If the input to TR₄ is a '0', TR₄ remains off and charge is transferred from C₁ through TR₂ and TR₃ to C₂. The gate of TR₈ is now negative. While ϕ_2 is present, C₃ is also charged. Pulse ϕ_2 is now removed, and ϕ_1 reapplied. Transistors TR₆ and TR₇ are turned on (at the same time, C₁ is recharged). Because of the charge stored on C₂, TR₈ is ON, and C₃ is discharged during this ϕ_1 pulse via TR₆ and TR₈. There is therefore a '0' level at the output of TR₈, and the original input information has been shifted one place to the right. During this ϕ_1 period C₄ is discharged if TR₈ is on, in preparation for a further transfer of information during the next clock cycle.

In circuits such as this, C₁, C₃, etc. consist of diffusion capacitance and aluminium-to-substrate capacitance, and the layout must be designed to make C₁ greater than C₂ because the charge on C₁ is shared between C₁ and C₂ in the ϕ_2 period. Similarly, C₃ and C₄ share their charge during ϕ_1 (assuming the gating MOSTs are off). It is possible with this type of circuit to remove the V_{DD} rail altogether and replace it by phase signals as shown in Fig. 7.4. Here, the operation of the circuit is as previously described, except that the charge for C₁, C₃, etc. is taken from the clock lines rather than from a d.c. rail. In designing 2-phase circuits, great care must be taken in layout to ensure an optimum balance between the various circuit capacitances.

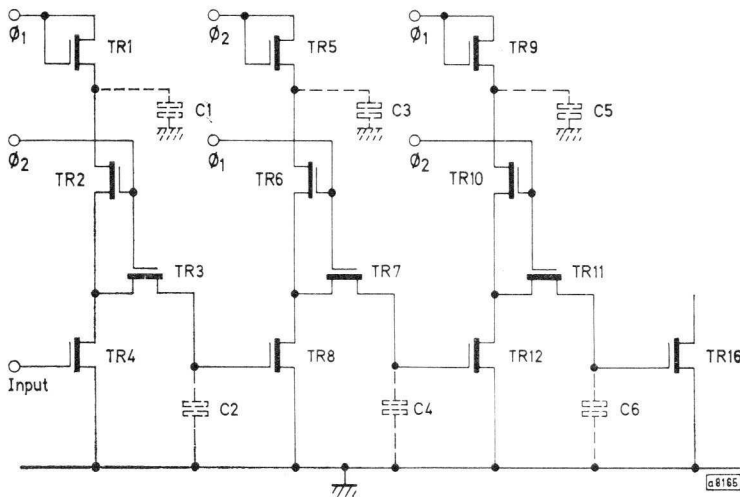


Fig. 7.4—Dynamic shift-register without d.c. power rails

As with most dynamic systems, the clock rate must not be reduced below a certain minimum value. At 25°C this value may be as low as 1kHz but at high temperatures, say 75°C, the leakage of the reverse-biased p-n junctions (source and drain diffusions to substrate) limits the time for which a charge can be held on gate capacitances, and the minimum speed may have to be raised to say 10kHz.

Clock waveform generation for two-phase circuits

The required clock waveforms for two-phase logic are as shown in Fig. 7.5. The main requirement is that the two phases do not overlap. In the simplest case, a waveform such as Fig. 7.6 could be used, derived directly from a bistable element as in Fig. 7.7, but in circuits where

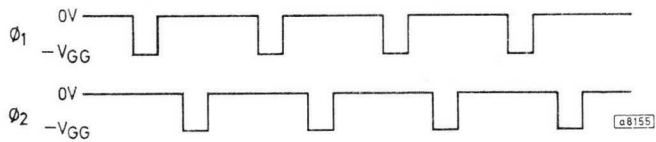


Fig. 7.5—Two-phase clock waveforms

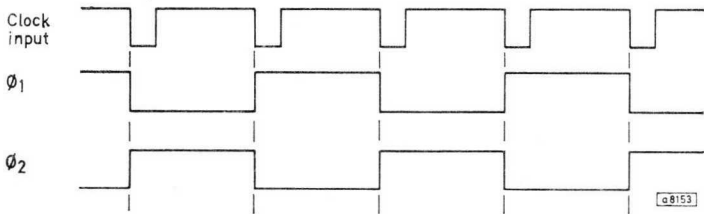


Fig. 7.6—Simplest form of 2-phase clock waveforms

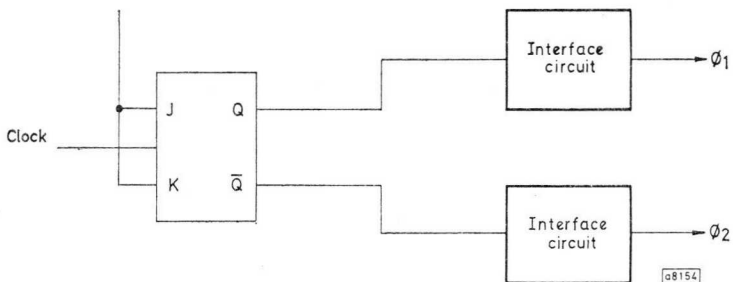


Fig. 7.7—Simple 2-phase clock generator

d.c. flows during the phase pulses, no reduction in power dissipation would be obtained. By modifying the circuit to Fig. 7.8, any possibility of overlap is eliminated, and the spacing between ϕ_1 and ϕ_2 can be controlled by varying the input clock pulse duration. Gates 1 and 2 may be integrated circuit gates or may be incorporated as part of the interface circuits. The technique described above is used in Fig. 8.15 (page 92) to generate the clock waveforms for a four-phase circuit.

An alternative method of generating clock waveforms for dynamic logic uses delays or monostables. A circuit using elementary delays is shown in Fig. 7.9. The circuit of Fig. 7.10 uses the FJK101 monostable to provide the necessary waveforms. This monostable may be made to trigger from either a positive or a negative-going input transition. This feature is used here to separate the two monostable active periods. Pulses O_2 and O_4 are the inverse of O_1 and O_3 respectively and either pair

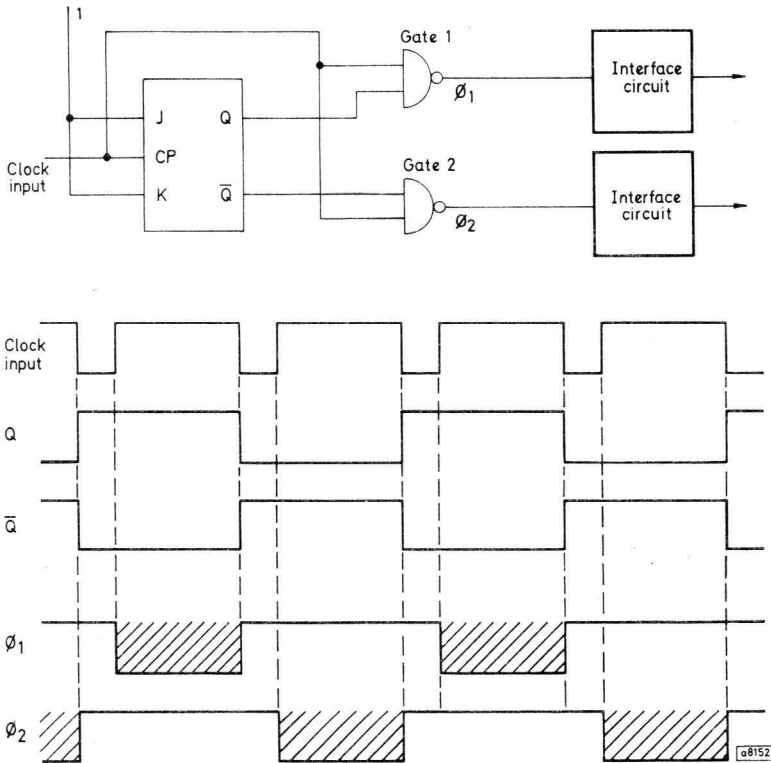


Fig. 7.8—Simple gating circuit to eliminate phase overlap

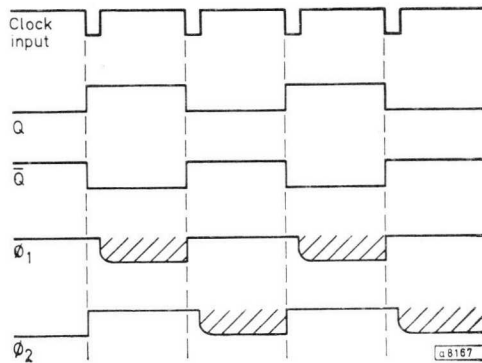
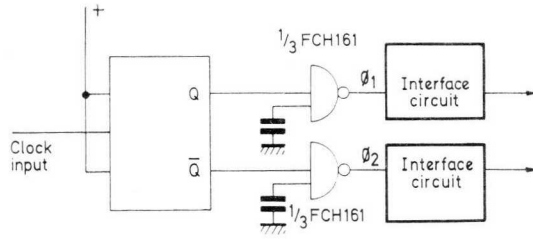


Fig. 7.9—Simple 2-phase clock waveform generator using delay elements

(O_1 with O_3 or O_2 with O_4) may be used to drive the interface level changing circuits, depending on whether these interface circuits provide a logical inversion or not. The timing capacitor shown gives a pulse duration of approximately $1\mu s$.

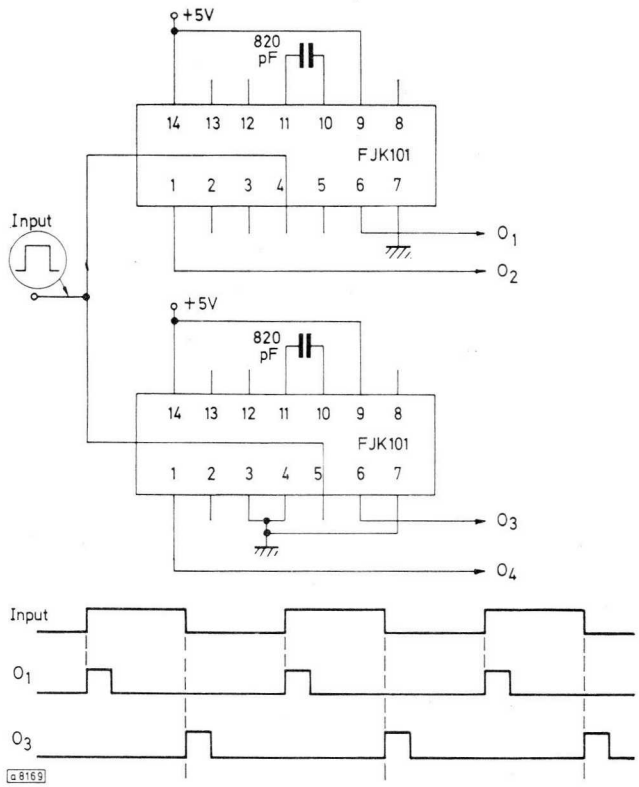


Fig. 7.10—Use of monostables to generate 2-phase waveforms

CHAPTER 8

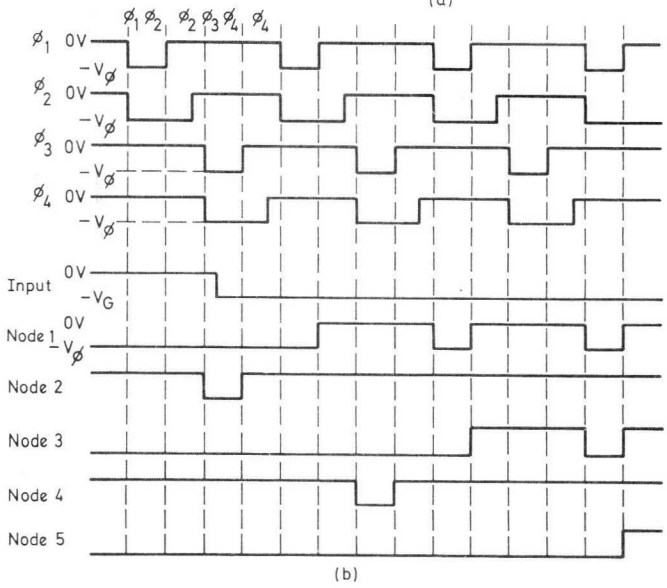
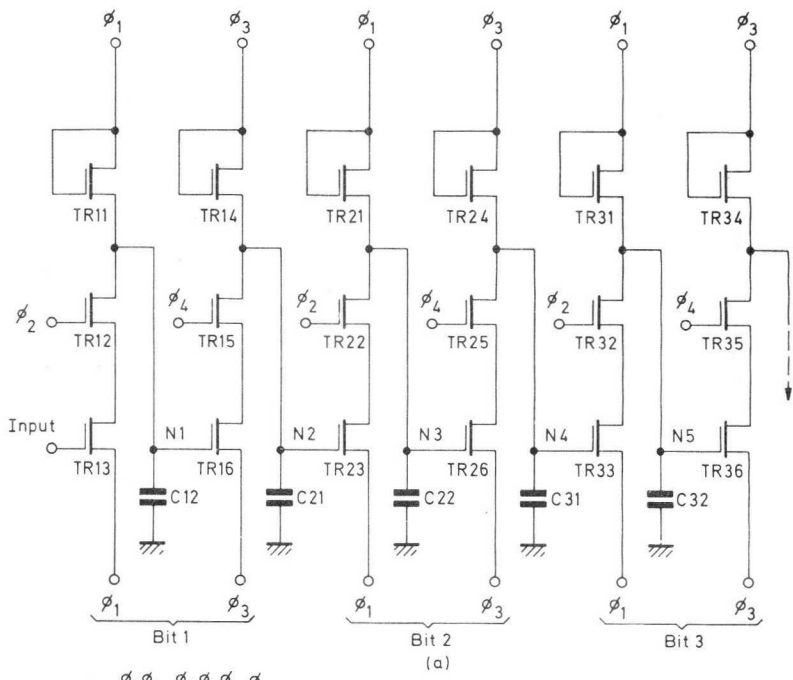
FOUR-PHASE DYNAMIC LOGIC CIRCUITS

Four-phase dynamic MOS logic offers high-speed operation, extending to at least 5MHz, with very low dissipation (typically $100\mu\text{W}$ per shift-register bit at 1MHz), at the same time allowing devices of minimum size to be used. In many circuits all individual MOSTs can be of the same size.

The principle of operation is an extension of the 2-phase operation, but the circuit is designed so that the only input current required is that necessary to charge or discharge node capacitances; this current is supplied from the 'phase' signals, and unless some static or quasi-static circuitry is included in the chip no d.c. supply is required.

The most commonly-available type of 4-phase logic circuit is the shift-register, and the operating principles of 4-phase circuits will be described in the first instance by reference to shift-register elements. The basic shift-register circuit is shown in Fig. 8.1a, and the waveforms are shown in Fig. 8.1b. The operation of the shift-register is as follows.

During the ϕ_1, ϕ_2 period TR_{11} and TR_{12} are on; TR_{13} may or may not be on depending on the input voltage level. In any case, as a result of TR_{11} being in conduction, C_{12} is charged to a negative level (as are C_{22} , C_{32} , etc.). At the end of the ϕ_1 pulse TR_{12} is held on by ϕ_2 , and if TR_{13} is on it discharges C_{12} to zero through the lower ϕ_1 line. If the input voltage is zero, TR_{13} is off and C_{12} retains its negative charge. Pulse ϕ_2 then disappears and after a short delay ϕ_3 and ϕ_4 pulses are applied producing a negative charge on C_{21} (and also on C_{31} , C_{41} , etc.). When ϕ_3 is removed, ϕ_4 remains and if C_{12} holds 'zero' then C_{21} remains charged. If C_{12} holds a negative charge, C_{21} is discharged.



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Fig. 8.1—Section of 4-phase dynamic shift register

Thus, after a complete cycle of clock pulses, the logic level originally applied to the input is transferred through a complete stage and is then held on C_{21} . After a further clock cycle the same logic level appears on C_{31} . Information is thus sequentially shifted at each clock cycle through

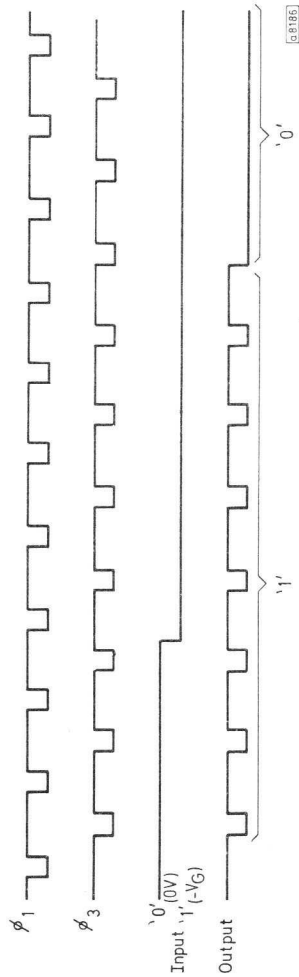


Fig. 8.2—Input and output waveforms of 4-bit shift-register

one stage of the shift-register, and input information appears at the output after a delay of N clock periods where N is the number of stages. Note that if the input level is a '1' (negative) for a number of clock cycles then this level remains constant, apart from leakage, on C_{21} . If the input level is a constant '0' (zero) however, the level on C_{21} pulses to a negative level during the ϕ_3 period. The output of a 4-phase circuit is also of this form and must not be read during the ϕ_3, ϕ_4 period. Information is true at the output from the end of the ϕ_3 pulse to the beginning of the next ϕ_3 pulse. Input information is read in during the ϕ_2 period. Input and output waveforms of a 4-bit shift-register are shown in Fig. 8.2.

FOUR-PHASE LOGIC SWITCHING TIMES

The switching times of 4-phase circuits determine the minimum clock pulse duration and hence the maximum operating frequency. Two switching times are important:

- 1) Charge time of node capacitors to a sufficiently high negative voltage during the pre-charge periods ϕ_1, ϕ_3 .
- 2) Discharge time of node capacitors during the periods when only the ϕ_2 or ϕ_4 pulses are present.

Pre-charge time

During the pre-charge time the input to TR_{13} (Fig. 8.1a) may or may not be negative. If it is negative then when ϕ_1 and ϕ_2 are simultaneously present, TR_{12} and TR_{13} provide a parallel path with TR_{11} to charge C_{12} . In this condition the charge time will obviously be a minimum.

The worst case, which must be considered when designing a circuit, is when the input is at zero and the node capacitances are charged through $TR_{11}, TR_{14}, TR_{21}$, etc. These devices operate in the saturated mode, and the node capacitor voltage as a function of time is given by replacing V_s by V_ϕ (phase voltage) in Eq. 5.8.

$$V_C = \frac{(V_\phi - V_T)^2}{(2C/\beta t) - (V_\phi - V_T)}$$

The maximum final output voltage $V_{fin.}$ would be $V_\phi - V_T$, and the rise-time to a fraction α of this final value is

$$t_\alpha = \frac{2\alpha C}{\beta V_{fin.}(1-\alpha)}$$

where β is the effective β value of TR_{11}, TR_{14} , etc., and is a function of the effective gate voltage, and C is the total load capacitance including the aluminium over thick oxide (interconnect) as well as the gate capacitance of the driven device. Examples of the calculation of the effective capacitance are given in the discussion on layouts (page 84).

FOUR-PHASE GATING CIRCUITS

As with static and 2-phase systems, normal gating functions can be built using 4-phase techniques. Fig. 8.3 shows a number of possible circuit configurations for logic gates. Fig. 8.3a shows a gate in which the first half provides a NAND function, the output of which appears after a half-bit delay. The half-bit delay is indicated by the subscript (ϕ_2), indicating that the output signal appears at the end of ϕ_2 . After a further half-bit delay the inverted output (now true AND) appears at the output of the second half of the gate, at the end of ϕ_4 .

In normal 4-phase shift-register stages all devices are the same size, but in gating circuits device sizes must be modified to ensure a uniform working speed and uniform logic levels. In Fig. 8.3a, TR₃ and TR₄ are twice as wide as the other devices in the circuit. Fig. 8.3b introduces the NOR function, and here all the devices can be of the same size. Fig. 8.3c shows a more complex combinational logic system using half-bit logic timing; that is, it performs separate logic functions during the two half-bit shift periods. Fig. 8.4 shows a non-delaying inverter and a normal ϕ_3, ϕ_4 stage for driving other sections of the array. The two output sections are separately driven by TR₂, TR₃, and TR₄ and TR₅. If this arrangement is not adopted the correct charge levels cannot be maintained at the various node points within the circuit.

Sneak paths

Fig. 8.5a shows a simple logic circuit. As the gates of TR₄ and TR₉ are supplied from a common input A and must conduct together it would seem reasonable to use one transistor in place of TR₄ and TR₉ as shown in Fig. 8.5b. However, a sneak path can occur in this simplified circuit as follows. If B, C and D are at '1' and A is at '0', TR₈ can conduct via TR₃ and TR₅ and node 9 is discharged. This should not happen and cannot occur in the circuit of Fig. 8.5a. Hence, if the circuit is simplified it should be carefully examined for sneak paths.

FOUR-PHASE BISTABLE CIRCUITS

Bistables in 4-phase logic consist, as in other logic forms, of interconnected gates. In the case of 4-phase circuits the logic information is only stored in the form of gate charge and must be 'refreshed' regularly. This 'refreshing' process is provided by the clock signals. Fig. 8.6 shows a 4-phase bistable circuit such as might form part of a 4-phase memory circuit.

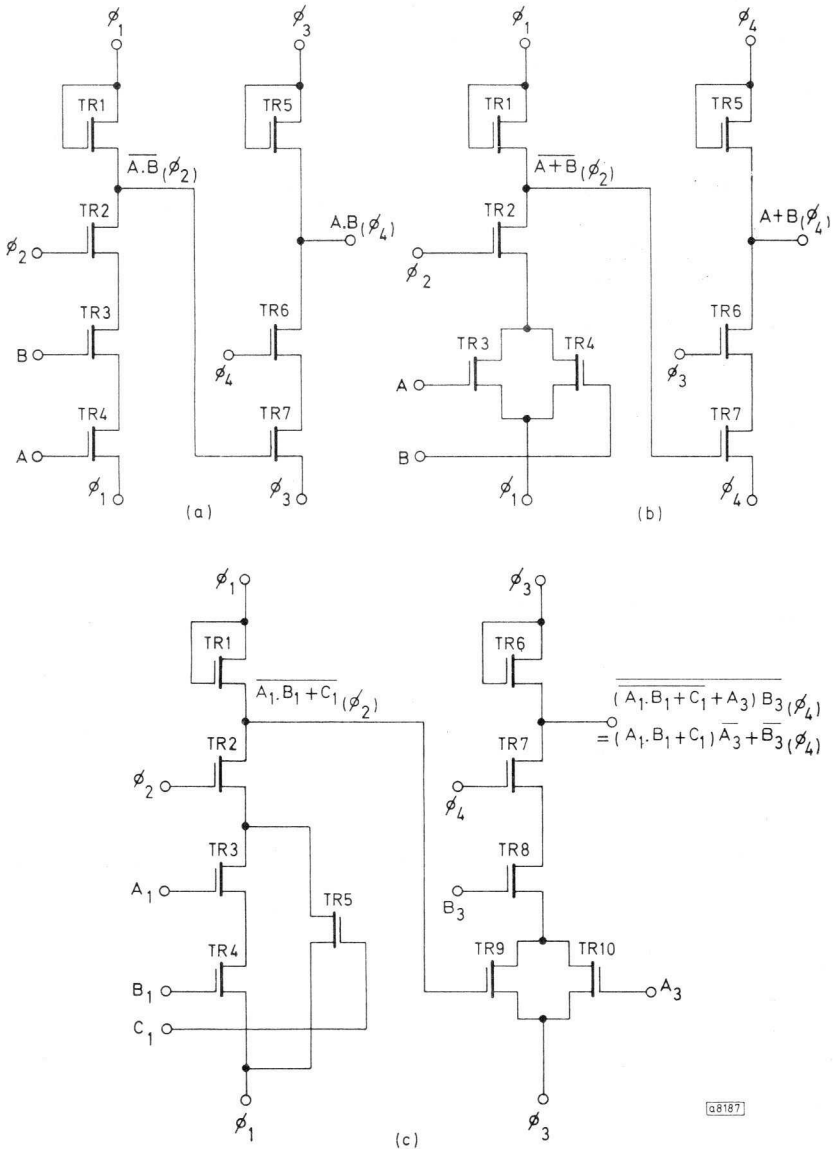


Fig. 8.3—Possible logic gate circuit configurations
 a) Four-phase AND/NAND gate
 b) Four-phase OR/NOR gate
 c) Combinational 4-phase logic

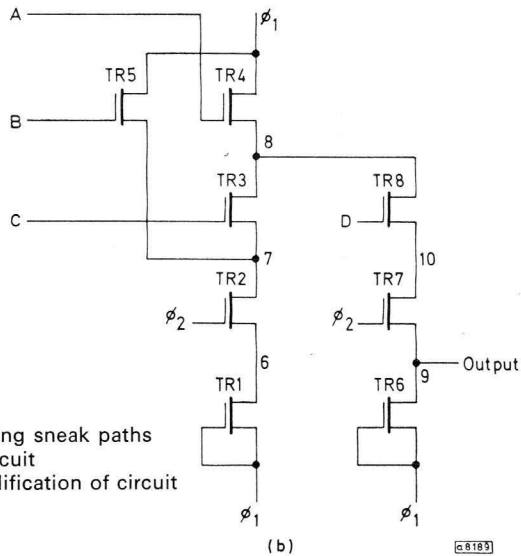
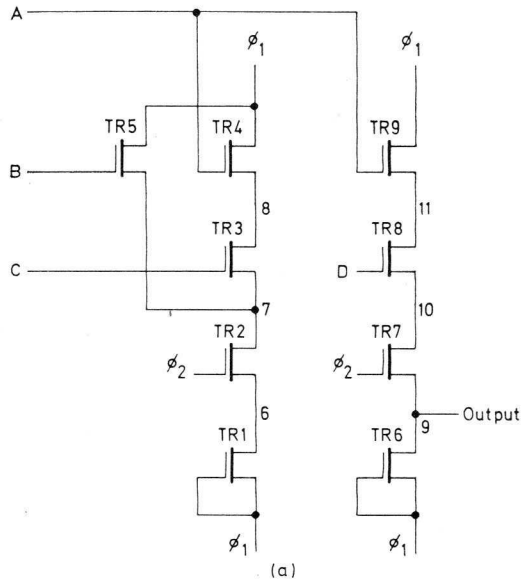


Fig. 8.5—Circuits illustrating sneak paths
 a) simple logic circuit
 b) danger of simplification of circuit

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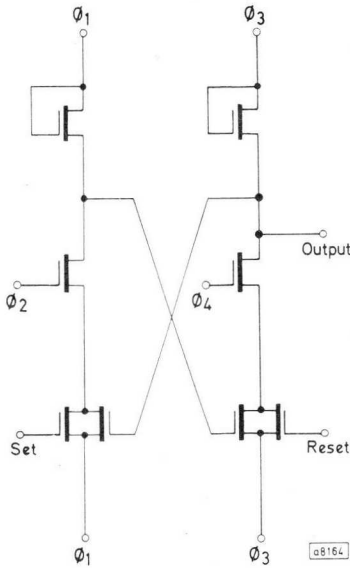


Fig. 8.6—Four-phase bistable

Calculation of capacitances

The capacitance of a node to the substrate can be estimated by considering its components separately. These calculations are only approximate, but they do give a useful guide to the composition of the node capacitance. For a more detailed calculation it is necessary to consider the variation of thin oxide capacitance with voltage. The simplified equations used for estimating the node capacitance are as follows:

$$\text{Capacitance of p-diffused regions to the substrate} = \frac{\text{area in } \mu\text{m}^2}{10(V+0.7)^2} \text{ fF}^*,$$

where V = p-diffusion-to-substrate bias voltage.

$$\begin{aligned} \text{Capacitance of aluminium over thick oxide to the substrate} &= 3.4 \times 10^{-2} (\text{area in } \mu\text{m}^2) \text{ fF}. \end{aligned}$$

$$\begin{aligned} \text{Capacitance of thin oxide to the substrate} &= 3.4 \times 10^{-1} (\text{area in } \mu\text{m}^2) \text{ fF}. \end{aligned}$$

*1 femtofarad = $1 \text{mpF} = 10^{-15} \text{F}$

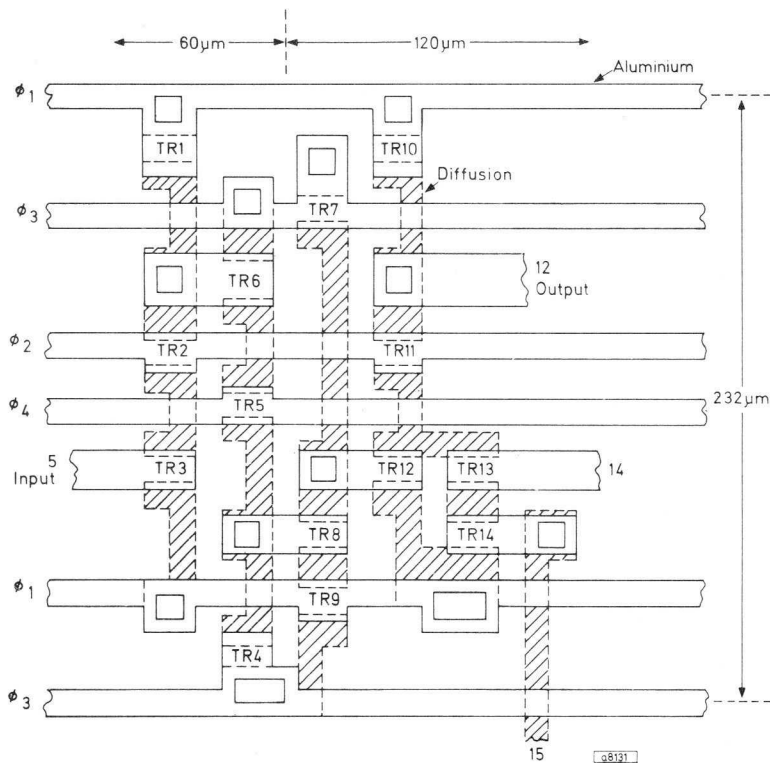


Fig. 8.7—Layout for 4-phase circuits (example 1)

As an example, the capacitance to the substrate for node 6 (Figs. 8.8 and 8.10) is estimated below. The diffusion bias voltage is taken as $-10V$. The source and drain of TR_6 are assumed to be connected to the substrate. Area of diffusion as drawn $= (20 \times 20) + (20 \times 20) + 10(34 + 26) = 1400 \mu m^2$. Additional area due to sideways diffusion $= 649 \mu m^2$.

Total capacitance of diffusion to substrate at $-10V$ bias

$$= \frac{1400 + 649}{10(10 \cdot 7)^{\frac{1}{2}}} \approx 63 fF.$$

Capacitance of aluminium over thick oxide to substrate $= 3 \cdot 4 \times 10^{-2} \times 140 \approx 4 \cdot 8 fF$.

Capacitance of gate of TR_6 to substrate (aluminium over thin oxide) $= 3 \cdot 4 \times 10^{-1} \times 12 \times 16 \approx 65 fF$.

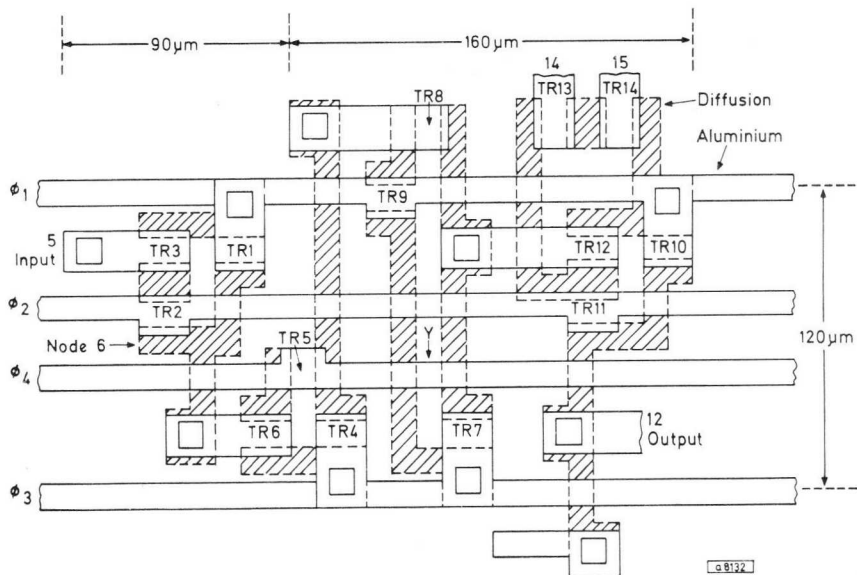


Fig. 8.8—Layout for 4-phase circuits (example 2)

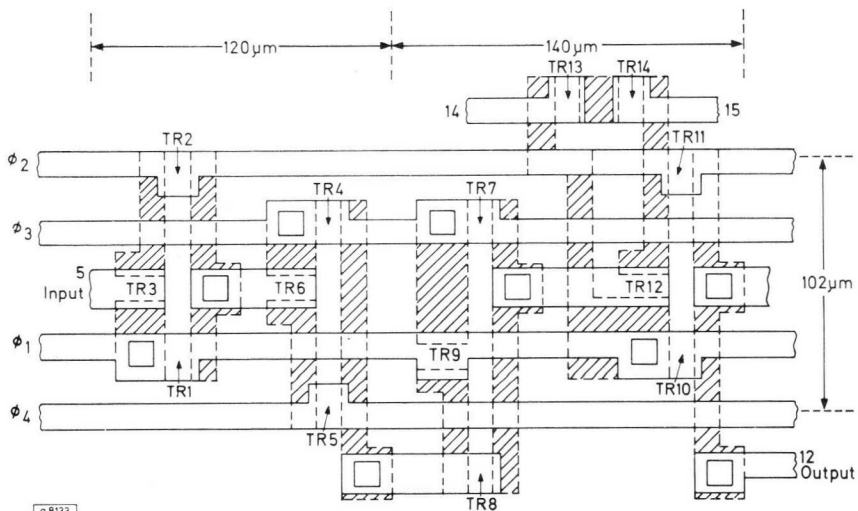


Fig. 8.9—Layout for 4-phase circuits (example 3)

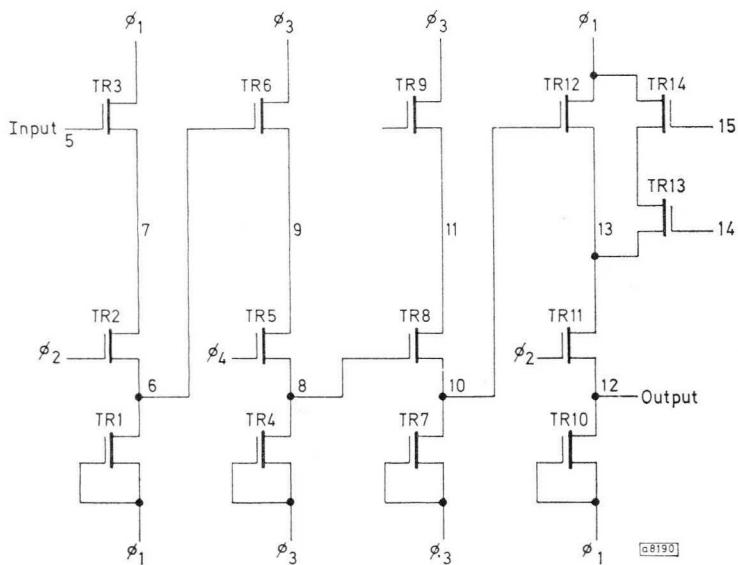


Fig. 8.10—Circuit diagram for layout examples

Total capacitance of

node 6 to substrate ($C_{6, o}$) = $63 + 4 \cdot 8 + 65 \simeq 133\text{fF}$.

Although this calculation is approximate it has been found that elementary calculations based on this value do give a useful guide to the circuit performance.

The equations can be used to estimate crossover capacitances. In the layout of Fig. 8.8 the capacitance C_x between ϕ_4 and node 12 is given by:

$$C_x = 3 \cdot 4 \times 10^{-2} (\text{p-region under the } \phi_4 \text{ line in } \mu\text{m}^2)$$

$$= 3 \cdot 4 \times 10^{-2} \times 10 \times 13 \simeq 4 \cdot 4\text{fF}.$$

Transistor feedback capacitances can also be estimated. For example, the gate-to-drain capacitance C_{gd} of TR₆ in Fig. 8.8, when TR₆ is off, is given by:

$$C_{gd} = 3 \cdot 4 \times 10^{-1} (\text{area gate overlaps drain in } \mu\text{m}^2)$$

$$= 3 \cdot 4 \times 10^{-1} \times 12 \times 4 \cdot 5 \simeq 18\text{fF}.$$

Parasitic channels

Parasitic channels can occur between two adjacent p-diffused regions if they are crossed by an aluminium interconnection. For example, a parasitic transistor can occur at Y in Fig. 8.8 with ϕ_4 serving as the gate.

Normally, the MOST formed in this way has a thick gate oxide and consequently a high threshold voltage, which is normally greater than the maximum voltage rating of the circuit. However, parasitic channels may be formed which will destroy the circuit operation if this voltage rating is exceeded.

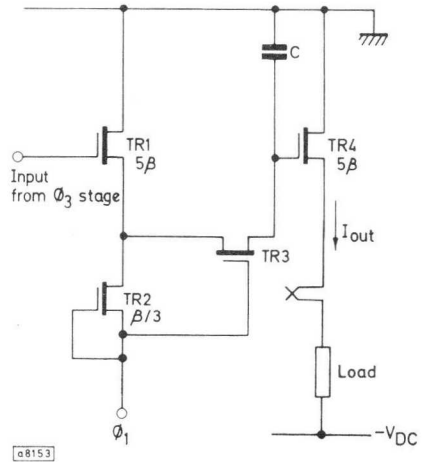
STATICISOR FOR FOUR-PHASE CIRCUITS

As stated earlier, in 4-phase circuits, while a '1' output level is constant (negative) a '0' output pulses to the '1' level during the ϕ_3, ϕ_4 coincidence time. When signals are to be used outside the 4-phase MOS logic system, such as into static MOS logic or bipolar circuits, it is necessary to eliminate the '1' level pulse during the '0' output state so that both logic states are d.c. levels. Fig. 8.11 shows a staticisor circuit which could be included in a 4-phase chip.

The device sizes are different from the normal 4-phase logic transistors and the figures indicate the relative β of the devices used, taking a normal logic transistor as 1β . When the input level is a '1', TR_1 remains on during the complete clock cycle and TR_4 remains off, thereby providing a '1' output.

When a '0' input is fed to the circuit, TR_2 and TR_3 provide a charge to C during the ϕ_1 period, but during the ϕ_3 period when the input goes to a '1' state, TR_3 and TR_1 are off, and C remains charged, holding TR_4 in the ON state. Transistor TR_4 is larger than the normal logic transistors to provide an output current level suitable for use in interface circuits.

Fig. 8.11—MOS staticisor for 4-phase logic circuit



Low power staticisor for four-phase circuits

Fig. 8.12 shows a low-power 4-phase staticisor circuit for use in lower speed applications. The output information for the 4-phase system is fed in at the input terminal and charges C_1 during ϕ_2 . During ϕ_3 this charge is transferred to C_2 , thus operating TR4. The correct levels may require three clock pulses before they are achieved, but this staticisor does not pass current through the series devices to ϕ_1 as is the case for Fig. 8.11.

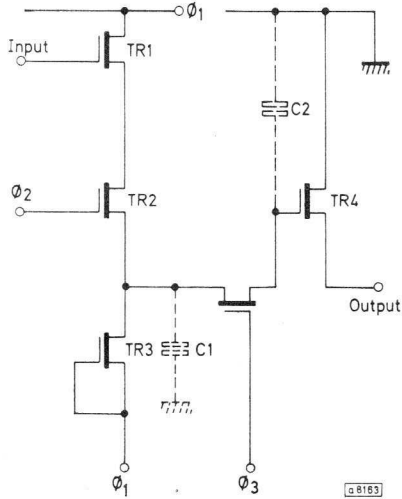


Fig. 8.12—Low-power 4-phase staticisor

CLOCK PULSE GENERATORS FOR FOUR-PHASE LOGIC CIRCUITS

The 4-phase clock waveforms necessary for this form of dynamic logic require that there is no overlap between ϕ_2 and ϕ_3 or between ϕ_4 and ϕ_1 . A suitable logic circuit to provide these waveforms is shown in Fig. 8.13. The circuit consists of a 2-stage binary counter, and gates G_2 to G_5 decode the four possible logic states. To prevent pulse overlap, the width of the clock pulse (CP) is subtracted from the \bar{A} waveform before the decoding gates, thereby giving positive prevention of overlap, as shown in Fig. 8.14.

Fig. 8.15 shows a complete 4-phase clock generator using a TTL counter with a discrete component circuit to provide the gating and the necessary voltage level change for interfacing to the MOST circuits. This circuit operates at input frequencies up to 4MHz, giving a 4-phase clock rate of 1MHz. More sophisticated interface circuits could be used to provide a higher operating speed.

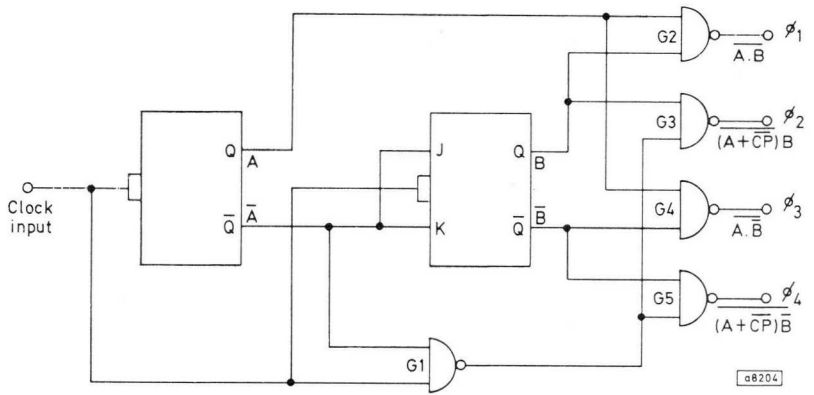


Fig. 8.13—Four-phase clock generator schematic

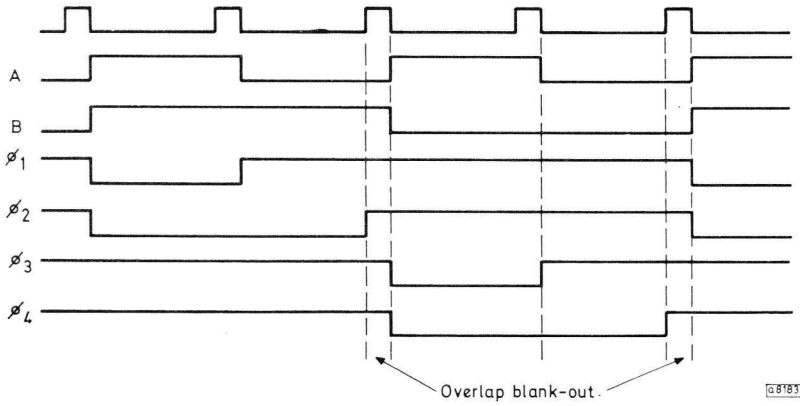


Fig. 8.14—Four-phase clock waveforms

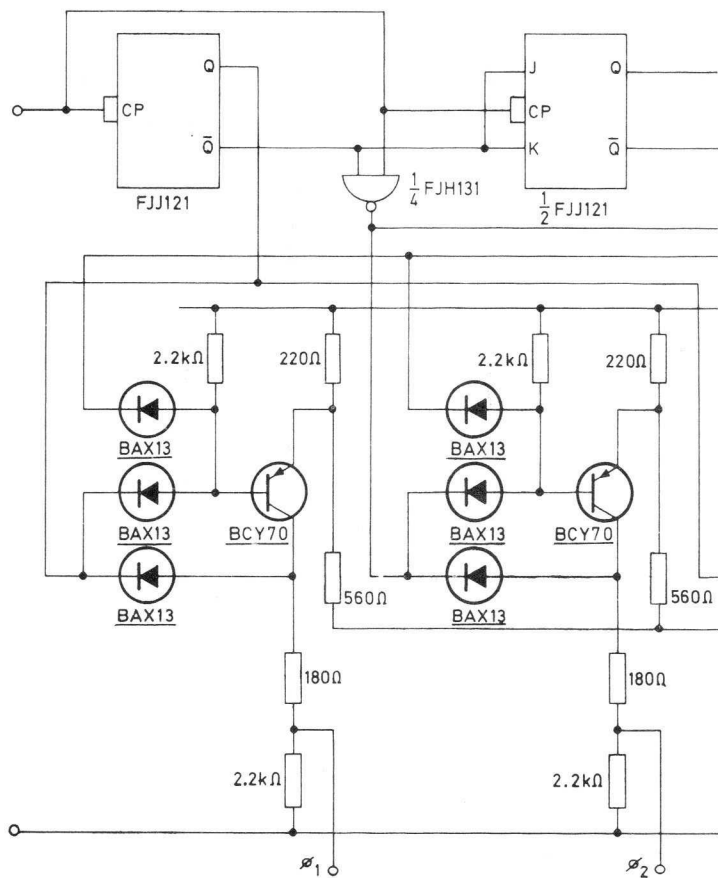
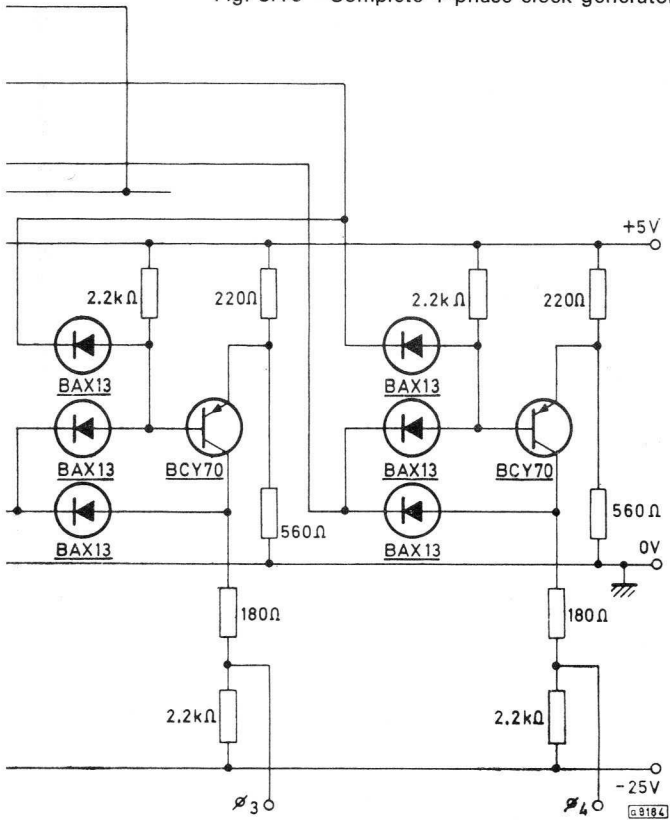


Fig. 8.15—Complete 4-phase clock generator



CHAPTER 9

INTERFACE CIRCUITS

Frequently, systems will be built which are partly MOS logic and partly bipolar circuitry. In this case it is necessary to have circuits designed to translate voltage levels from the 5V or 6V bipolar logic levels to the 10V to 25V levels associated with MOST circuits. Circuits for this purpose are called interface circuits.

The type of circuit used depends on the particular application, the factors to be considered being the required speed, capacitive loading, and which supply line is regarded as the system common line. Several methods of connection of supply and common rails at the input and output of MOS circuits are possible, as shown in Fig. 9.1.

Operating speed of interface circuits

The operating speed of bipolar interface circuits depends on a number of factors including the available drive signal level, capacitive load, desaturation times and voltage swings. The definitions of the switching times referred to in this chapter are as shown in Fig. 9.2. The propagation delay t_{pd1} is defined, for an input interface circuit, as the time taken from the instant the TTL or DTL gate input level is changed to the instant when the output level of the interface circuit reaches the threshold level from the '0' state. Similarly, t_{pd0} is the time taken for the interface circuit to reach the threshold level from the '1' state after the driving gate input level is changed.

INPUT INTERFACE CIRCUITS

Input interface circuits, positive rail common

Fig. 9.3 shows a simple p-n-p arrangement for interfacing from TTL or DTL to an MOS input. The DTL or TTL gate must be of the type with a passive (resistive) pull-up output circuit, or of the type where no load resistor is included in the gate. 'Totem pole' output gates must not be used. This circuit is suitable for low speed operation only, the operating speeds being as given below.

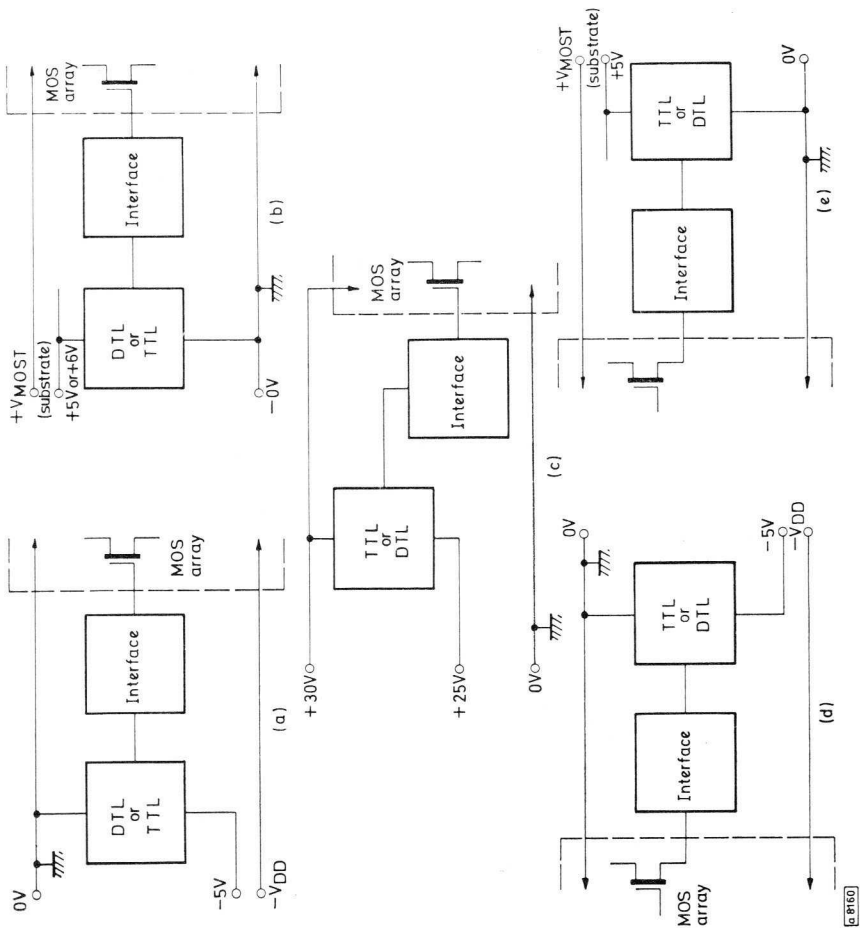


Fig. 9.1—Interface supply arrangements
 a), b), c) input
 d), e) output

Performance of Fig. 9.3 circuit

t_{d0}	35ns	} to V_T level
t_r	30ns	
t_{d1}	1000ns	
t_r	600ns	
t_{pd0}	≈ 60 ns	
t_{pd1}	$\approx 1.1\mu$ s	

These figures were achieved when driving normal MOS logic inputs representing only a few picofarads.

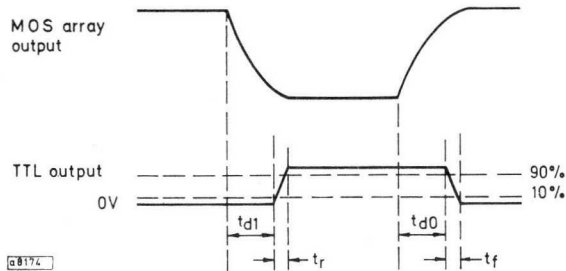
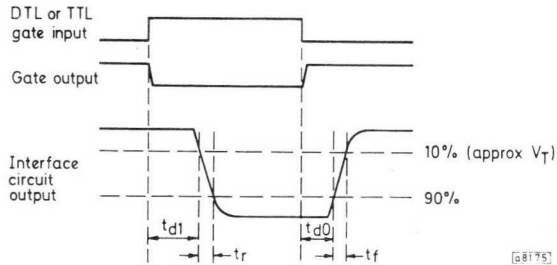


Fig. 9.2—Interface waveforms
a) input
b) output

The simple circuit discussed above benefits considerably in operating speed if the transistor is held out of saturation by means of a diode clamp (D_1 and D_2) as shown in Fig. 9.4. The inclusion of the diode clamp gives considerable improvement in t_{pd1} as shown below. See note on page 98.

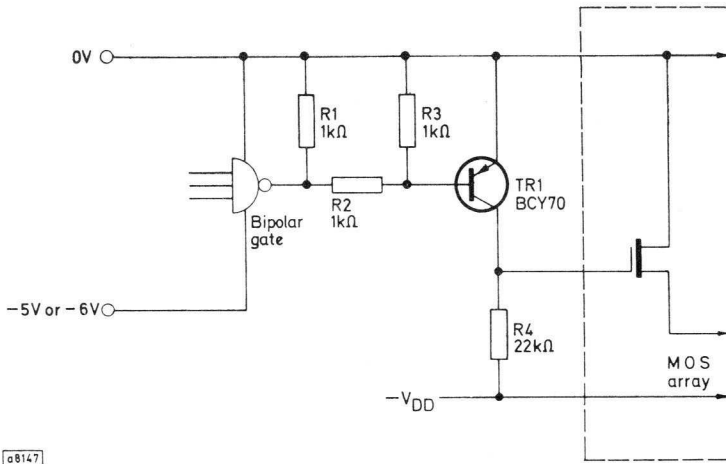


Fig. 9.3—Simple p-n-p input interface circuit

Performance of Fig. 9.4 circuit

t_{d0}	35ns	
t_f	50ns	
t_{d1}	80ns	
t_r	600ns	
t_{pd0}	75ns	} to V_T level
t_{pd1}	180ns	

Where high capacitive loads are to be driven, such as are associated with the clock lines of long shift-registers or the control lines of MOS stores, a more complex circuit is required if high speed operation is to be achieved. Fig. 9.5 shows a circuit using an active pull-up stage and incorporating antisaturation diodes. This circuit is considerably faster than the two simple circuits described above even when driving capacitive loads.

Performance of Fig. 9.5 circuit

	MOS logic load	200pF Capacitive load
t_{d0}	7ns	10ns
t_f	18ns	35ns
t_{d1}	25ns	30ns
t_r	100ns	100ns
t_{pd0}	25ns	50ns
t_{pd1}	30ns	45ns

} to V_T level

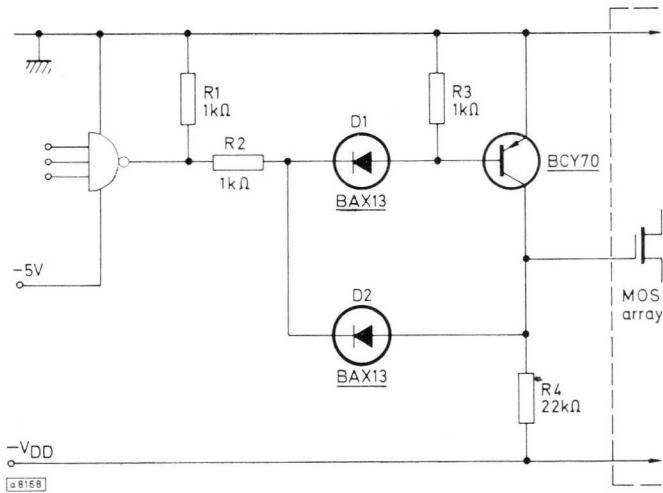


Fig. 9.4—Improved input interface

Input interface circuits, negative rail common

It may be necessary in some cases to use the V_{DD} rail as the line which is common to the MOS circuits and the low level logic. This situation normally arises only as a result of particular requirements at the output of the system. The use of the V_{DD} rail as the common line requires careful consideration since it can lead to a reduced system noise immunity. A simple interface circuit of this type is given in Fig. 9.6. The speed of the circuit is very dependent on the choice of the value of R_L and the transistor type.

Performance of Fig. 9.6 circuit (load = 15pF)

	$TR_1 = BC108$ $R_L = 22k\Omega$	$TR_1 = BC108$ $R_L = 2\cdot2k\Omega$	$TR_1 = BSX20$ $R_L = 2\cdot2k\Omega$
t_{d0}	$2\mu s$	$0\cdot7\mu s$	40ns
t_f	50ns	50ns	40ns
t_{d1}	20ns	20ns	20ns
t_r	$0\cdot5\mu s$	150ns	100ns
t_{pd0}	$2\cdot5\mu s$	850ns	140ns
t_{pd1}	$\simeq 30ns$	25ns	25ns

} to V_T level

Note that the BSX20 circuits are restricted to a 20V supply rail. Fig. 9.7 shows an n-p-n version of the p-n-p circuit given in Fig. 9.5 The input

circuit in this case consists of a diode shifting circuit rather than a resistive coupling circuit as in Fig. 9.5.

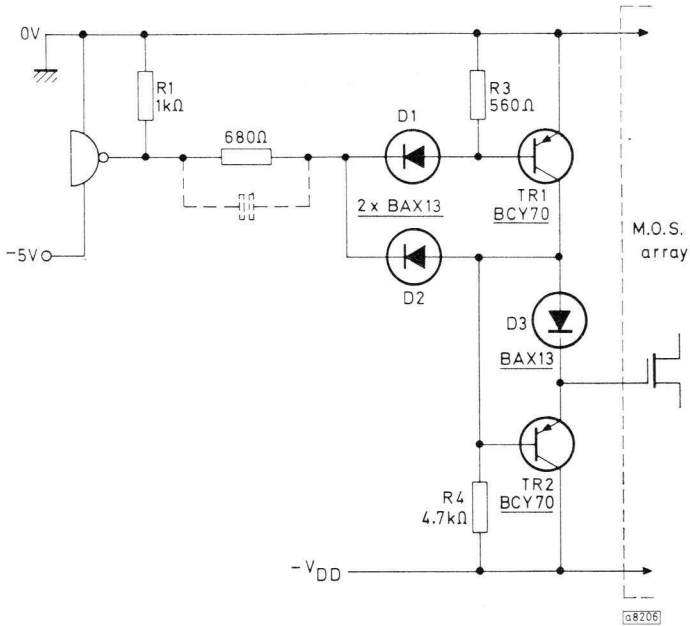


Fig. 9.5—Totem pole input interface with positive rail common

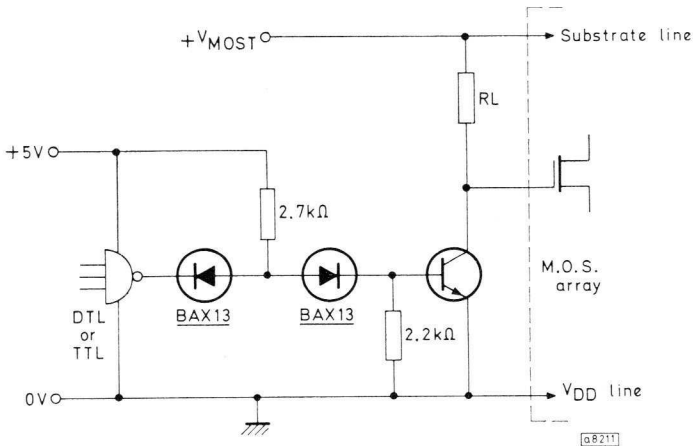


Fig. 9.6—Simple n-p-n input interface

Performance of Fig. 9.7 circuit using BSX21 transistors

	15 _p F load	200 _p F load
t_{d0}	7ns	20ns
t_f	80ns	120ns
t_{d1}	5ns	15ns
t_r	50ns	60ns
t_{pd0}	6ns	80ns
t_{pd1}	10ns	20ns

Note that in interface circuits using antisaturation clamps (Figs. 9.4, 9.5, and 9.7) diode D_1 may be omitted if D_2 is a fast germanium type operating within its temperature range.

Direct input interface circuits

It is possible to interface directly from certain DTL and TTL gates such as the FJH311 and FJH321 into an MOS array. With open collector gates which are rated for operation up to 12V on the output stage the circuit arrangement shown in Fig. 9.8 may be used. This arrangement, while providing a simple interface, is complicated by the need for an additional supply rail.

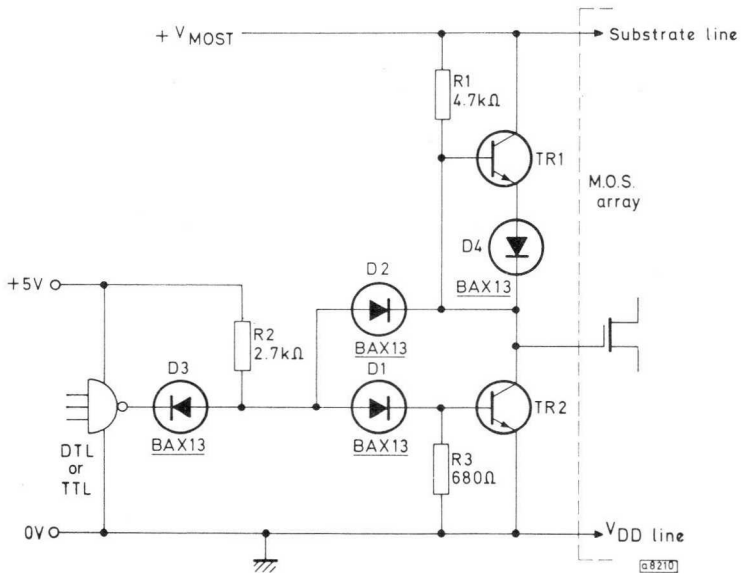
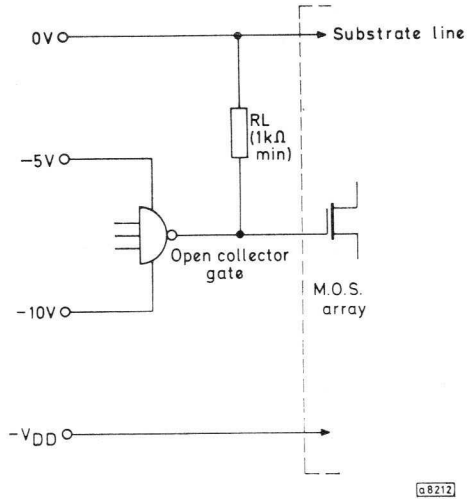


Fig. 9.7—Totem pole input interface, n-p-n version

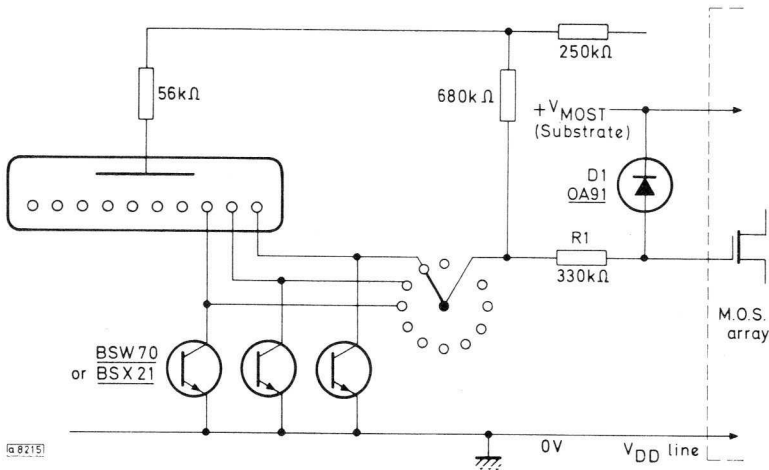
Fig. 9.8—Direct input interface



□ 8212

Input interface from indicator tubes

When information is displayed on gas discharge numerical indicator tubes it is possible to interface with a resistive circuit from the display cathodes to an MOS circuit. Fig. 9.9 shows this arrangement. Resistor R_1 ensures that non-conducting cathodes are held high, and R_1 and D_1 prevent the input of the MOS array from being damaged by positive inputs.



□ 8215

Fig. 9.9—Input interface from indicator tube

OUTPUT INTERFACE CIRCUITS

The output stage of an MOS array usually consists either of an open drain device with source connected to substrate, or an inverter stage including a load MOST (Fig. 9.10). The characteristics of these output stages depend on the physical size of the device used, but in broad terms they may be regarded as a current source which is either on or off. The available current is subject to variation due to normal production spreads, and when considering the requirements for output current from MOS devices this must be taken into account.

In Fig. 9.10a, the effective gate voltage applied to TR_3 when TR_2 is off is given by

$$V_{G(\text{eff})} = V_{DD} - 2V_T.$$

Thus, if we consider a circuit operating with a nominal 22V supply with a $\pm 10\%$ tolerance, and a spread in V_T of 2V to 5V, we have:

$$V_{G(\text{eff})\text{min}} = 20 - (2 \times 5V) = 10V$$

$$V_{G(\text{eff})\text{max}} = 24.2 - (2 \times 2V) = 20.2V.$$

If we now add to this the effect of a 2:1 spread in β_0 , (that is, 5 to $10\mu\text{A}/\text{V}^2$), the total spread in available current from TR_3 could be as much as 8:1. In practice the spread is less than this because of the series resistance of the p-diffusion in the source circuit which provides negative feedback, and in designing the output stages of MOS arrays this effect may be deliberately increased (Fig. 9.11) to reduce the current spread and thereby limit the power dissipation of the output stage to a satisfactory level.

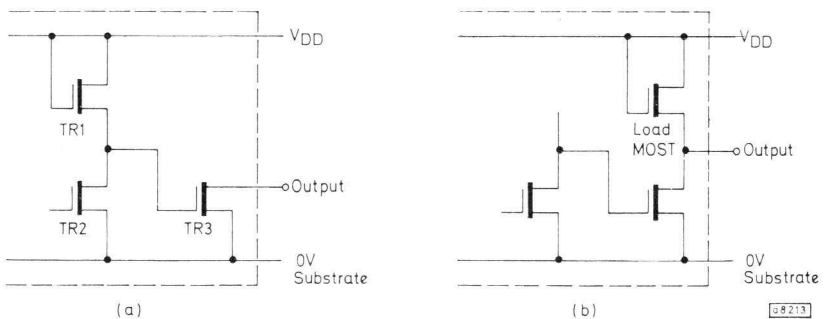


Fig. 9.10—Basic MOST output circuits

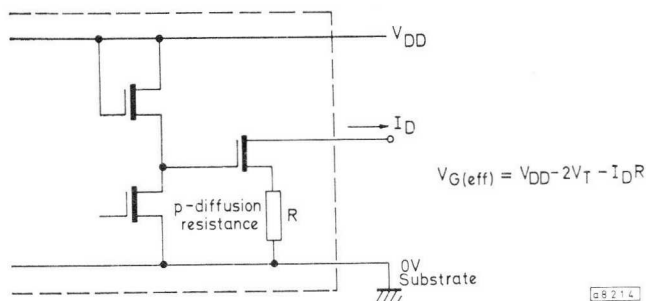


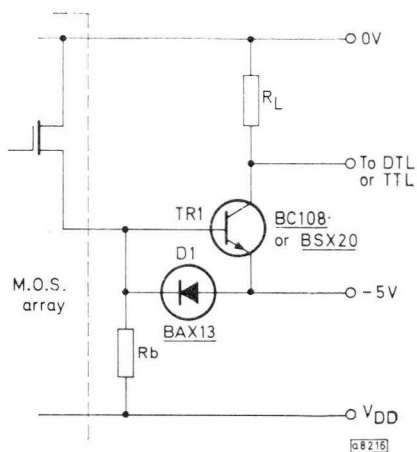
Fig. 9.11—Source resistance to limit output dissipation

Simple output interface, positive rail common

A simple output interface circuit using the substrate line as a common rail for the MOS and the bipolar logic is shown in Fig. 9.12. The operating speed depends on the size of the output MOS device and its effective gate drive voltage, as well as the transistor type and circuit values.

Typically, with an output MOST having an aspect ratio W/L of 4 and $R_b = 100k\Omega$, propagation delays of 70ns are achieved with the BSX20. If a BC108 is used, t_{pd0} is 100ns, and t_{pd1} is approximately $1.2\mu s$.

Fig. 9.12—Simple output interface circuit



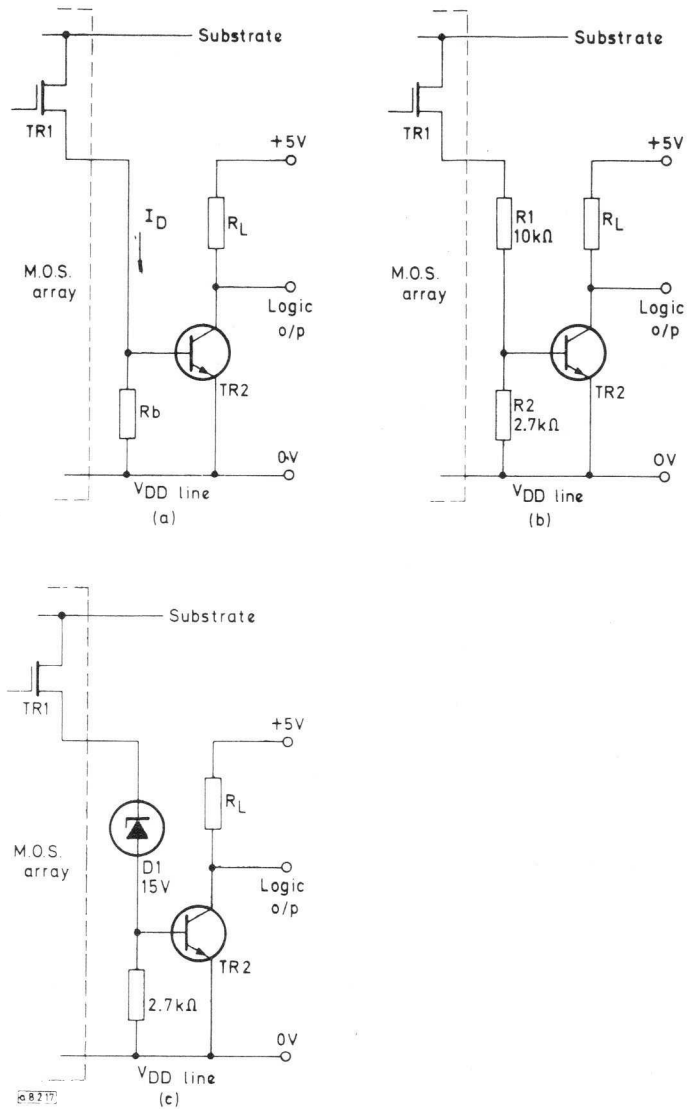


Fig. 9.13—Output interface circuits with negative common rail

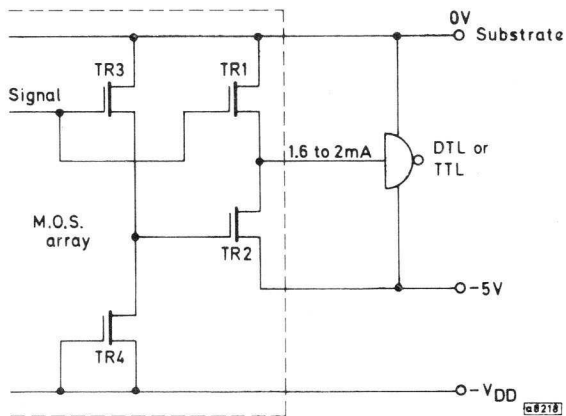


Fig. 9.14—Direct output interface

Simple output interface, negative rail common

A possible output interface circuit could be as shown in Fig. 9.13a. In this case the MOS device turns current on and off to the base of TR₂. In this circuit the MOST TR₁ supplies base current to the bipolar device TR₂. In the ON state, however, almost the full supply voltage is supported by the MOS transistor, leading to high dissipation. In Figs. 9.13b and 9.13c, some of this voltage is taken up by an external resistor or voltage regulator diode. Figs. 9.13b and 9.13c have typical average propagation delays of 150ns with BSX20 transistors.

DIRECT OUTPUT INTERFACE CIRCUITS

MOS arrays can be designed to be directly compatible with DTL or TTL. In this case the MOS output must be capable of sinking a current of 1.6mA with an output voltage of 0.4V for TTL compatibility. To feed DTL, a current of 2mA at 0.6V is satisfactory. The output circuit arrangement is as shown in Fig. 9.14.

When the MOS logic 'signal' is high (that is, negative) TR₃ and TR₁ are turned on, and TR₂ is held off. The input to the logic circuit is therefore high. When the MOS 'signal' is low, TR₁ and TR₃ are off, and TR₂ is turned on via the load MOST, TR₄. Transistor TR₂ is a very large device and must have an ON resistance of less than 250Ω, including the diffusion resistance. This type of device would normally have an interdigitated or comb geometry to provide the necessary W/L ratio. Because of the large size of the device, the output speed is low, since the gate capacitance of such a structure could be some 5pF, and this has to be charged via TR₄.

For this type of device the crystal area necessary could be as much as $250\mu\text{m} \times 300\mu\text{m}$, and this therefore represents a costly solution. The size also limits the number of such outputs which can be accommodated on a chip, and circuits with more than say five such output circuits would probably be uneconomical, when the additional cost of the MOS array is compared with the cost of adding external interface circuits.

Direct output stages for feeding low power TTL where the input current requirement is only some $200\mu\text{A}$ are a feasible proposition, and can be achieved with much smaller devices and therefore without a severe economic penalty.

CHAPTER 10

INPUT PROTECTION

MOSTs at the input of an array require special precautions to prevent damage (thin oxide breakdown) to the gate by high voltages which may be applied during handling. These voltages may arise as electrostatic charge on tools, such as soldering irons, or may be due to the person handling the devices having become charged to a high voltage by friction between clothing and insulated chairs. The charge on a person may reach several kilovolts, and may be retained for some time if shoes with synthetic soles are worn.

To protect the MOS arrays against electrostatic voltages at the inputs, a special input protection device is associated with each input bonding pad. This device is an avalanche breakdown device, which is designed to protect against overvoltage and the short duration high current surges which may be associated with excessive voltage inputs. The device is designed so that it can be incorporated in the normal manufacturing process without the need for additional processing steps. Several forms of breakdown protection device may be incorporated, including:

- 1) Avalanche bulk breakdown
- 2) Gated diode
- 3) Thick oxide MOST.

Avalanche bulk breakdown device

This form of breakdown is the avalanche breakdown of a reverse biased p-diffusion to the substrate in which it is contained. It occurs at some 60 to 70V. In a simple structure, such as Fig. 10.1a, there is a relatively high series resistance between the point of breakdown and the substrate contact. This produces a voltage drop when avalanche current flows, and gives a soft breakdown characteristic.

If a second p-diffusion area is inserted near the first, as shown in Fig. 10.1b, and this diffusion (B) is earthed, the current path after breakdown has occurred between region A and the substrate is the short path between

A and B to earth, rather than the long path through the substrate to the substrate back contact. This form of device provides a sharp breakdown characteristic.

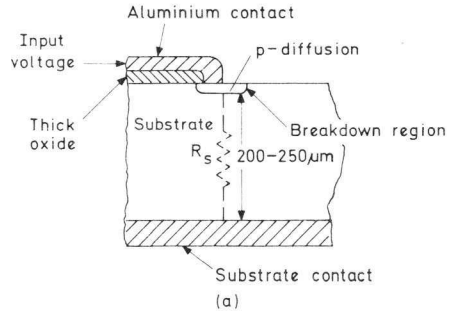
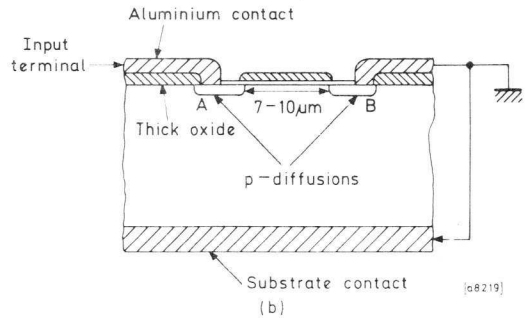


Fig. 10.1—Bulk breakdown
 a) simple structure
 b) low-resistance device



Gated diode protection device

If a p-diffusion is covered by thin oxide over which is an earthed aluminium layer such as in Fig. 10.2, the presence of the earthed aluminium

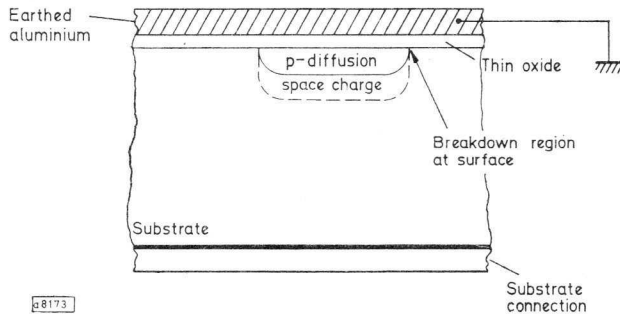


Fig. 10.2—Gated diode

modifies the breakdown characteristic of the p-n junction near the surface of the structure. The effect is to reduce the breakdown voltage at that point to about 40 to 50V.

Complete input protection device

A practical input protection circuit contains both the above forms of device, separated by a resistor. The circuit is arranged to provide a progressive breakdown as the input voltage is increased. The output of the protection device is connected to the gate circuits of normal logic MOSTs, and when the protection devices are in operation the voltage applied to these gates is held within safe limits.

The equivalent circuit of a complete input protection device is shown in Fig. 10.3. The voltage regulator diodes represent the avalanche breakdown of the device and the various resistors r are the distributed circuit resistances.

The resistor R (normally $1k\Omega$ to $2k\Omega$) is deliberately inserted as a p-diffused region. This resistance ensures that as the current through the gated diode increases, the voltage drop across R also increases and the bulk breakdown diodes are brought into effect. A practical layout for an input protection device might be as shown in Fig. 10.4.

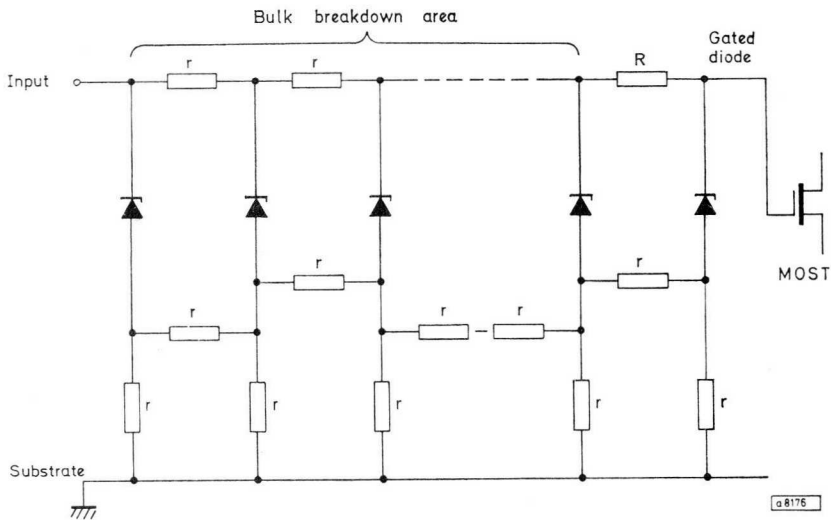


Fig. 10.3—Equivalent circuit of complete input protection device

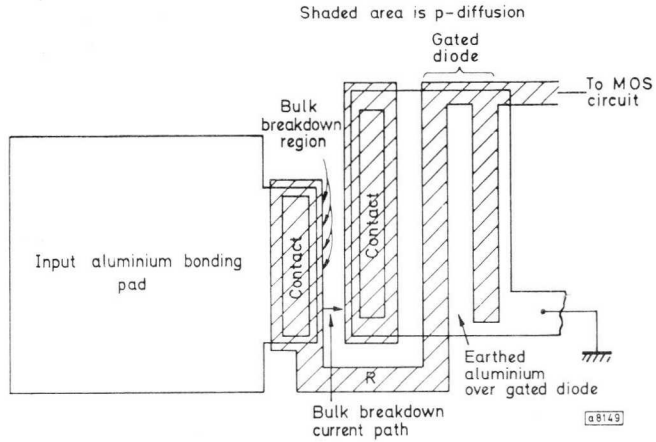


Fig. 10.4—Input protection device

Thick oxide MOST

Additional input protection can be obtained by connecting a MOST as shown in Fig. 10.5. This device is made with thick oxide gate insulation and has a high threshold voltage, say 50V. When this voltage is exceeded on the input the MOST turns on and input current flows through the channel to substrate, thereby limiting the input voltage to a safe level.

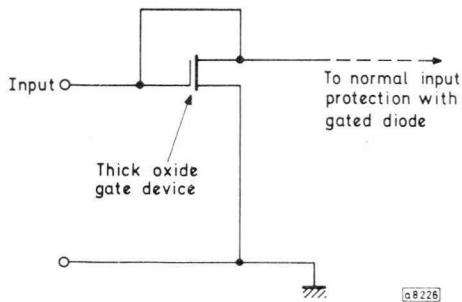


Fig 10.5—Additional input protection

CHAPTER 11

MOS LOGIC APPLICATIONS

This chapter outlines a number of typical applications which are admirably served by MOS integrated circuits. In general, MOS arrays contain a large amount of logic and are most suited to fairly complex systems. Simpler systems are frequently best built with bipolar logic circuits. For equipments which are to be produced in small quantities, or where it is desirable to have the ability to modify the logic for particular requirements, the bipolar approach often will provide the most economic solution.

SHIFT-REGISTER APPLICATIONS

The shift-register is probably the most widely used MSI (medium-scale integration) logic array device. The main uses of shift-registers are for

- 1) Delay elements
- 2) Counting circuits and timing dividers
- 3) Temporary data storage.

Other applications are in

- 4) Arithmetic units
- 5) Conversion from parallel to serial modes or serial to parallel modes.

Of these, all but conversion between parallel and serial modes may be accomplished by the use of MOS shift-registers. In parallel/serial conversion it is necessary to have access to the input of individual stages, and for conversion from serial to parallel each output is required. These requirements place severe limitations on the package requirements and also, because of the need for extra bonding pads and output buffers, the chip size of such a device would be much larger than that of a normal serial shift-register with only the final and maybe a few interstage connections brought out. Serial/parallel or parallel/serial conversion is feasible up to about 10 bits with present-day packages.

Shift-registers as delay elements

Data entered into a shift-register is passed from stage to stage at each clock pulse. Thus, data entered into a 256-bit shift-register appears at the output 256 clock pulses later. The 'FD' dynamic MOS shift-registers provide a versatile range of elements for use in delay applications.

The FDN126 and FDN136 may be arranged to provide an effective shift-register length of any number of bits between one and 64. Fig. 11.1 shows a block diagram of the FDN136 single-phase dynamic shift-register which operates up to 1MHz. (The FDN126 is similar but operates with a 2-phase clocking system, and has a maximum shift rate of 3MHz).

The control lines A_1 to A_6 determine the active length of the shift-register. A logical '1' (negative) applied to a control input 'enables' the previous delay stage. A logical '0' (zero volts) causes the previous section to be bypassed. As an example, Fig. 11.2 shows the connections necessary to make a 26-bit delay.

In many applications it is necessary to recirculate the information held in a shift register (Fig. 11.3a). Fig. 11.3b shows two methods of connecting recirculating gates.

Shift-registers as counters and dividers

The simplest form of counter or timing divider is the ring counter, such as is shown in Fig. 11.4. Control circuits are necessary to enter a single '1' into the register. This '1' is then recirculated through the register and appears at the output at intervals of 'n' clock pulses, where 'n' is the number of stages in the shift-register.

Fig. 11.5 shows a possible arrangement of a shift-register with gating to provide for reset and to allow a single pulse to be entered. Gates G_1 and G_2 form a bistable circuit which may be set or reset by switch S_A . When S_A is in the 'clear' position the input to the shift-register is held at a logical zero, and the register can be filled with zeros. When S_A is set to 'run', gate G_3 is enabled, and at the same time the monostable is triggered to provide a narrow single pulse to enter the shift-register. This single pulse is then recirculated under the control of the clock pulses.

Fig. 11.6 shows a ring counter with direct TTL interfacing. By modifying the circuit arrangement the shift-register can be converted to a Johnson or twisted ring divider as in Fig. 11.7, giving a cycle length of $2n$ clock pulses where 'n' is the number of stages in the shift-register. The interface circuit design will depend on the gate types used.

For division by large numbers, shift-registers may be cascaded or connected as synchronous dividers. The cascading of shift-registers is only really feasible with static types. Two static shift-registers connected in cascade, with the output of one providing the clock for the second,

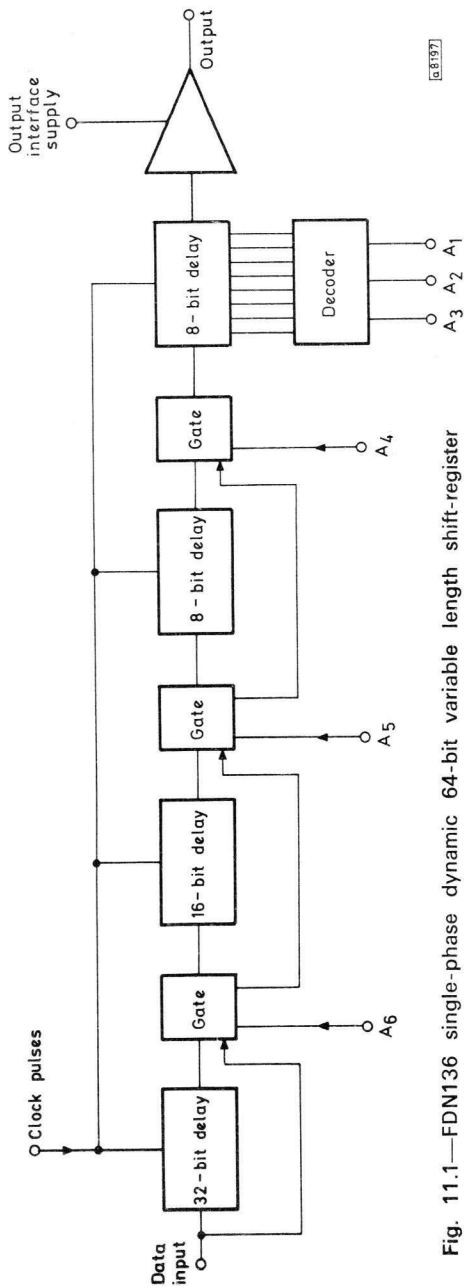


Fig. 11.1—FDN136 single-phase dynamic 64-bit variable length shift-register

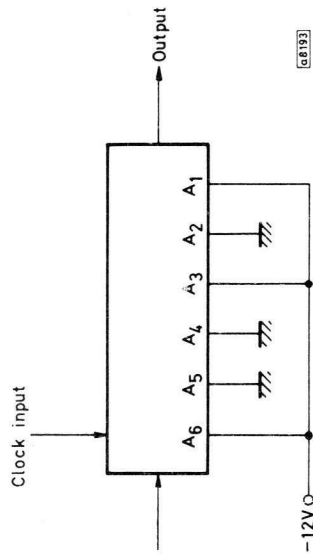


Fig. 11.2—FDN126/136 arranged as a 26-bit delay

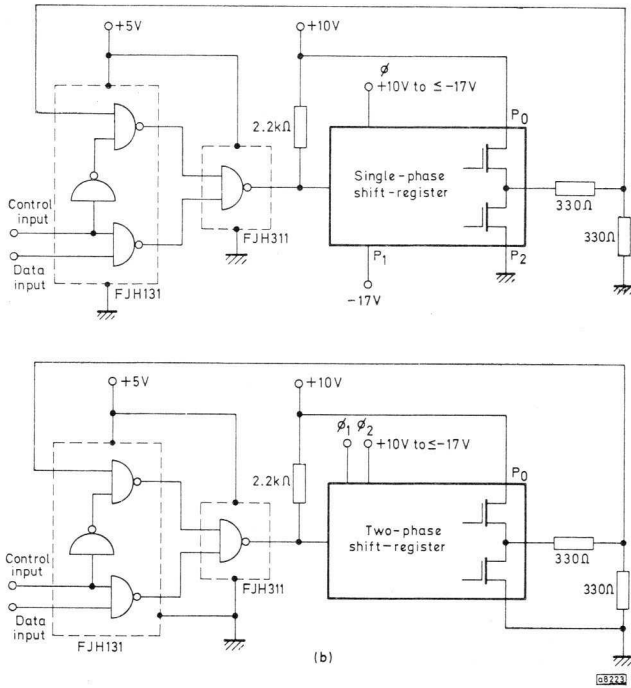
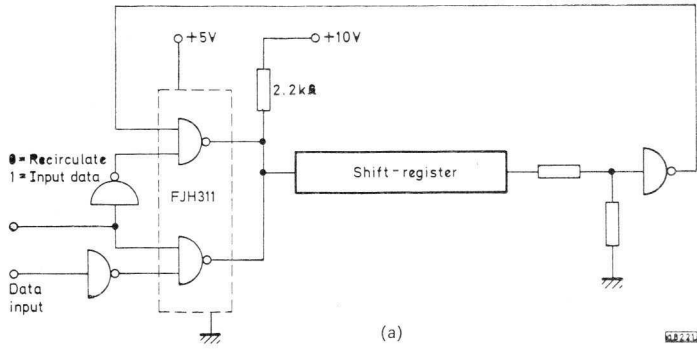


Fig. 11.3
 (a) Recirculation in shift register
 (b) Methods of connecting recirculating gates

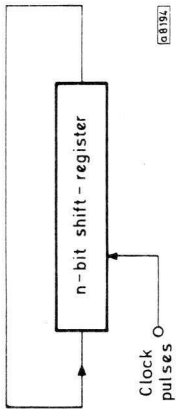


Fig. 11.4—Ring counter divider

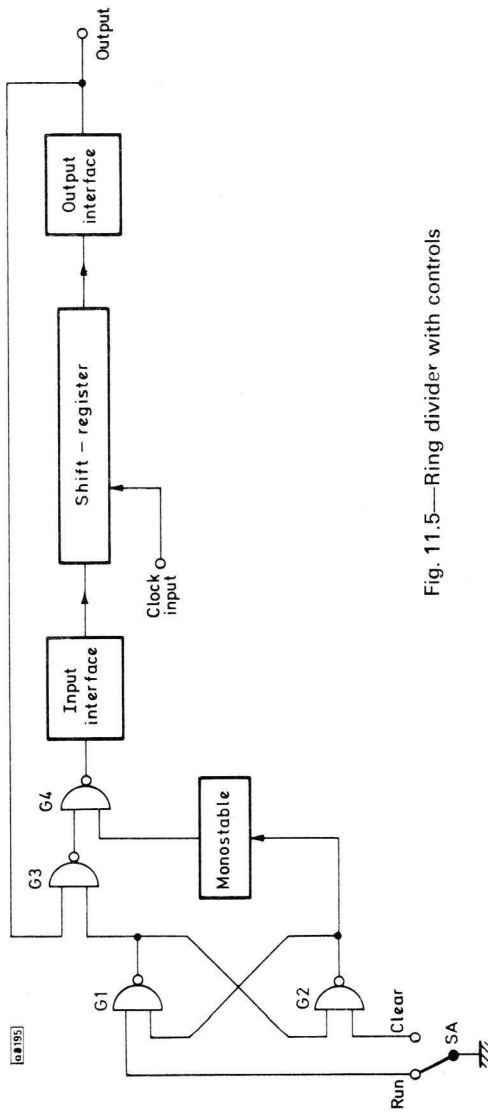


Fig. 11.5—Ring divider with controls

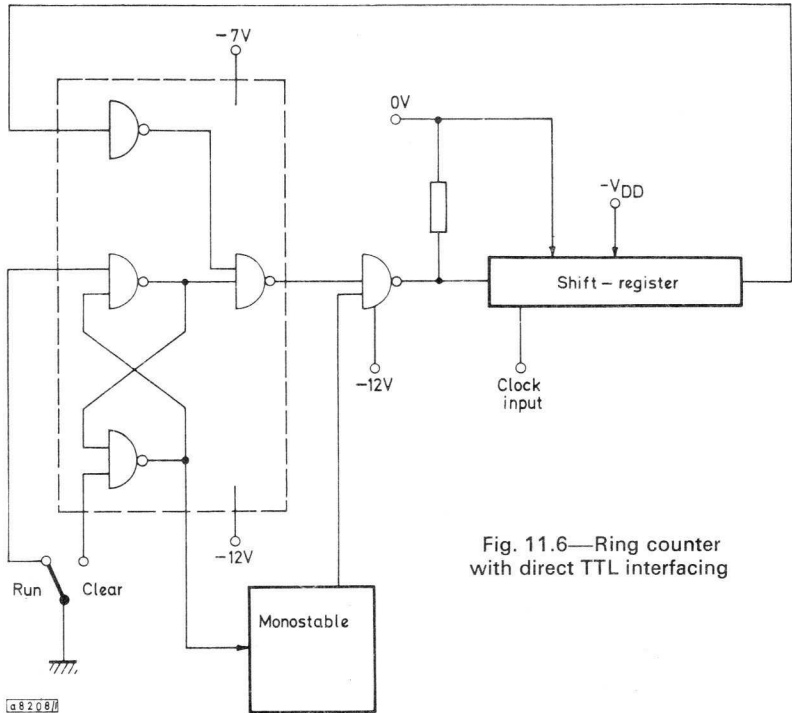


Fig. 11.6—Ring counter with direct TTL interfacing

will provide a division of the original clock pulse rate by $4N_1N_2$. Fig. 11.8 shows an example of such a system.

With dynamic shift-registers, a different system is required. One method is to use coincidence gating as shown in Fig. 11.9. Here, the shift-registers have lengths of 63 and 64 bits. When each shift-register is recirculating a single '1', these '1's coincide at the outputs at intervals of 63×64 pulses, giving an effective division of 4032.

Shift-registers as storage elements and memories

For many data storage applications where a capacity of up to a few thousand bits is required and rapid access is not necessary, a serial memory formed of MOS shift-registers provides an economic solution. In some cases it may be used simply as temporary storage in sequential systems where data is entered at the shift-register input, and after passing through the register it is used and then discarded. This type of application is really only an extension of the use of shift-registers as delay elements. More frequently, in storage applications the data will be recirculated through the shift-register and read out (non-destructively) when required.

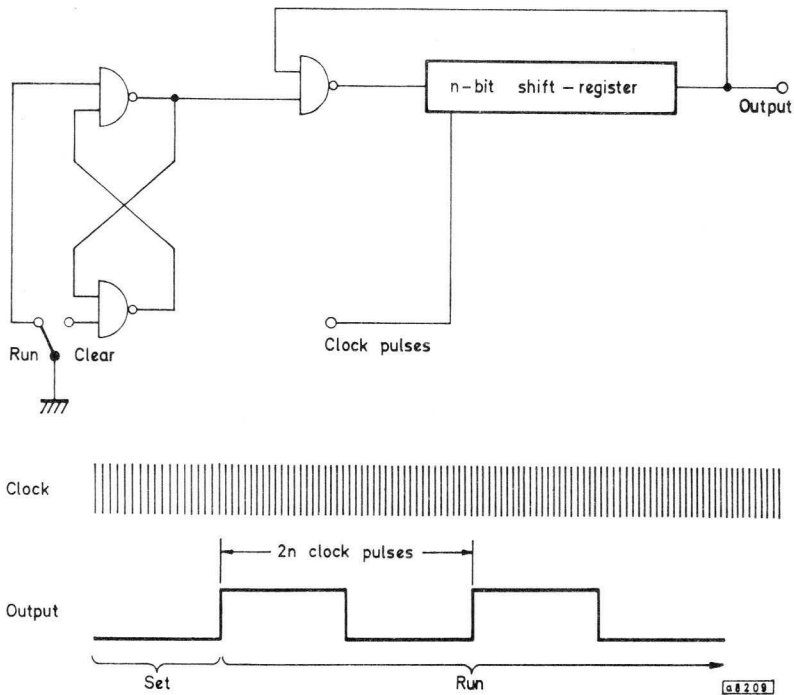
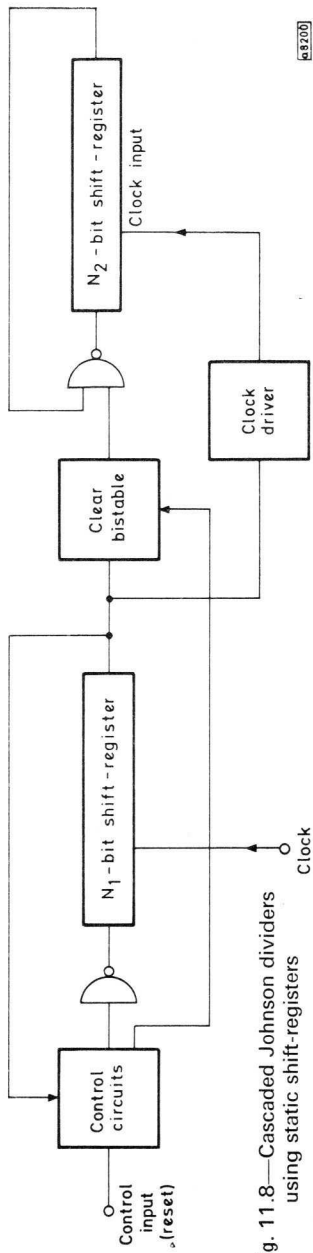


Fig. 11.7—Johnson or twisted ring divider

There are two possible basic ways of organising shift-register memories, as shown in Fig. 11.10. In Fig. 11.10a the data is held in a completely serial fashion, and is read out one bit at a time, taking n clock pulses to read out an n -bit word. In Fig. 11.10b a number of shift-registers, say 16, are used in parallel. Sixteen-bit words are then entered in parallel form and read out in parallel as required. This form of memory obviously provides much more rapid access than the serial arrangement.

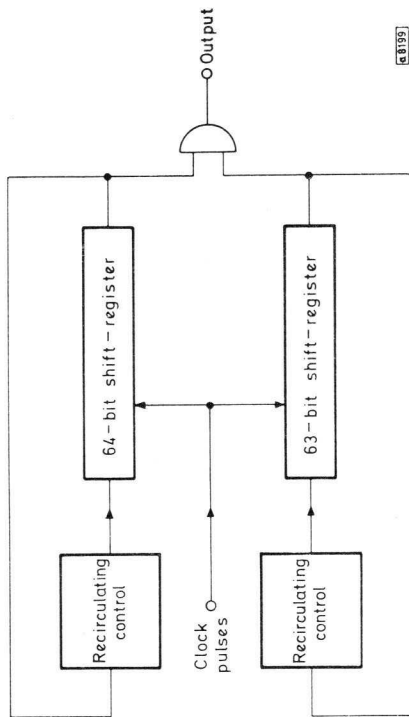
In either form of organisation it is necessary to have additional control circuits for the memory. The most important requirement in order to use any form of memory is that one must know where, in the memory, particular sections of data are held. In other words, data must be capable of being inserted at a particular address in the memory, and must be capable of being retrieved by examining the same address. In a serial memory the addressing function is provided by the use of an address counter which is operated in synchronism with the shift-register.

Fig. 11.11 shows a block diagram of a recirculating memory operating in the serial mode. The 256-bit shift-register holds 16 words, each of 16 bits.



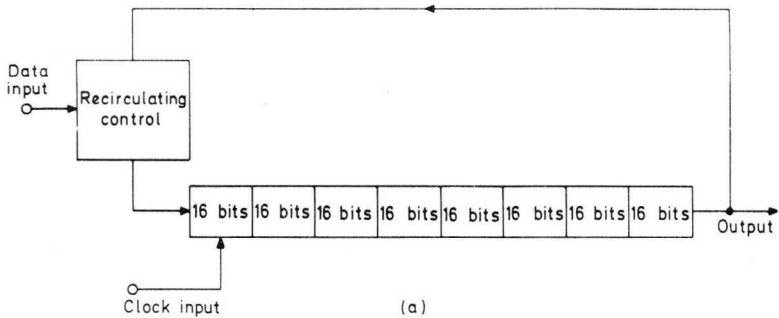
68700

Fig. 11.8—Cascaded Johnson dividers using static shift-registers

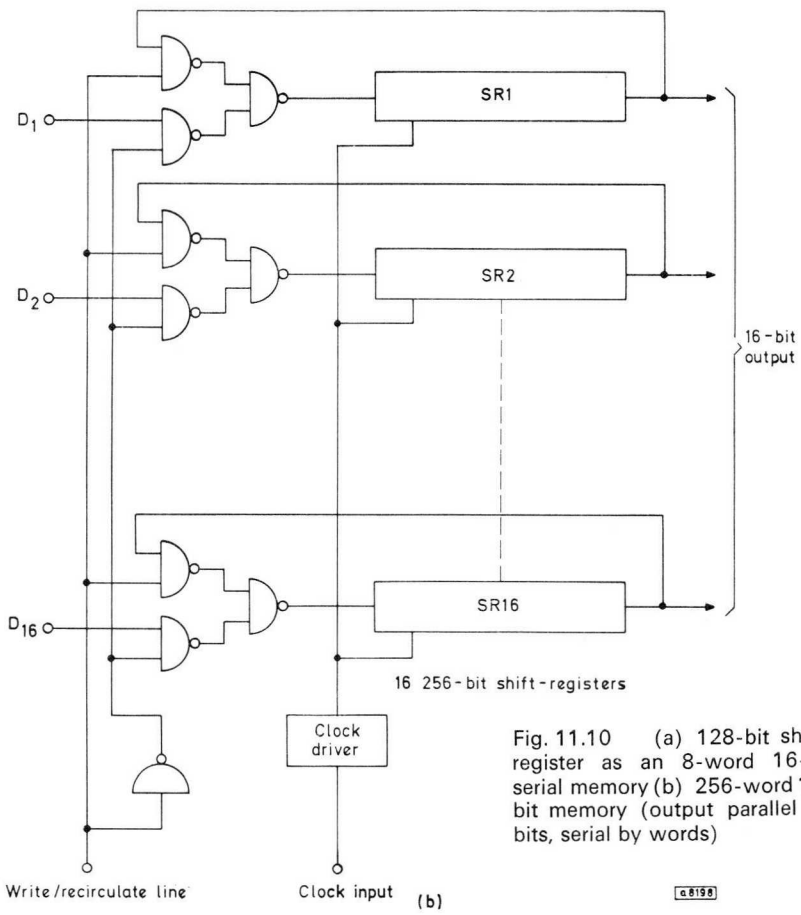


68195

Fig. 11.9—Division by 4032 using coincidence gating of two dynamic shift-registers



(a)



(b)

Fig. 11.10 (a) 128-bit shift-register as an 8-word 16-bit serial memory (b) 256-word 16-bit memory (output parallel by bits, serial by words)

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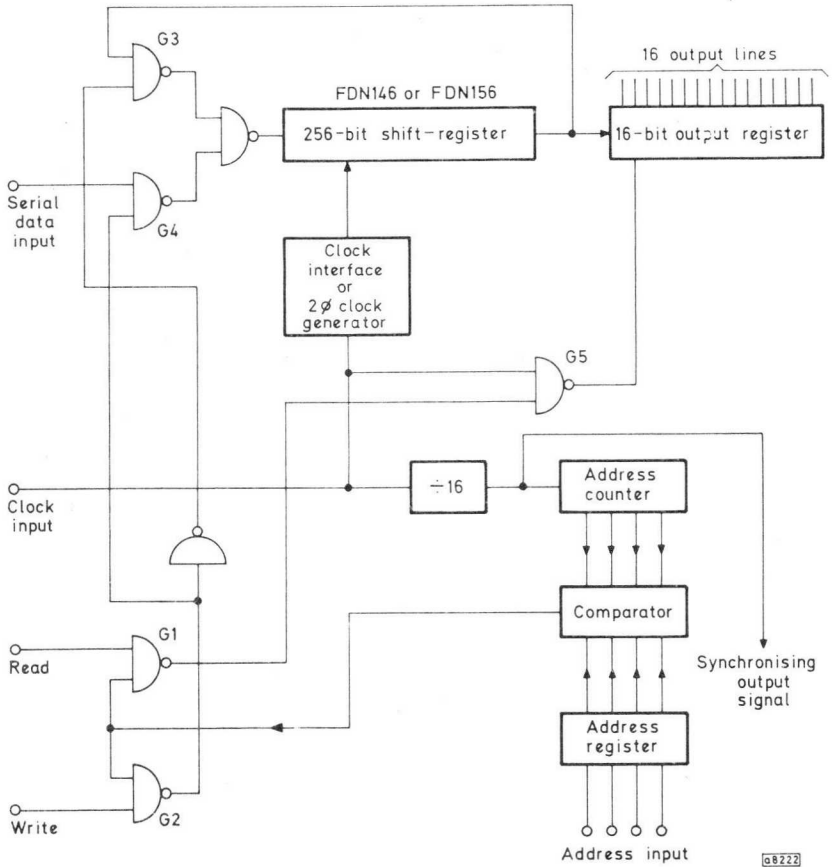


Fig. 11.11—Schematic of 16-word 16-bit serial memory

The clock input feeds the shift-register via any necessary interface circuits, and at the same time it is divided by 16 and fed to a 4-bit address counter. The required address is inserted into a holding register and compared with the contents of the address counter. When the counter reaches the desired address, an output from the comparator enables gates G_1 and G_2 . If the system is in the 'write' mode, G_2 is opened and G_1 remains closed. Gate G_3 closes, preventing further recirculation of data, and G_4 is opened, allowing new data to be fed in. In the 'read' mode, G_1 is opened for a period of 16 clock pulses as soon as the address comparator is satisfied, and allows 16 clock pulses to be fed to the output register. The

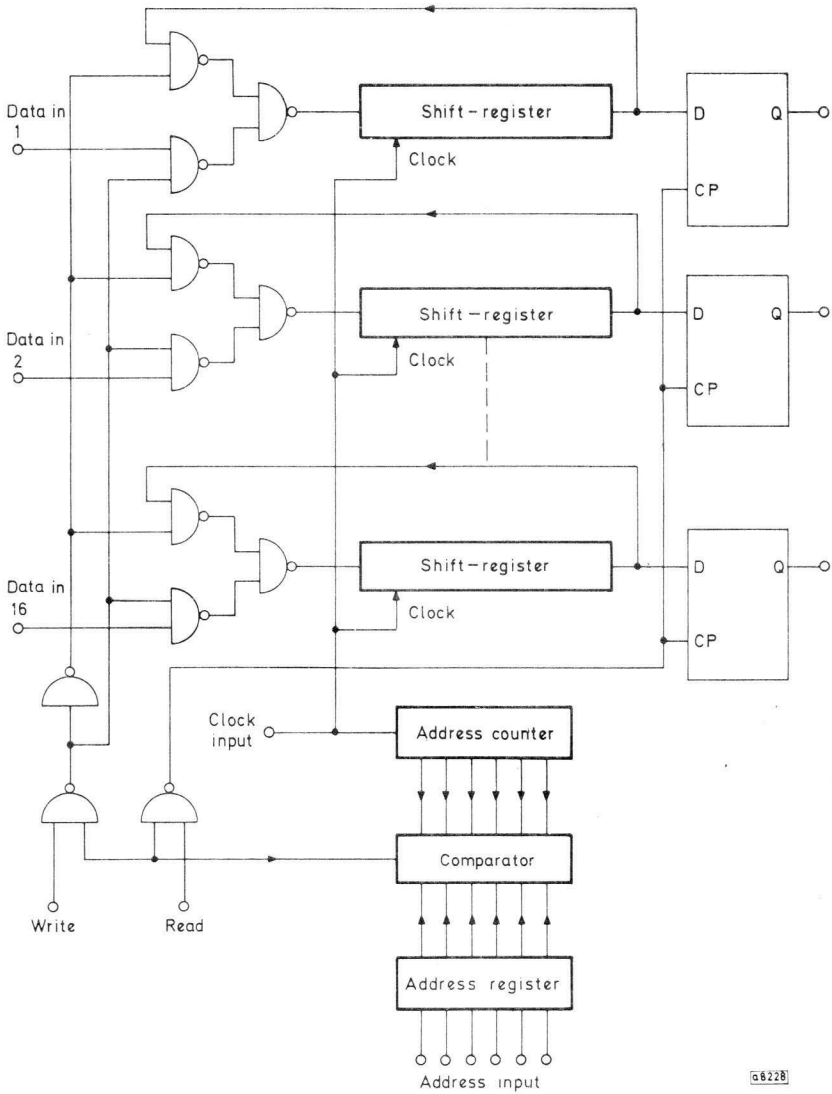


Fig. 11.12—Parallel output serial memory block diagram

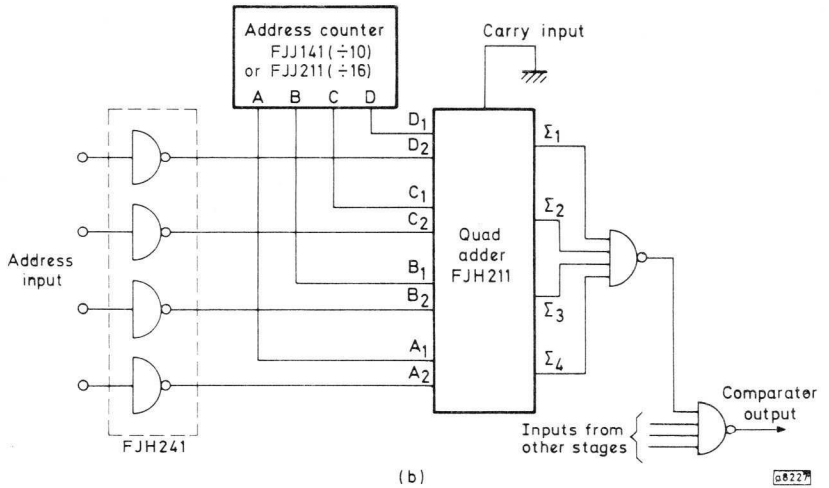
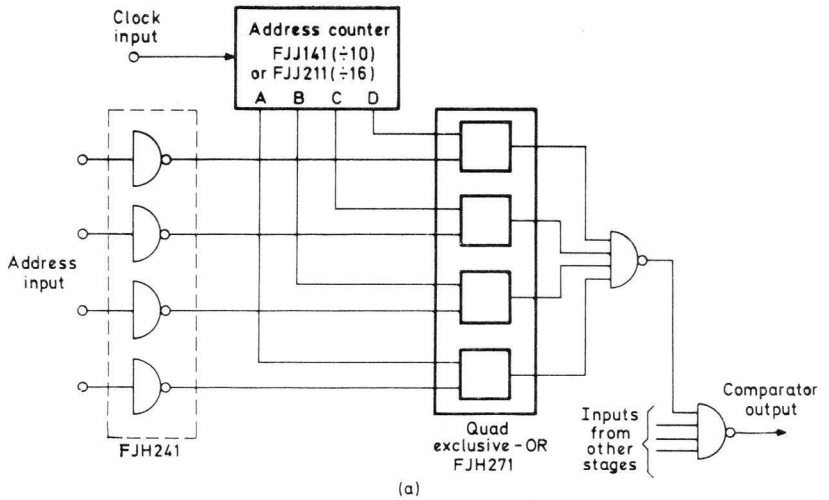


Fig. 11.13—Address comparators using TTL complex functions

appropriate 16 bits of data are fed into the output register but are at the same time recirculated to the input of the main register. A synchronising signal from the $\div 16$ stage feeding the address counter is used to ensure that an address cannot be written into the address register at any time other than at the beginning of any complete 16-bit period.

Fig. 11.12 shows a similar arrangement for a serial/parallel recirculating memory. The register output data is strobed into 'D' bistables under the control of the comparator output signal which in this case lasts for only a single clock period. Input data, in the 'write' mode, is strobed into the register, also by means of the address comparator output. Two possible configurations of the address comparator section using TTL complex packages are shown in Fig. 11.13.

Shift-registers in alarm systems

By using a signal-scanning system to examine a number of input data sources sequentially, and comparing the data from the current scan with that from the previous scan, any changes in the states of the input signals between scans can be detected. This type of system can be used to form the basis of an alarm system suitable for such applications as process control, and burglar or fire alarms. The basis of such a system is a serial memory, for example as shown in Fig. 11.11 or Fig. 11.12, the number of bits per word being dictated by the number of levels to be detected from each scanned input. In many cases a 1-bit per word organisation will be all that is necessary.

The simplest system for such applications is shown in Fig. 11.14. Data from the various sensing points are fed to a multiplex switch unit and are strobed into the shift-register under the control of the clock pulse. At the same time the multiplexed output is fed to a comparator circuit and compared with the shift-register output. The number of switch points

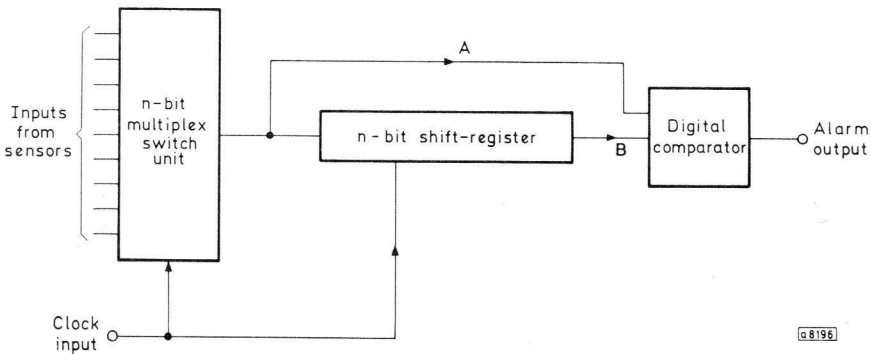


Fig. 11.14—Simple alarm system using MOS shift-register

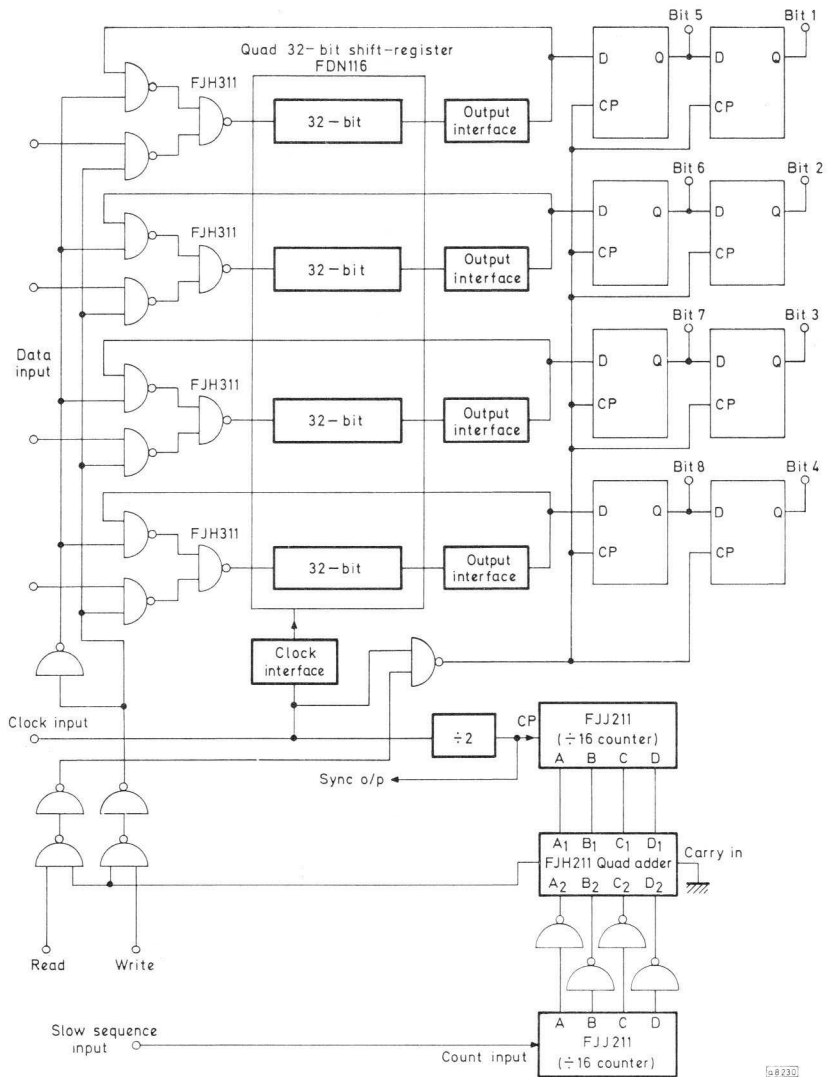


Fig. 11.15—Slow-sequence control memory using dynamic registers

is equal to the number of bits in the shift-register, therefore at each pulse the inputs to the comparator are from the same data point for current and previous scans. Any difference in these signals will be detected by the comparator and an alarm signal will be produced. If the system is extended to contain an address counter, suitable logic can be included to determine which transducer is producing an error signal. Further, in some cases two or three scans may be held in store and an alarm raised only if a number of scan sequences produce an error signal.

Shift-registers in slow sequencing controls

In applications such as machine tool sequencing control, the rate at which data is required by the control system is determined by its own mechanical response time. In some cases there may be several minutes between operations. In sequence controls based on static shift-registers the data can be shifted as slowly as one requires, but when dynamic shift-registers are employed, the data must be continuously recirculated at a comparatively rapid rate. In these cases the slow-speed operation is obtained by means of the addressing system. Fig. 11.15 shows a method of sequentially operating the address-counting logic for a register such as in Fig. 11.12. In this case the memory is organised in a serial/parallel mode. Two 4-bit words are read out for each address, giving a total capacity of 32 4-bit words or 16 8-bit words. The 'D' bistables used as the output store also act as a 2-bit shift-register. The rate of read-out is determined by the input rate to the address counter which can be from d.c. to half the maximum clock rate permitted by the shift-register (that is, d.c. to 500kHz with the FDN116 or d.c. to 1.5MHz with the FDN106).

OTHER APPLICATIONS OF SHIFT-REGISTERS

The following sections describe other applications of shift-registers.

Arithmetic functions

Arithmetic functions can be performed by using shift-registers as memories. The systems shown above can, for example, be used to feed binary adders to give a sequential addition. The main difference between the organisation of this type of unit and the basic recirculating store system is that when adding two binary numbers, the sum may replace one of the numbers, thereby making an economy in the number of registers used. Fig. 11.16 shows an example of such a system.

Display

In many forms of alpha-numeric display a recirculating store is used to refresh or update the information displayed. Here, shift-registers are frequently used in conjunction with read-only memories as character generators, as will be shown later.

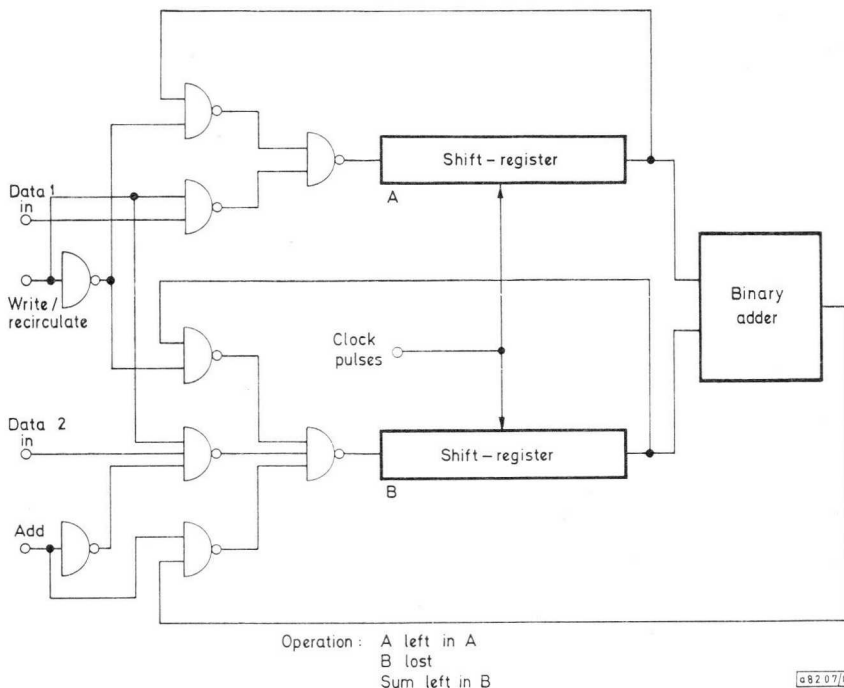


Fig. 11.16—Shift-registers used in binary serial addition

MOS IN COUNTING APPLICATIONS

MOS circuits frequently can provide considerable economies in counting circuits when compared with bipolar counters. However, there are some limitations particularly those associated with the number of pins available on a package. While it is possible to design, say, a 4-decade BCD counter and provide parallel outputs from a 24-lead package, this will in general not lead to the most economic solution.

System economies may be achieved by a multiplexing technique, where an MOS counter is designed to contain, say, four BCD decades and four 4-bit stores, but only four output lines are provided and these are internally switched sequentially to the outputs of the four decades. This leads to an economy in other parts of the system, such as when a display is required. Fig. 6.20 showed such a counter used to drive four display tubes. A single decoder circuit (BCD to decimal) is shared between the four display tubes, and the anodes of these display tubes are switched sequentially in syn-

chronism with the multiplexing signals fed to the counter circuit thereby ensuring that the output of decade 1 is displayed on tube 1, decade 2 on tube 2, and so on. This form of counter is suitable for use in many forms of digital instrument, but may also be used in control systems where the output is required to be fed into shift-registers or other forms of stores.

READ-ONLY MEMORY APPLICATIONS

The operation of read-only memories has been described in an earlier chapter. Applications for these devices include:

- 1) Fixed tables for use in calculating routines.
- 2) Fixed sequences for control logic.
- 3) Data routing control.
- 4) Decoding or code changing.
- 5) Display (as character generators).

Read-only memories may be either static or dynamic in operation. In general, the dynamic type provides a more economic chip design because of the smaller chip size. Power dissipation in dynamic types is also usually lower than in static types.

The contents of read-only memories may be customised or 'standard'. In the customised types the organisation of the memory, that is the number of words and the individual word-length, is fixed by the manufacturer, but the contents of each word are specified by the user.

CODE CHANGING

Code changers, or encoders or decoders, are essentially fixed logic arrays having a number of inputs and outputs. The output logic states are a fixed function of the input states.

One of the most common code-changing requirements is from 4-line BCD to 10-line decimal. This needs only a fairly simple arrangement and is best achieved by the use of standard bipolar integrated circuits. More-complex code changing, however, is economically achieved by the use of MOS arrays in the form of read-only memories.

An example of this type of code changing is the replacement of Selectric keyboard code by the ASCII code. The Selectric code is a 7-bit code and comprises 90 characters. The ASCII code is also a 7-bit code but in a code-changing application such as this the r.o.m. can also be programmed to provide additional outputs for odd or even parity, or both. The FDR106Z1 provides this function in addition to a number of other code-changing functions associated with display applications.

READ-ONLY MEMORIES IN DISPLAY SYSTEMS

The requirements of character generation for alpha-numeric displays where characters are generated in the form of a matrix of, say, 7×5 or 9×7 dots result in very large logic arrays. For a set of 64 characters of the form shown in Fig. 11.17, the conversion of a 6-line input to a code of 64 words, each of 35 bits, is required.

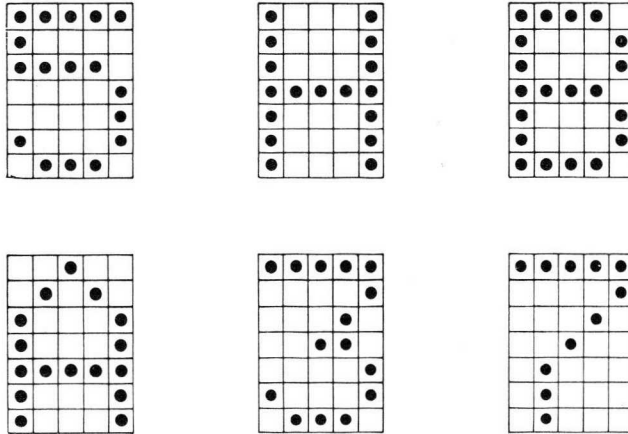


Fig. 11.17—Typical character forms on 7×5 matrix

Alpha-numeric characters of the matrix form are usually displayed either on cathode-ray tubes, using a television scan principle, or on a matrix display device such as the dot matrix tube. In either case the most economic circuit arrangements can be made when the characters are presented to the display device sequentially, row by row, or column by column.

The FDR116Z1 (Fig. 11.18) is a character generator read-only memory of this type. The characters are produced in a 7×5 matrix, and are presented at the output of the r.o.m. as a sequence of seven words each of five bits, that is, the characters are presented row by row.

The memory is arranged, in effect, in eight zones, though for character generation only seven are used. Each zone contains 64 words, each of five bits, corresponding to one row of each of the 64 characters held in the memory. The zones are addressed by three address lines, A_1 , A_2 and A_3 . The remaining address lines, A_4 to A_9 , are used to select the particular

required character within each zone. Thus to select, say, letter 'E' the address required is

A ₄	A ₅	A ₆	A ₇	A ₈	A ₉
1	0	1	0	0	0

Once this address is selected, A₁, A₂ and A₃ are sequenced through binary 000 to 111 (eight steps) to produce the complete character pattern, line by line; Fig. 11.19 makes this clear. The complete contents of the FDR116Z1 are shown in Fig. 11.20 (pages 130 to 133).

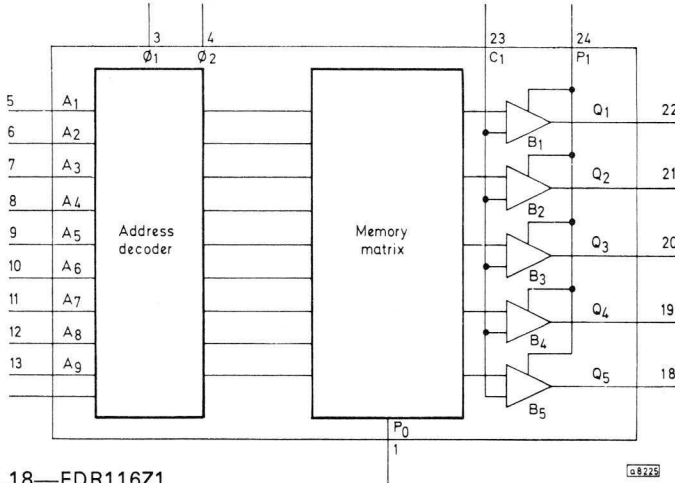


Fig. 11.18—FDR116Z1 read-only memory

Fig. 11.19—Selection of letter 'E' from FDR116Z1

Address		A ₄	A ₅	A ₆	A ₇	A ₈	A ₉																																																	
		1	0	1	0	0	0																																																	
Zone	A ₁	A ₂	A ₃	<table style="display: inline-table; border-collapse: collapse;"> <tr> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">2</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">3</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">4</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">5</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">6</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">0</td> <td style="border: 1px solid black; padding: 2px;">0</td> </tr> <tr> <td style="border: 1px solid black; padding: 2px;">7</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> <td style="border: 1px solid black; padding: 2px;">1</td> </tr> </table>				0	0	0	0	0	0	1	1	1	1	1	1	2	1	0	0	0	0	3	1	0	0	0	0	4	0	0	1	1	1	5	1	0	1	0	0	6	0	1	1	0	0	7	1	1	1	1	1	Word
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2	1	0	0	0	0																																																			
3	1	0	0	0	0																																																			
4	0	0	1	1	1																																																			
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6	1	0	1	Word 5																																																				
7	0	1	1	Word 6																																																				
8	1	1	1	Word 7																																																				

Raster scan alpha-numeric display systems

The organisation of the FDR116Z1 r.o.m., which presents the characters row by row at the output, makes it suitable for raster scan display systems.

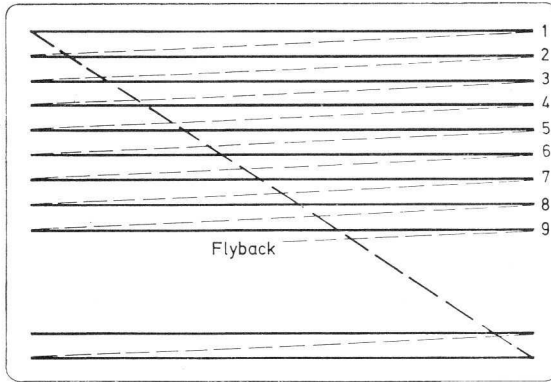
OUTPUTS			
ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
		00	01
A9 A8 A7 A6 A5 A4	A3 A2 A1	00	11
<div style="border: 1px solid black; padding: 2px; display: inline-block;"> x x </div> 0 0 0 x x 0	0 0 0		
	0 0 1		
	0 1 0		
	0 1 1		
0 0 0 x x 1	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1		
0 0 1 x x 0	0 0 0		
	0 0 1		
	0 1 0		
	0 1 1		
0 0 1 x x 1	1 0 0		
	1 0 1		
	1 1 0		
	1 1 1		

OUTPUTS

ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	OUTPUTS			
		Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
A0 A8 A7 A6 A5 A4 ┌ x x		00	01	10	11
0 1 0 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 0 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 x x 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				
0 1 1 x x 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1				

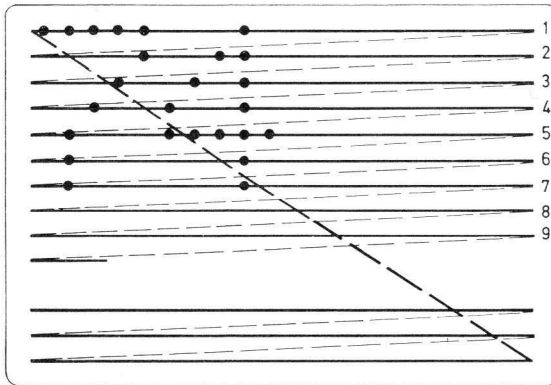
ASCII CHARACTER ADDRESS INPUTS		WORD SELECT INPUTS	OUTPUTS			
			Q5 Q4 Q3 Q2 Q1	Q6 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1	Q6 Q4 Q3 Q2 Q1
A9 A8 A7 A6 A5 A4		A3 A2 A1	00	01	10	11
$\overline{\text{X}}$ X 1 0 0 X X 0		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0	0 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0	0 0	0 0
1 0 0 X X 1		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0	0 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0	0 0	0 0
1 0 1 X X 0		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0	0 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0	0 0	0 0
1 0 1 X X 1		0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	0 0	0 0 0 0 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0 0 1 0 1 0	0 0	0 0

OUTPUTS				
ASCII CHARACTER ADDRESS INPUTS	WORD SELECT INPUTS	ASCII CHARACTER ADDRESS INPUTS		
		Q5 Q4 Q3 Q2 Q1	Q6 Q4 Q3 Q2 Q1	Q5 Q4 Q3 Q2 Q1
A9 A8 A7 A6 A5 A4	A3 A2 A1	00	01	10
				11
	0 0 0			
	0 0 1			
	0 1 0			
	0 1 1			
	1 0 0			
	1 0 1			
	1 1 0			
	1 1 1			
	0 0 0			
	0 0 1			
	0 1 0			
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	0 0 1			
	0 1 0			
	0 1 1			
	1 0 0			
	1 0 1			
	1 1 0			
	1 1 1			



(a) Raster scan

(a)



(b) Dot characters on raster scan

(b)

α8203

Fig. 11.21—Principle of raster scan display

The principle of raster scan display is shown in Fig. 11.21. A spot on the face of a CRT sweeps the complete screen in a series of lines (Fig. 11.21a). If bright-up pulses are applied to the grid or cathode of the CRT at the correct times during the sweep, characters can be built up as shown in Fig. 11.21b.

This type of display can be built up by the use of an r.o.m. character generator, and MOS shift-registers used as recirculating memories to refresh the display at each scan.

Fig. 11.22 shows the basic parts of a raster scan character display

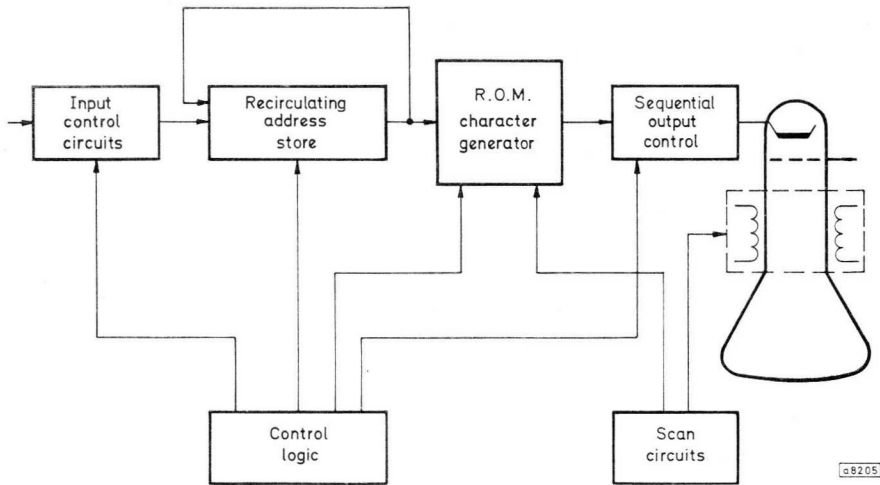


Fig. 11.22—Basic functional blocks of raster scan display system

system in block form. The recirculating memory contains the r.o.m. addresses of all the characters required for display. These addresses are fed sequentially to the r.o.m. Because characters are built up of various numbers of dots but are spread over seven scan lines, each address must be presented seven times in synchronism with the line scan signals. To generate a line of characters, the address of the first character is applied to the r.o.m. at the beginning of the scan line. This causes the five bits of the first of the seven lines to be produced at the output of the r.o.m. These five dots are sequentially applied to the CRT cathode as bright-up pulses, under the control of the sequential output control logic.

The first five dots of character 1 appear at the first part of line 1 of the raster scan. The recirculating store then provides the address of the second character to the r.o.m. and as the scan moves across the screen the first (upper) five dots of character 2 are displayed on line 1. This process continues until line 1 of the scan is completed. The scan generator then produces a flyback signal and begins to scan line 2. At this time character 1 is again addressed by the store and the control logic ensures that the dots for row 2 of this character are displayed on the tube face, followed by row 2 of character 2 and so on. The process continues until row 7 of the characters has been displayed on line 7 of the scan. This procedure produces one complete line of text, and the procedure continues as the remainder of the tube face is scanned to build up a number of complete lines of text.

In a practical system for producing N_L lines of text each of N_C characters, the address memory must contain $N_C \times N_L$ addresses. Each address consists of six bits. Since each character consists of seven lines, each having five dots plus a single dot space between characters, the total number of bits of data used to provide the display is $6 \times 7 \times N_C \times N_L$. In a system providing, for example, 10 lines of 50 characters the total number of bits used in the display is 21 000, each line consisting of 300 dots. Such a display might be accommodated in a 100-line display, allowing for a 3-line space between rows of text. If the display is refreshed at 20ms intervals, each line scan takes approximately $160\mu\text{s}$ allowing for flyback time. The data rate is therefore $160/300\mu\text{s}$ per bit or 534ns, equivalent to a data frequency rate of 1.88MHz. Each address must be available to the r.o.m. for at least five dot periods, that is, $2.66\mu\text{s}$ at each scan.

Fig. 11.23 shows the system requirements for a raster scan display system in simplified form. The six recirculating shift-registers containing the character addresses each consist of 320 bits, this length being conveniently made up of $256+64$ bits, as provided by standard size shift-registers.

The clock generator feeds a $\div 6$ counter which is decoded. The first five pulses are used to feed the r.o.m. outputs from the 6-bit shift register to the video amplifiers. The $\div 7/\div 3$ block produces a 3-bit partial address for the r.o.m. (to determine the line in use) and also generates a 3-line space between lines of text. The sixth pulse generates a space between characters. The clock generator runs at the display 'bit rate', and after division by six it provides the clock for the recirculating memory at the character rate. To keep track of the stored characters two address counters are required, one to count the scan or text line and the other to count the character positions within a line of text. To enter characters to the display at the required position, and to allow for editing functions, comparators and input address buffers are also required. The outputs of these circuits control the input buffer and the marker generator.

Larger raster displays

Alpha-numeric display systems using raster scan on CRTs are being standardised to display 16 lines, each of 80 characters. This type of display can be built with a television monitor system having a 50Hz field scan at 312 lines per field. (This is a normal 625-line display without interlace.) Such a display line has a line scan time of $64\mu\text{s}$, of which $52\mu\text{s}$ can be used as the display time.

Each line contains 80×6 dots which must be produced in $52\mu\text{s}$, giving

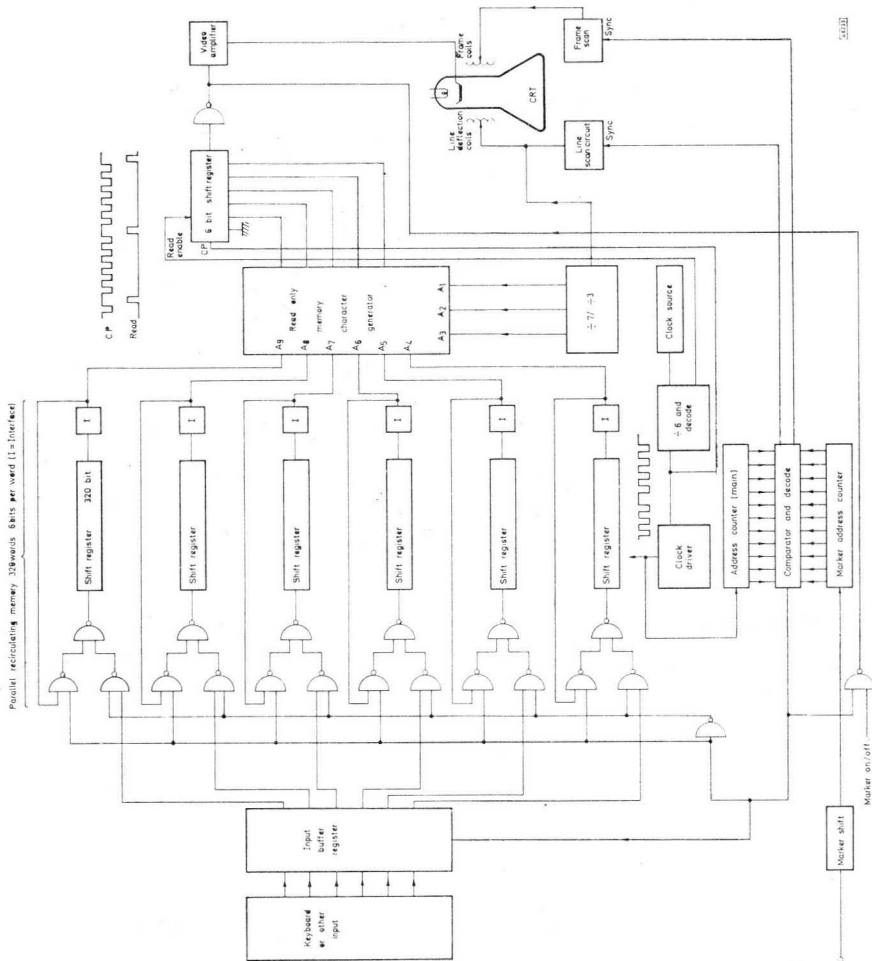


Fig. 11.23—System requirements for raster scan display

a clock rate of $480/52\mu\text{s} = 9.2\text{MHz}$ or 108ns/bit . The total time for each character space on one line scan is $6 \times 108\text{ns} = 648\text{ns}$. The r.o.m. address pulses for each character must be available for at least 648ns . Because the FDR116Z1 has a typical access time of 750ns and because of other circuit delays, it is necessary to multiplex either two or three read-only memories to provide the character information at the correct times. The circuit delays must be compensated for in the system design.

DATA ROUTERS

Data routing applications occur, for example, in control equipment, calculators and computers. The requirements are that input data which

may appear on one or more lines is routed to one of several output lines under the control of a number of address lines. Fig. 11.24 shows a 'black box' interpretation of the requirements.

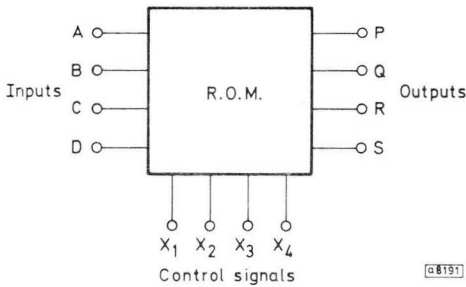


Fig. 11.24—Data router

As an example, consider the following as the requirements for a specific data routing problem.

Table 11.1

Condition No.	Input	Output
1	A	→ P
2	A	→ Q
3	A	→ R
4	A	→ S
5	B	→ Q and S
6	B	→ P and R
7	C	→ R
8	D	→ P
9	D	→ R
10	D	→ P, Q and S

For simplicity, the requirements for the 'A' input will be considered first in order to give an outline of the principle of operation.

For the 'A' input the routing required is:

Table 11.2

A	→ P
A	→ Q
A	→ R
A	→ S

The four conditions can be satisfied by four address conditions, say X₁ X₂, which can be accommodated in two address bits.

Table 11.3

Condition No.	Condition	Address	
		X ₂	X ₁
1	A → P	0	0
2	A → Q	0	1
3	A → R	1	0
4	A → S	1	1

In operation, the addressed output must have the same logical level as the 'A' input. This can be achieved by the use of a simple r.o.m. of 16 bits (four words of four bits) in which X₁ X₂ address the required output, and the level of the 'A' signal ('1' or '0') is used as a third address bit. The contents of the r.o.m. to perform the required operation are as shown below.

Table 11.4

Inputs (address)			Outputs (word)			
A	X ₂	X ₁	P	Q	R	S
0	0	0	0	0	0	0
1	0	0	1	0	0	0
0	0	1	0	0	0	0
1	0	1	0	1	0	0
0	1	0	0	0	0	0
1	1	0	0	0	1	0
0	1	1	0	0	0	0
1	1	1	0	0	0	1

Because zeros are presented at the r.o.m. output if no word is addressed, this table can be reduced to:

Table 11.5

Inputs (address)			Outputs (word)			
A	X ₂	X ₁	P	Q	R	S
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	0

Thus in condition 1, where the 'A' input is required at 'R', the main input address X₂ X₁ is '1' '0'; if 'A' is a '1' the output word 0010 provides a '1' at the 'R' output, and if 'A' is a '0' the output is 0000 giving a '0' at 'R'. This

principle can be extended to cover a more-complex data routing problem such as that in Table 11.1 by the addition of more addresses. The problem posed in Table 11.1 could be solved by the use of a 40-bit r.o.m. organised as ten words of four bits, the contents and address requirements being as shown in Table 11.6. The $X_3 X_4$ address bits define the zone of operation, that is, which of the inputs is to be operated on. Address bits X_1 and X_2 define the required function. This principle can obviously be extended to cover far more complex data routing problems.

Table 11.6

Input				Required output				Address			
A	B	C	D	P	Q	R	S	X_4	X_3	X_2	X_1
1	X	X	X	1	0	0	0	0	0	0	0
1	X	X	X	0	1	0	0	0	0	0	1
1	X	X	X	0	0	1	0	0	0	1	0
1	X	X	X	0	0	0	1	0	0	1	1
X	1	X	X	0	1	0	1	0	1	0	0
X	1	X	X	1	0	1	0	0	1	0	1
X	X	1	X	0	0	1	0	1	0	0	0
X	X	X	1	1	0	0	0	1	1	0	0
X	X	X	1	0	0	1	0	1	1	0	1
X	X	X	1	1	1	0	1	1	1	1	0

RANDOM-ACCESS MEMORIES

MOS random-access memories find applications in systems ranging, for example, from computer storage to control systems and data logging.

The FDQ106 is a monolithic, 128-bit random-access read/write memory and is shown in Fig. 11.25. It is organised as two 64-bit memories with six common single-rail address inputs and two separate outputs; it is used as a 64-word, 2-bits per word memory. It requires a single-phase clock strobe pulse to refresh the data stored in all the memory cells simultaneously and to change the data stored in a cell in the write mode. It also incorporates a chip disable that inhibits both data inputs and output buffers for expanded memory applications. The memory is activated in the write mode by applying a write control pulse; at all other times it is in the read mode.

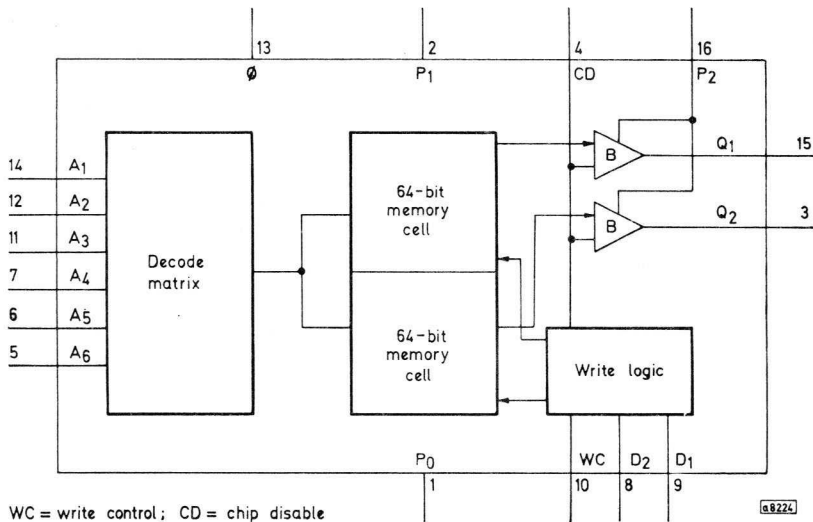


Fig. 11.25—FDQ106 read/write random-access memory

A simple arrangement for using a single memory as a 64-word 2-bit store is shown in Fig. 11.27. Data is written into the memory when the write control line (WC) is negative. At other times the memory is in the read mode. During change of address the strobe line ϕ must be negative, and the write control line must be at zero.

Memories of this type can be used to build up systems of, say, 64 words of 8 or 16 bits by using a number of parallel addressed memories as shown in Fig. 11.26. The figure shows the parallel address lines driven by TTL gates with 15V output ratings. The data inputs are also fed from TTL gates. The read/write control logic is not shown.

Stand-by low-power operation

In power-sensitive applications, if it is desirable to maintain the FDQ106 in a stand-by condition with no loss of stored data, all d.c. supplies to it may be shut down and the stored data can be preserved merely by maintaining a 10kHz strobe clock rate. Since, essentially, all d.c. power dissipation is in the address input inverters, decode circuits and output buffers, the power required to preserve the stored data is limited to reactive strobe power and whatever leakage current occurs at the strobe input lead. Because the reactive strobe power is frequency dependent, the lowest allowable frequency should be used for stand-by operation. A strobe frequency of less than 10kHz may be used if the ambient temperature is

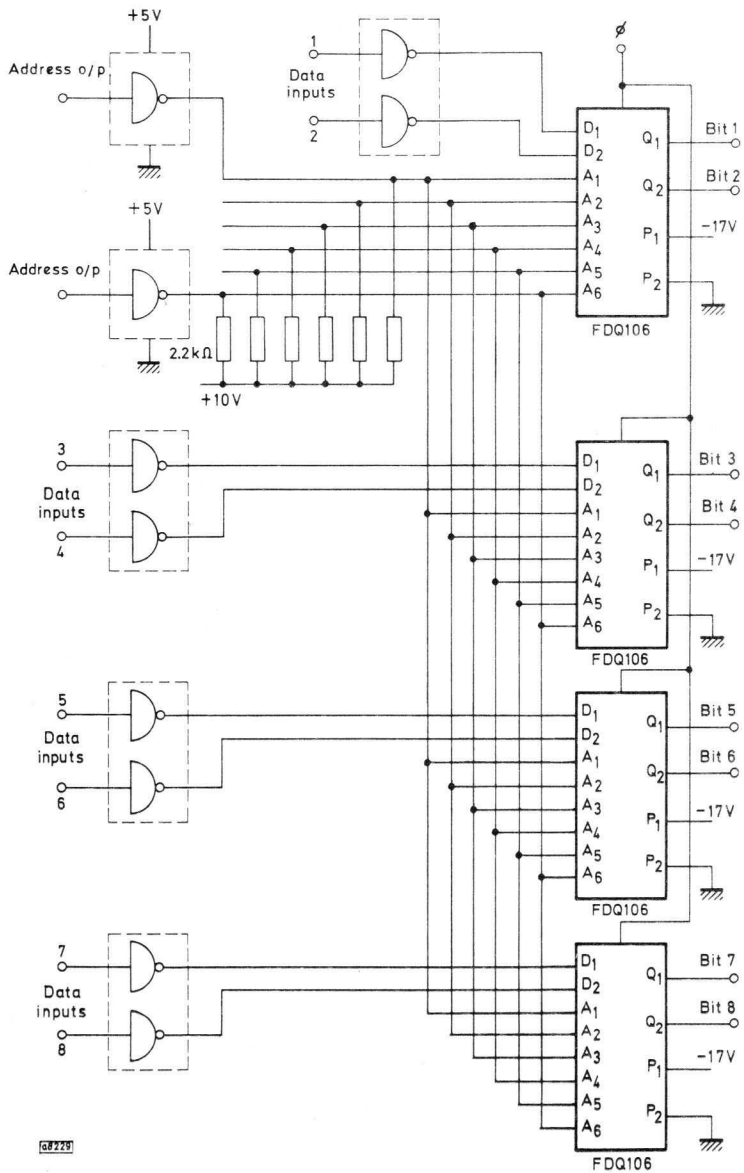


Fig. 11.26—Parallel addressed memories

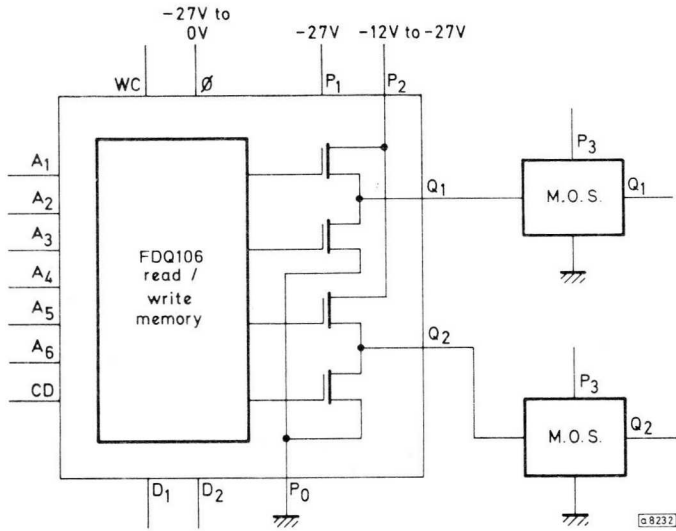


Fig. 11.27—Single memory as a 64-word 2-bit store

less than $+85^{\circ}\text{C}$. When d.c. power is returned to the circuit the strobe must be LOW and all normal timing considerations must be observed when operating the memory in this mode.

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